I-T Tables and BIRD42.3 Revisited

Bob Ross
Teraspeed Consulting Group

IBIS Summit Meeting
Design Automation Conference 2004
San Diego, California

June 8, 2004

TERASPEED
CONSULTING
GROUP

Some IBIS Summit Presentations Regarding Power Rails for SSN and I-T

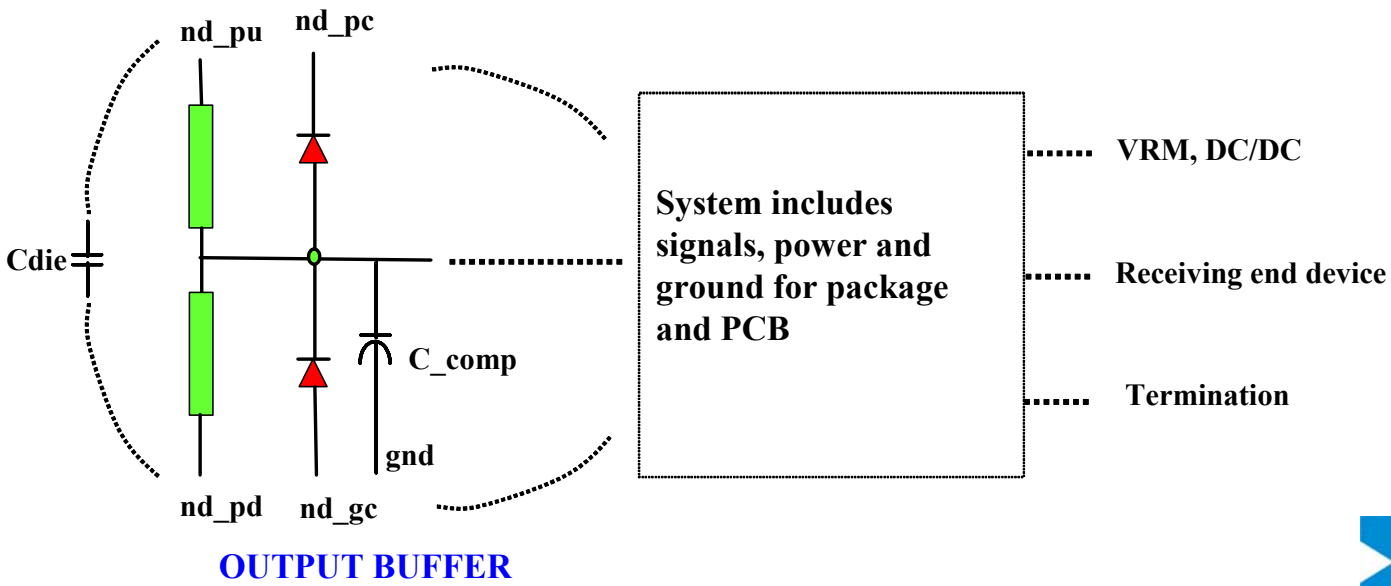
- See IBIS home page Articles, summits on the eda.org IBIS summits site
- Raymond Chen, Sigrity: Feb. 2004 (add Cdie)
- Bernhard Unger, Siemens: Jan. 2000 (adds Cpre and adjustment for rail collapse)
- Ambrish Varma, NCSU: June 2004 (simultaneous switching noise and rail collapse)
- Norio Matsui, Applied Simulation Technology: Jan. 2001 (LSI power and ground model for EMI simulation with internal clock and paths)
- Etienne Sicard, INSA: Sept. 2001, Sebastien Calvet INSA Jan. 2002 (chip core I-T model for EMI)
  - I-T source for supplies derived from statistical switching model simulations (with AMS or SPICE or simplified SPICE)
  - Part of ICEM model and IC-Emit freeware (Feb. 20, 2004)
  - Can be modeling using multi-lingual extensions
- C. Kumar, Cadence: Jan., Feb. 1998, Bob Ross Feb. 1998: (I-T tables in buffers and BIRD42.3)

TERASPEED CONSULTING GROUP

Adding Cdie (Chen, February 2, 2004)

After Adding Cdie

1. Driver end waveform will be more accurate.
2. Noise simulation will be more accurate, for example, power and ground noises at die pad.

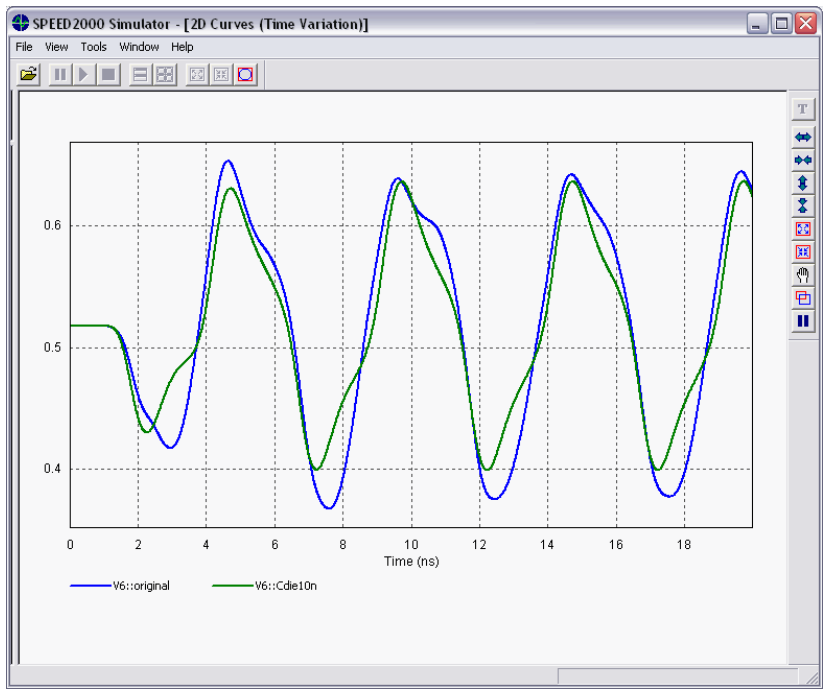


TERASPEED CONSULTING GROUP

Chen, Continued

After Adding Cdie

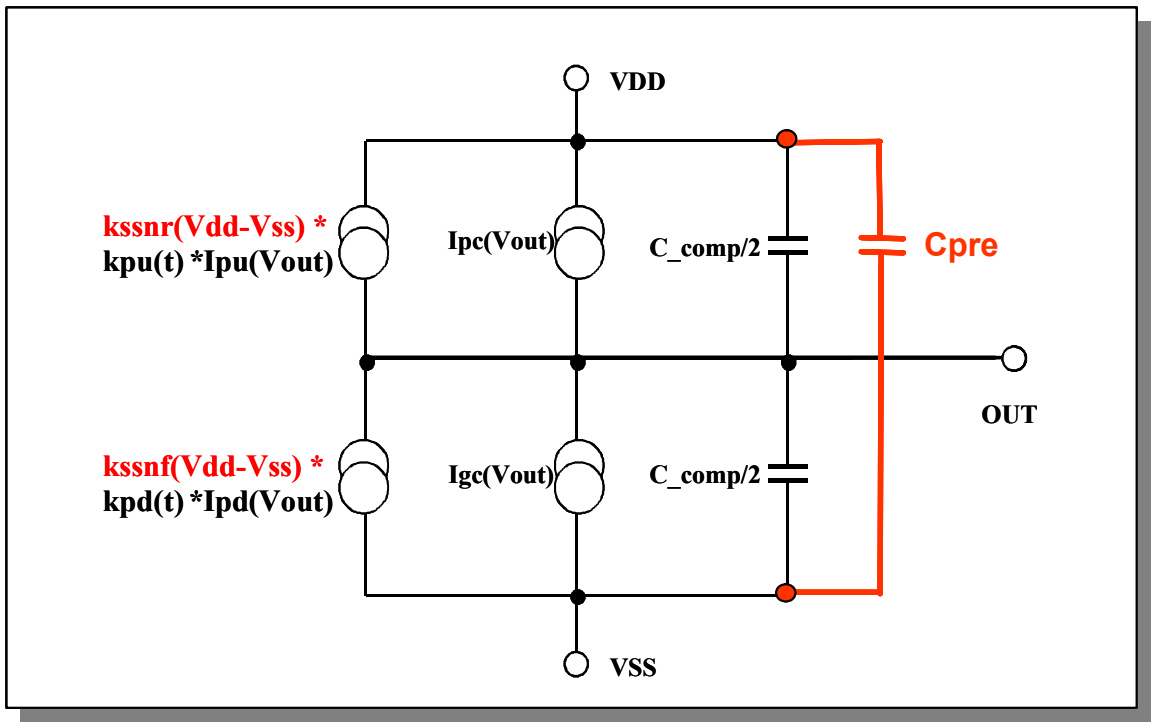
1. **With a few nF Cdie, victim line (stuck low) at the board receiver end shows less noise.**



TERASPEED CONSULTING GROUP

Rail Collapse Adjustment (Unger, January 31, 2000)

Enhanced two Waveform Behavioral Model including prestage Vdd-Vss Capacitance



Cpre:
Vdd-Vss prestage Capacitance

Evaluation:
SPICE simulation using a capacitance bridge

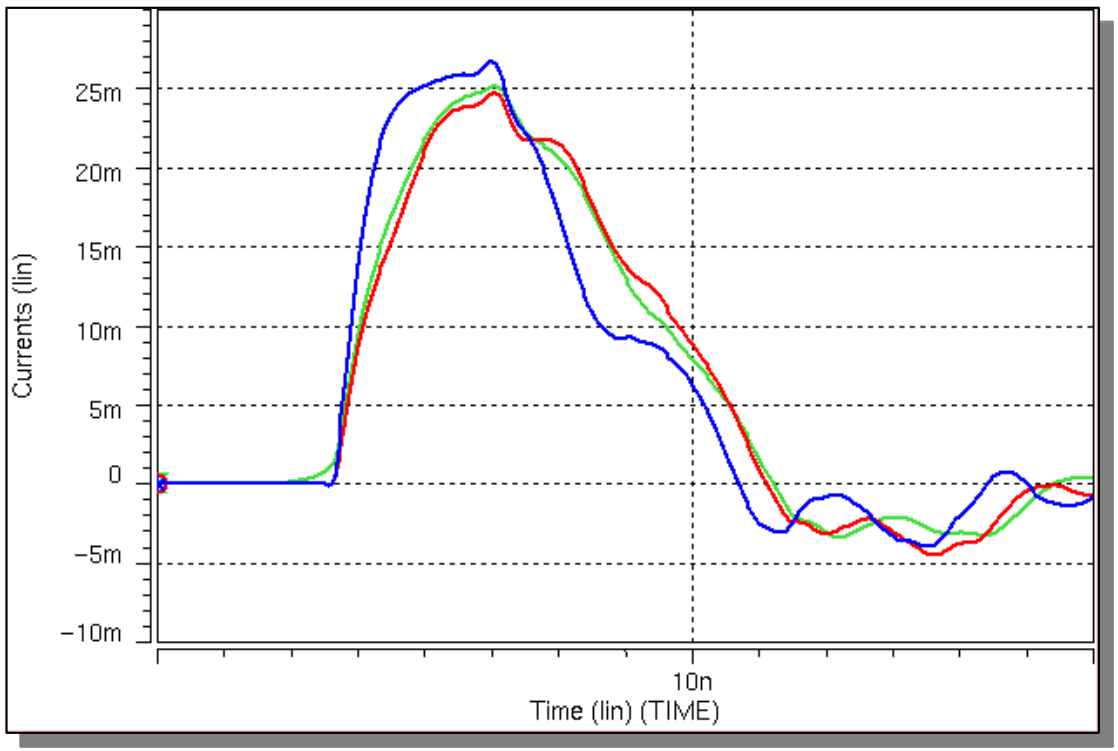
TERASPEED CONSULTING GROUP

Unger, Continued

BD4 SSN analysis results (rising edge)

Vdd current of 1 bd4 buffer

Number of SSO = 10



Supply currents:

Transistor based

Enhanced behavioral including prestage C

Usual behavioral

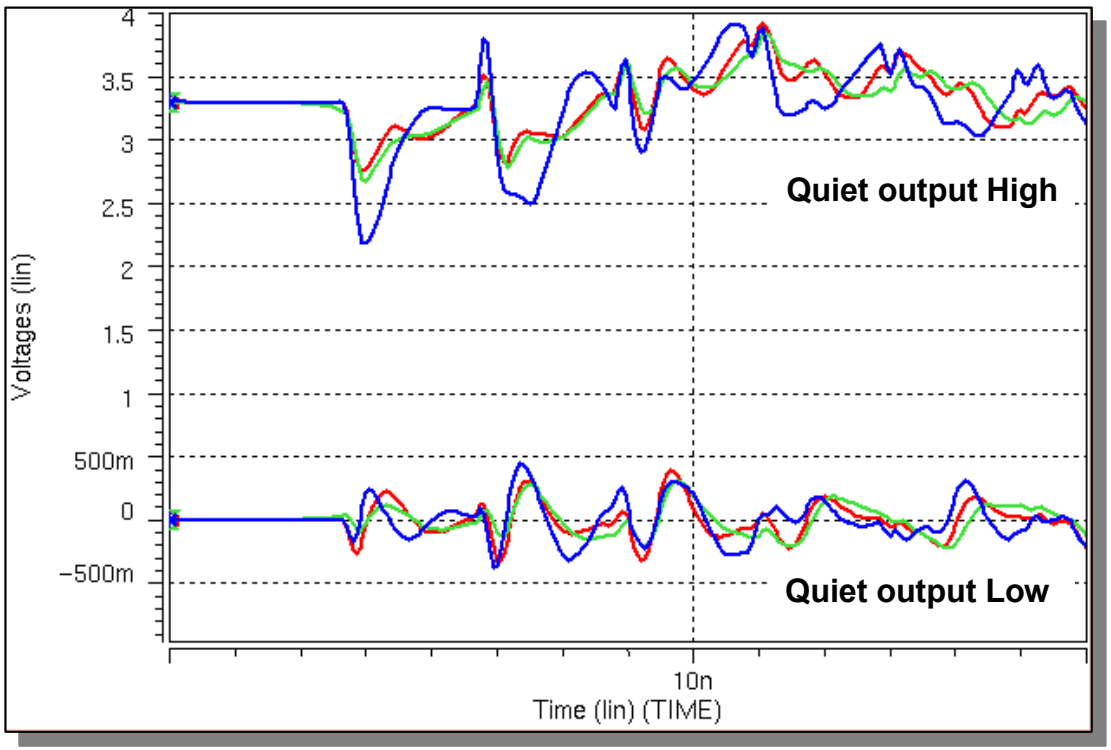
TERASPEED CONSULTING GROUP

Unger, Continued

BD4 SSN analysis results (rising edge)

Noise on quiet outputs

Number of SSO = 10



Quiet output signals:

Transistor based

Enhanced behavioral including prestage C

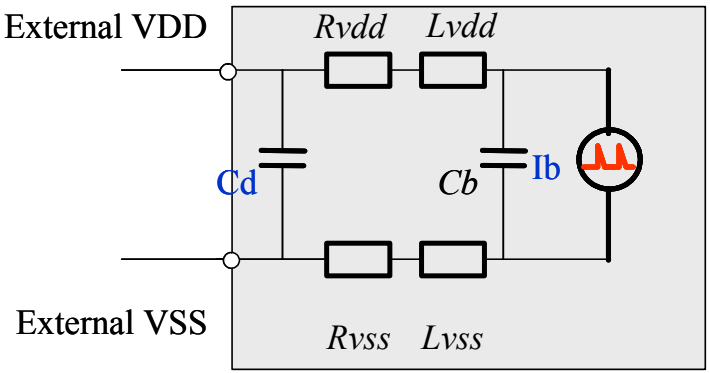
Usual behavioral

TERASPEED CONSULTING GROUP

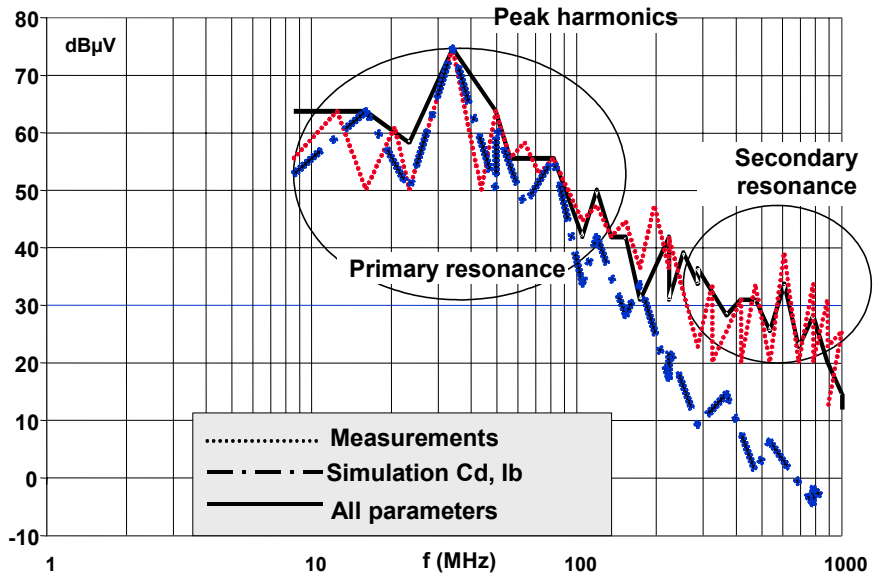
Core Emission I-T Model for EMI (Calvet, Jan. 28, 2002)

4. Core Emission Model

ICEM includes a simple core model, not handled by IBIS



Basic parameters	Cd, Ib
Advanced param.	R,L,Cb

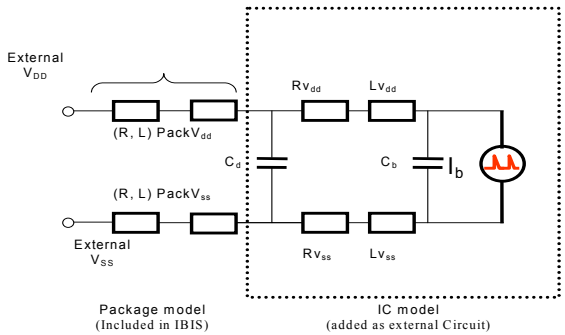


TERASPEED CONSULTING GROUP

Core Model I-T Emission Models as Multi-Lingual SPICE Extension of IBIS

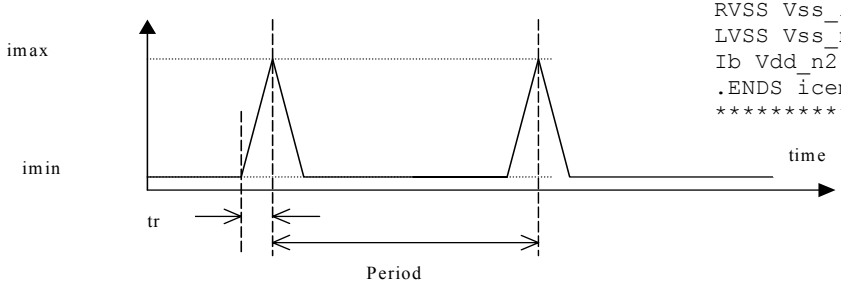
68HC12 D60

ICEM MODEL



LPackVss=2.2nH
LPackVdd=2.2nH
Cd=3.2nF
Rvss=2
Rvdd=2
Cb=50pF

Current generator Ib



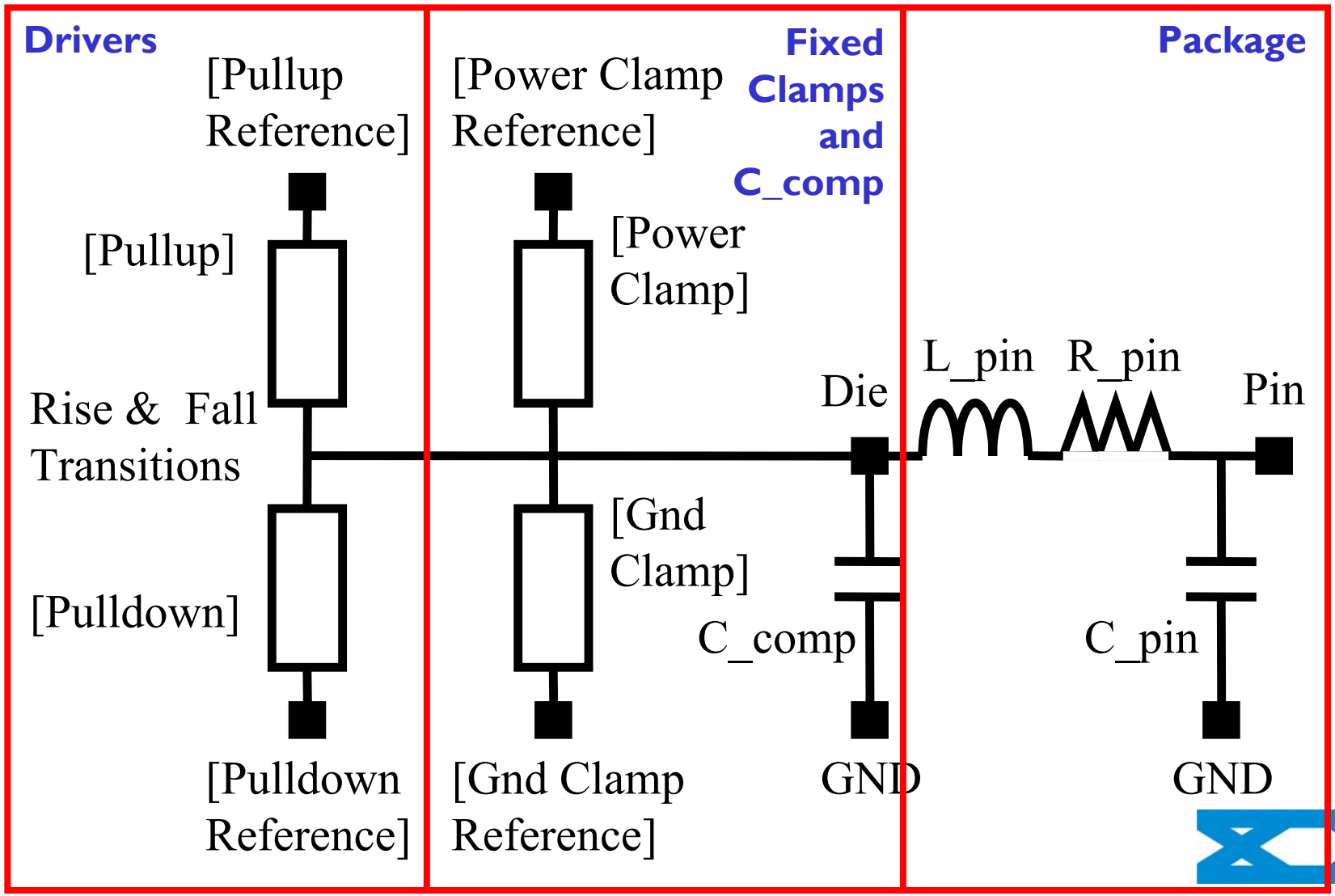
Period = 31.25ns.
Imin = 0.01A
Imax = 0.4A
Tr= 1ns

```
| Some additions to the IBIS model:
|*****************************************************************************
[Circuit Call]  ICEM
| mapping  port      node
Port_map   vdd_ic    12
Port_map   vss_ic    14
[End Circuit Call]  | Code connecting 12 to 65 and 14 to 66 on the die
                    | is not shown
|*****************************************************************************
[External Circuit] ICEM
Language SPICE
| Corner    corner_name    file_name  circuit_name (.subckt name)
Corner     Typ            icem_d60.spi  icem_typ
| Ports are in same order as defined in SPICE
Ports      vdd_ic    vss_ic
|*****************************************************************************

*  Separate SPICE file icem_d60.spi
*******************************************************************************
.SUBCKT icem_typ vdd_ic vss_ic
RVDD Vdd_ic Vdd_n1  2
LVDD Vdd_n1 Vdd_n2  2.2n
Cd Vdd_ic Vss_ic  3.2n
Cb Vdd_n2 Vss_n2  50p
RVSS Vss_ic Vss_n1  2
LVSS Vss_n1 Vss_n2  2.2n
Ib Vdd_n2 Vss_n2 PULSE(0.01 0.4 10ns 1.0ns 1.0ns 0.01ns 31.25ns)
.ENDS icem_typ
*******************************************************************************
```

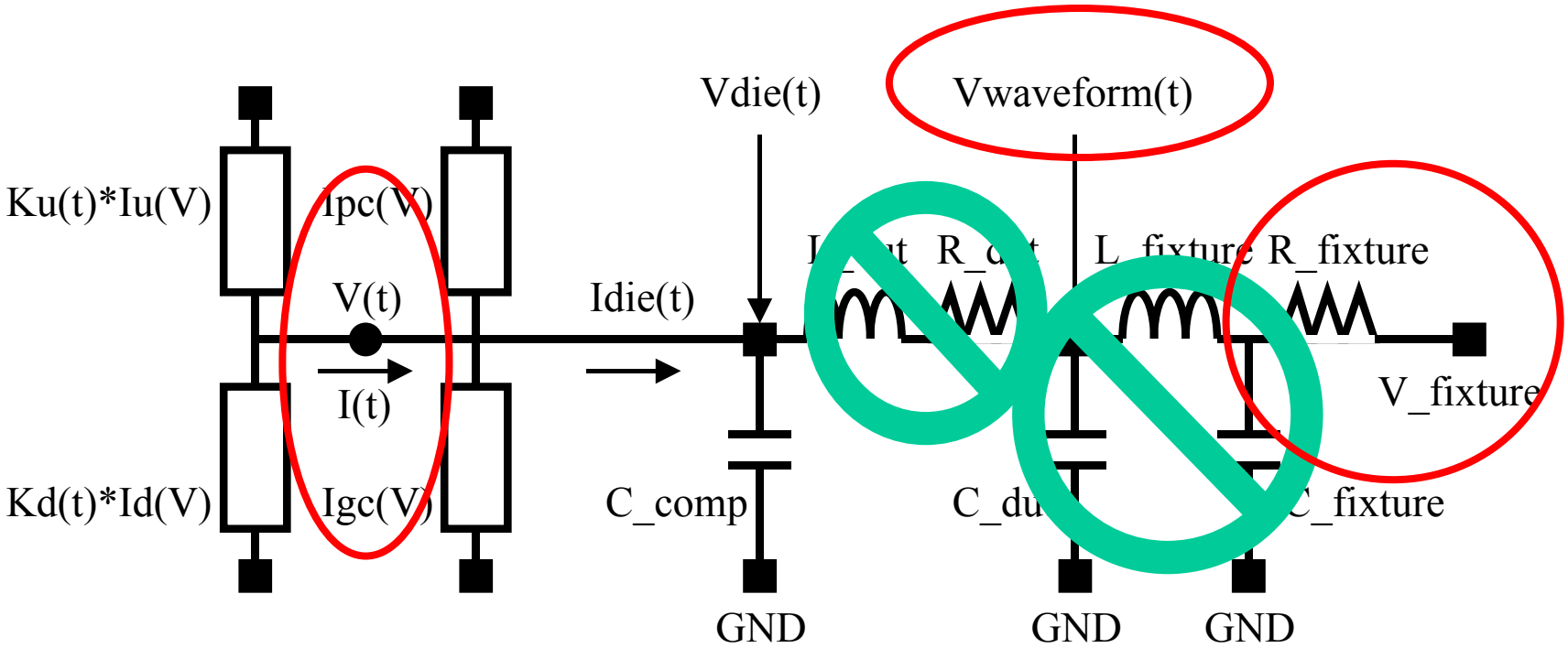

TERASPEED CONSULTING GROUP

BIRD 42.3 - IBIS 2.1 Buffer Model



TERASPEED CONSULTING GROUP

V-T Tables and Fixture Loads to get Ku(t), Kd(t) for Rise, Fall Edges



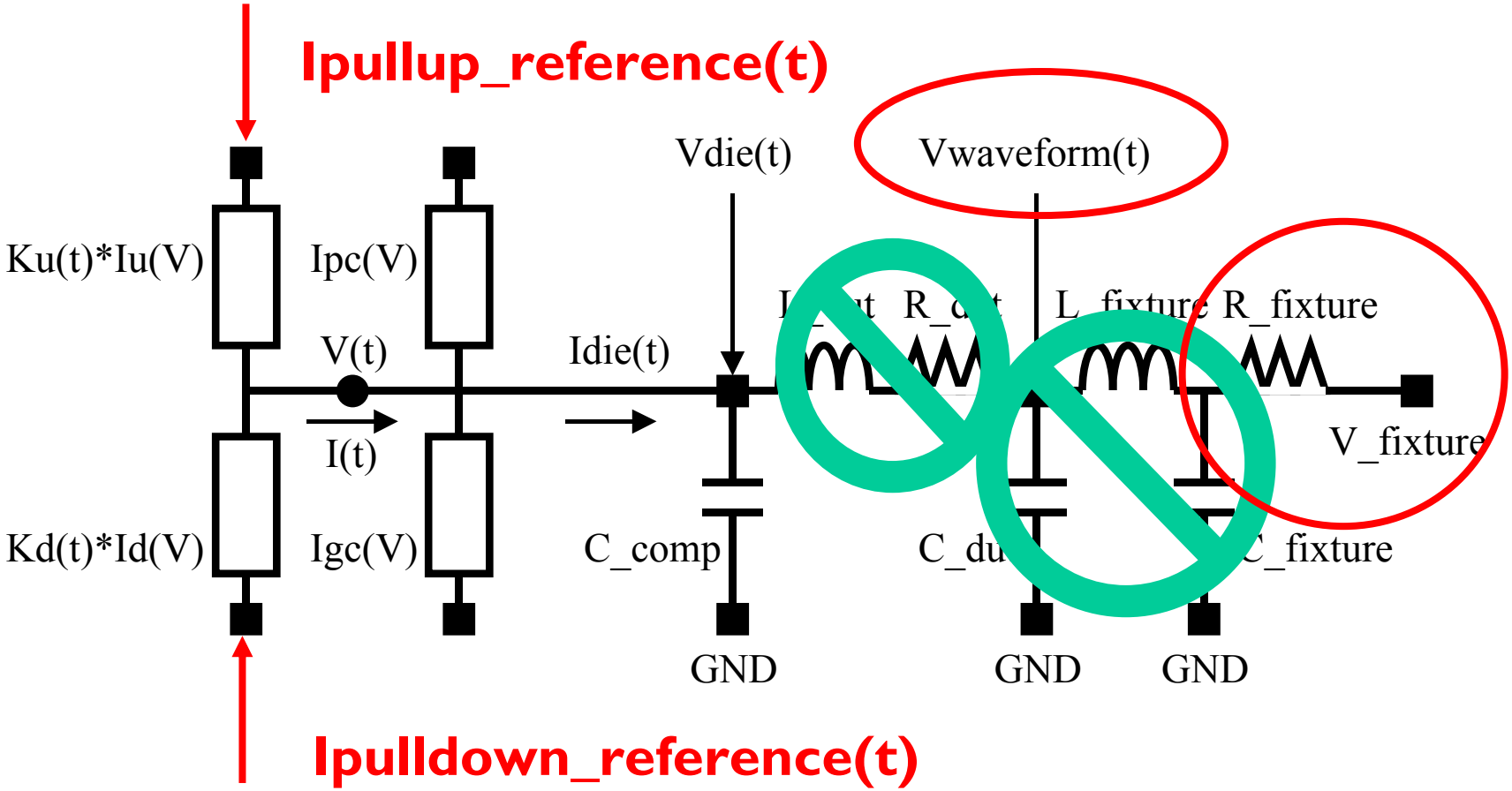
Recommended Loads:

50 Ω to Vcc

50 Ω to Gnd

TERASPEED CONSULTING GROUP

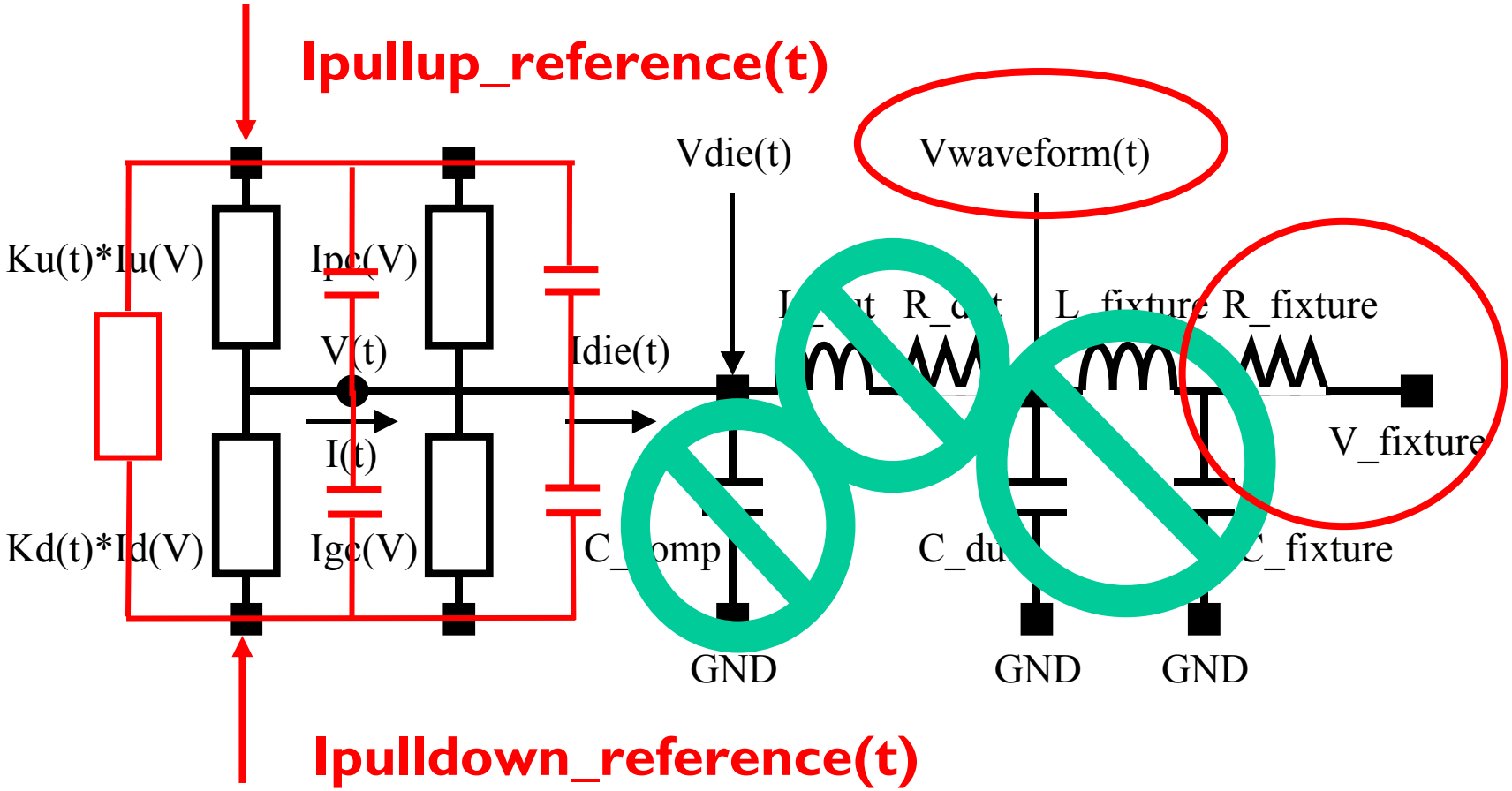
BIRD42.3 Proposal (V-T and I-T tables)



(0, 1, or 2 current tables allowed)

TERASPEED CONSULTING GROUP

Current Definition Problem?
EDA Spec., Processing Ambiguity



(0, 1, or 2 current tables allowed)

TERASPEED CONSULTING GROUP

BIRD42.3 Assumptions and Limitations

- Adds V-T and I-T PAIRS for a given fixture load
  - Under [Rising Waveform] or [Falling Waveform] table
    - Keep V-T table and its fixtures
    - [Pulldown Reference Current], [Pullup Reference Current] tables (None, both, or either - such as one easiest to isolate)
    - Could support Open_drain, Open_source and ECL models
- Currents might need to be separated from clamps or other current paths in the model
  - Permanent (internal terminator "clamps")
  - Individual capacitance to each rails
  - Very complex for tools to automatically do this

TERASPEED CONSULTING GROUP

Some Format Considerations

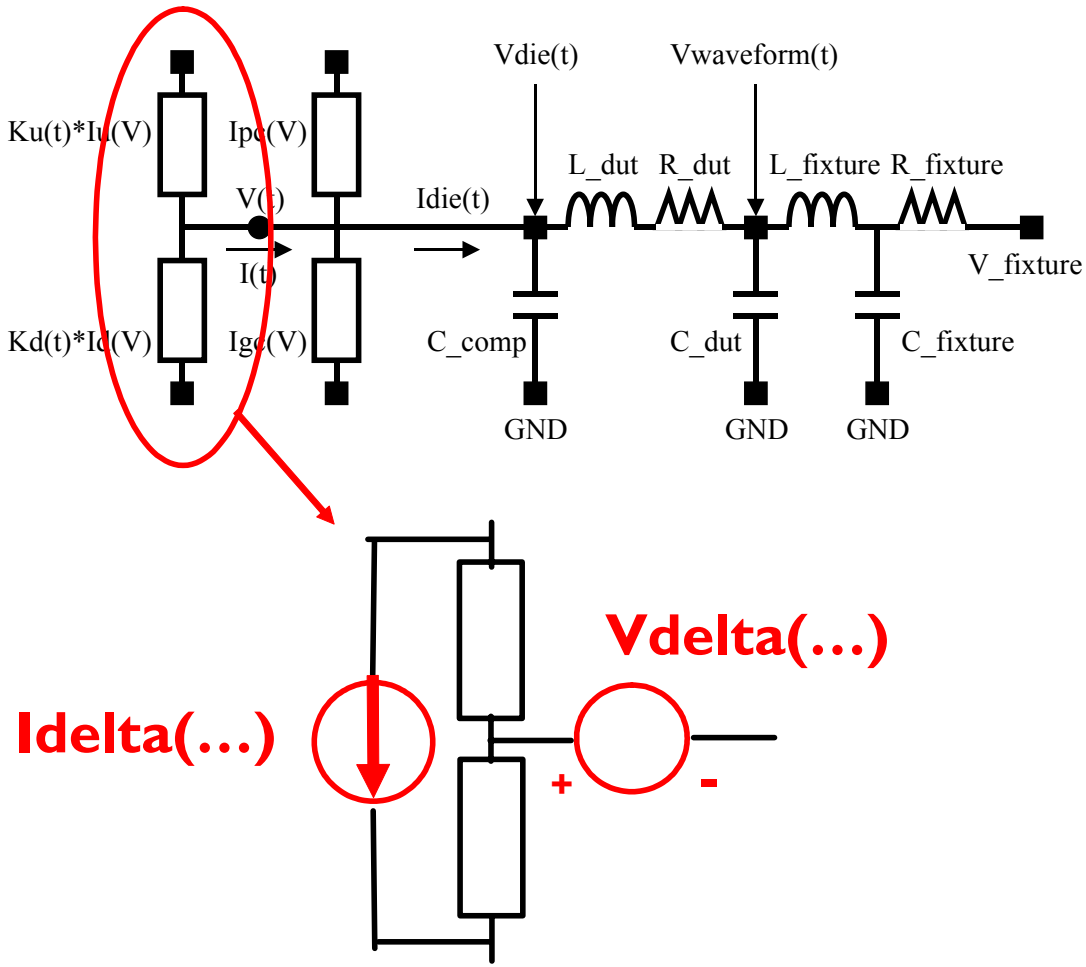
- Referenced to driver rails since clamps are optional, and clamp currents hard to isolate
- Extension limitations may exist
  - Driver Schedule – rails not necessarily common or inherited, nor currents easily allocated to scheduled models
  - Submodels – same rails, but triggered internal behavior needs triggered I-T data
  - True differential buffer current allocation not considered
  - ECL Pullup Reference Current allocation/algorithm issue

TERASPEED CONSULTING GROUP

EDA Tools: Several Choices for Over-specified Cases

- Voltage based solution option
  - Use the V-T table information first for V-T data matching via existing Ku(t), Kd(t) extraction methods
  - May not capture as accurately the rail currents
- Current based solution option
  - Use the current information first (more direct solution of Ku(t) and Kd(t) with excess common "crowbar" currents)
  - But not match the V-T data as well
- Augmented model for voltage and current matching
  - Adds Idelta(…) and Vdelta(…) variables for more matching options and strategies
    - (E.g., match V-T tables, then match currents with Idelta)
  - Idelta(), Vdelta() could be a function of Iu and Id currents
  - More research needed

Augmented Model (Ross, Feb. 26, 1998)



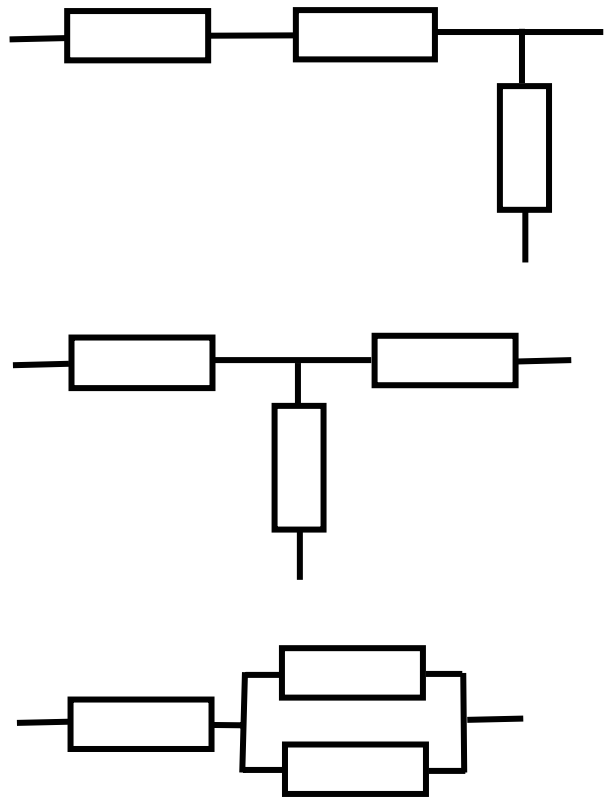
TERASPEED CONSULTING GROUP

I-T Extraction Issues

- SPICE based (most practical)
  - Still must carefully isolate rail currents and then post-process them to fit topology
  - Can use ideal current sense mechanism (0 V voltage sources)
  - Still may deal with fast current edges and spikes
  - Best R_fixture, V_fixture choices need to be investigated for overall accuracy (V_fixture = GND, Vcc, Vcc/2, etc.)
- Measurement based (many issues and may be impractical)
  - Includes the package
  - Current probe bandwidth & impedance vs. 50 ohm measurements
  - Or standard 1 ohm test load distortion
  - Several buffers on same power line
  - Unrelated currents from non-driver circuits

Package Model for Supplies (not explicit in IBIS)

- R_pin - L_pin - C_pin
  - Implied, but puts C_pin across voltage source
  - Could be distributed model (small T-line)
- R_pin - C_pin – Lpin
  - C_pin to reference rail, to ideal GND or across L_pin to Vcc
  - Moves C_pin from rail



Summary and Observations

- BIRD42.3 explained
  - Issues and compromises to fit in IBIS
  - EDA simulation options
- Other approaches given
  - SSN model extensions
  - Core I-T models for ICEM
- What is the problem?
  - Simultaneous switching noise of selected buffers?
  - Board power distribution issues and internal core noise?
- Do I-T tables help solve the problem?
  - I-T IBIS buffer extension or other proposals?
  - Multi-lingual extensions?
  - EDA tool support?

TERASPEED CONSULTING GROUP