IBIS Summit @ DAC 2005:

Library Characterization & Modeling: Issues, Recommendations and Possible Solutions

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Sponsors

Si2's Design Technology Council (DTC)

Ericsson	IBM Corporation	Philips Semiconductors
Freescale Semiconductor	Infineon AG	Sun Microsystems
Hewlett Packard	LSI Logic	Intel

Reality: 90nm onwards!

○ All tough problems at 130nm are still here,… and there are some new ones at 90nm…

Challenges: 90nm onwards!

○ Significant divergence between predicted & measured performance due to variability in process & temperature

  • Requires more complex and accurate libraries, including models for interconnect

○ Chips designed with multi-V_t and multi-voltage regions

  • Requires multiple libraries

○ Semiconductor processes will get more complex at 65nm …and beyond… which will lead to…

  • Even more complex libraries

Objective

Modeling & characterization environment:

- Increased accuracy to silicon at 90nm and 65nm

- Extendable to future technology nodes

- Support new capabilities (e.g. statistical timing)

- Maintain consistent modeling methodology

Issues

- Accuracy/consistency of library models

- Gap between requirements and capability

- Cost/Expertise needed to build accurate libraries

- Existing formats cannot express modeling needs

- Design tools closely "linked" to library

Model Accuracy

Requirements:

- ◯ Table lookup (piecewise linear)

- ◯ Arbitrary polynomials

- ◯ Current source models

- ◯ User definable equations / models

- ◯ Consistency across libraries

Capability Gap

Requirements:

○ Delay, power & signal integrity analysis

○ Multiple voltage libraries

○ Statistical modeling of process & other variations

○ Electromigration

Library Cost...

Requirements:

○ Automate characterization & modeling flow

○ Remove manual processes

○ Automate curve-fitting & model generation

○ Support hierarchical characterization

Library Format

Requirements:

○ Unambiguous syntax and semantics

○ Supported by popular industry tools

○ Independent of any specific tool

○ Community control / evolution
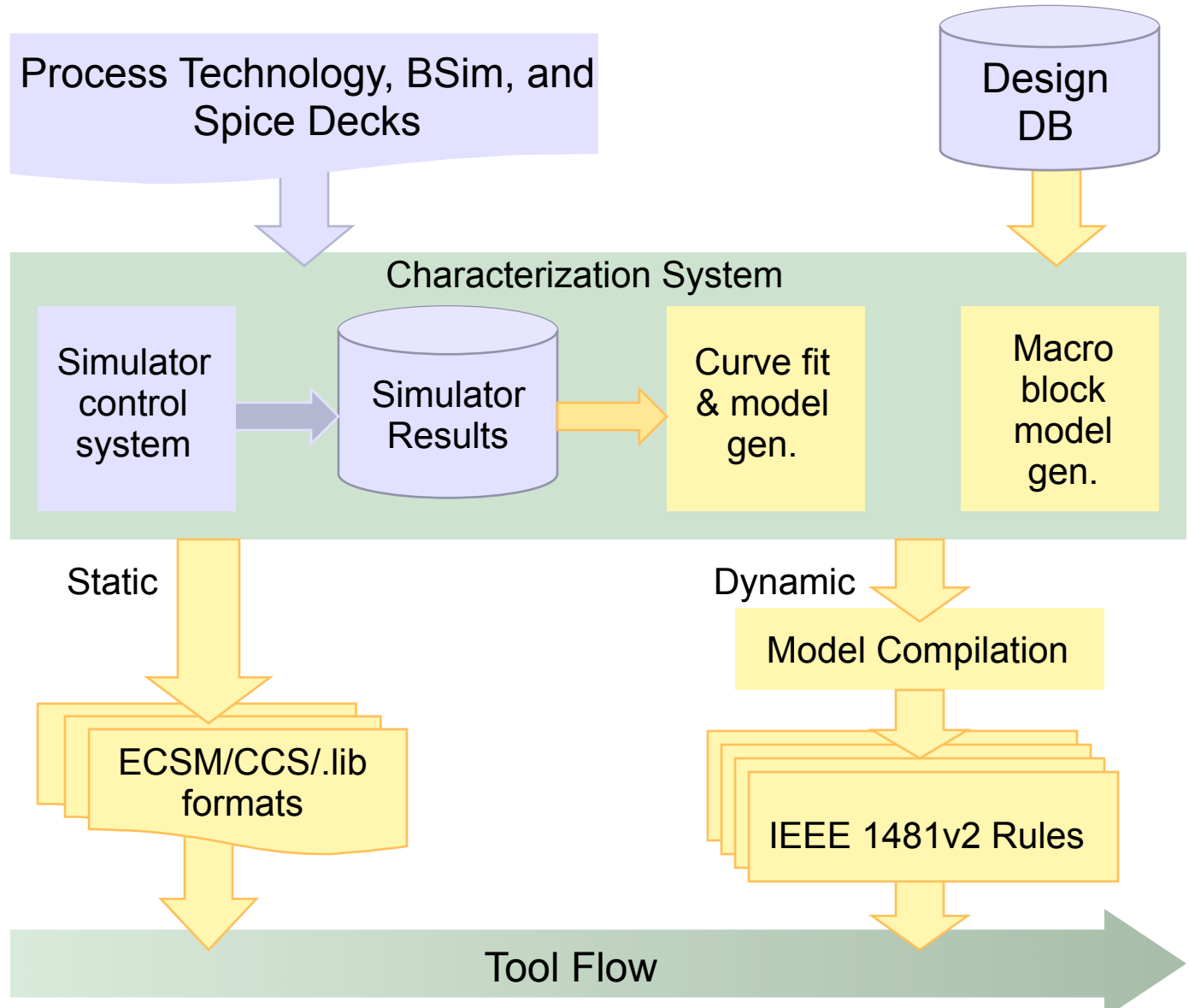
Tool "Linkage"

Requirements:

- Separation of tools from timing data / models

- API interface to modeling information

- Consistent results across all tools

- Silicon calculations defined by library provider
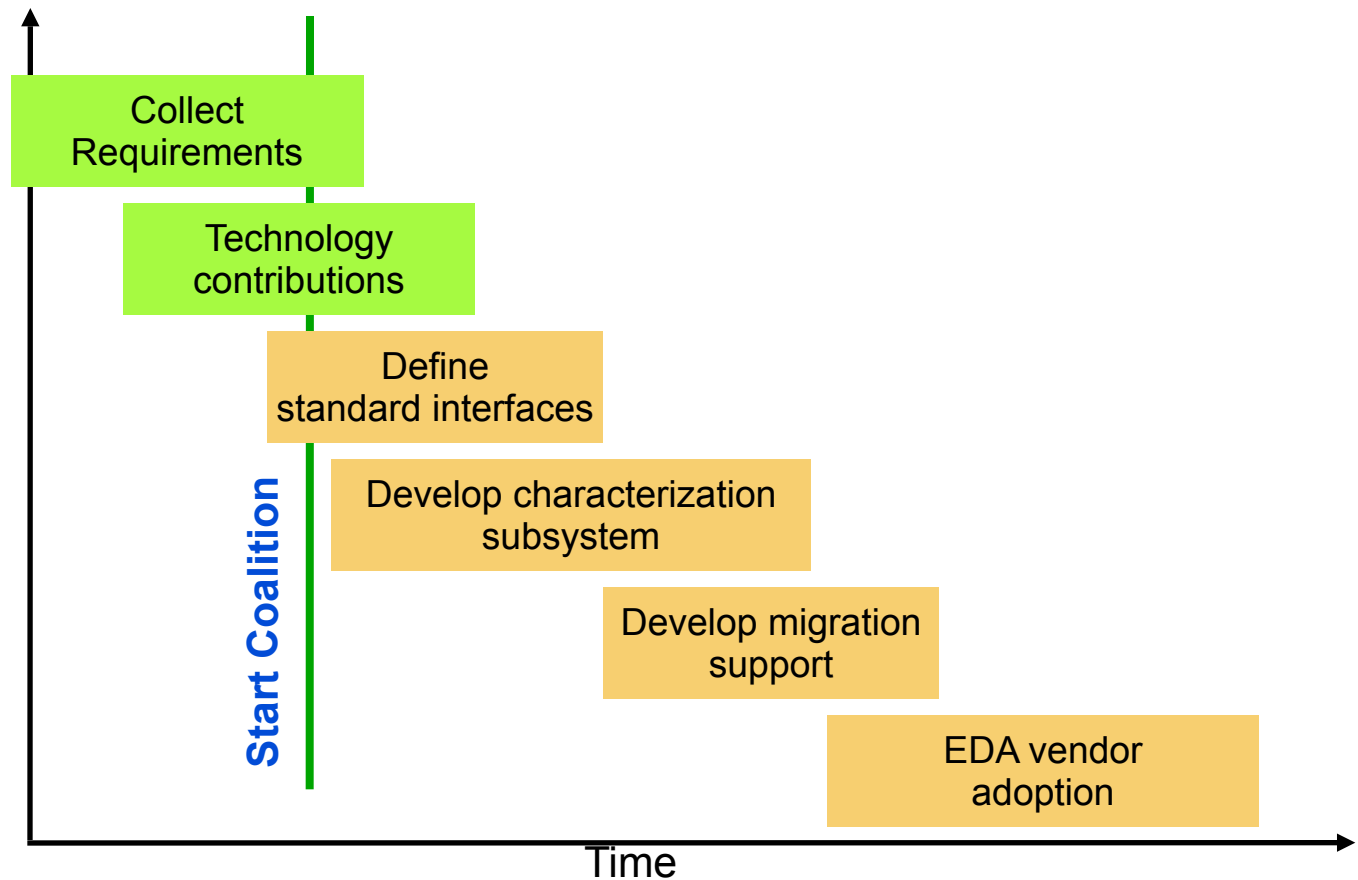
Roadmap

Library support for:

○ Statistical timing

○ Improved accuracy

- • Timing and noise

- • Leakage and total power

○ Temp variation

Modeling System

Process Technology, BSim, and Spice Decks

Design DB

Characterization System

Simulator control system

Simulator Results

Curve fit & model gen.

Macro block model gen.

Legend:

In-Scope

External

Static

Dynamic

Model Compilation

ECSM/CCS/.lib formats

IEEE 1481v2 Rules

Tool Flow

Create New Coalition

Modeled after OpenAccess Coalition

OMC Structure

Open Modeling Coalition

- Si2 members in good standing
- Chair, Vice-Chair, Secretary
- Owners of reference flow and overall implementation
- Majority voting for decisions

Technical Steering Group

- Upto 12 members
- Led by 2 chief architects
- 2/3 super-majority voting
- Owns roadmap, implementation plans
- Charters working groups
- Appoints champions for working groups

Working Groups

- Created and disbanded by TSG
- Champion from TSG is a member
- Participants are from coalition
- Chair appointed by TSG
- Initial list of WG's:
  - Interface to modeling subsystem
  - Interface for foundry information
  - Statistical timing
  - Static formats

Targeted Participants

- Integrated device manufacturers

- Silicon foundries

- Design automation vendors

- End user companies

- IP or library vendors

Open Library Modeling Meeting

Date: June 15, 2005

Time: 10:00 – 11:30AM

Place: Anaheim Convention Center, Room 202A

Si²

Summary

○ 8 Letters of intent from DTC members

○ 4 companies have submitted technology

○ BOD approval at April 7th meeting

Engaging industry players

Moving forward with formation of coalition

Open Modeling Meeting at DAC on 06/15