Multi-Gigabit SerDes System Level Analysis Using IBIS v4.1 (VHDL-AMS)

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June14th, IBIS Summit, Anaheim

Acknowledgements
(in alphabetical order)

- Luis Boluna, Cisco – Lab measurements
- Matt Hogan, MGC – IBIS v4.1/VHDL-AMS modeling
- Syed Huq, Cisco – vision and support
- Jayanthi Natarajan, Cisco – Pre layout and benchmarking
- Kim Owen, MGC – Pre and post layout
- Philippe Sochoux, Cisco – Post layout
- Eddie Wu, Cisco - IBIS v4.1/VHDL-AMS modeling

Many thanks to Andrea Fox, Michelle Havard, and Samuel Halm of Mentor Graphics

Agenda

- What is Multi-lingual Modeling
- HSPICE correlations
- Lab Measurements
- Pre/Post layout simulations
- Benchmarking
- What's next
- Conclusions
- References

IBIS Multi-lingual Modeling

- **Introduced with IBISv4.1 - February 2004**
  - **Supports modeling in VHDL-AMS, Verilog-AMS and SPICE**
- **VHDL-AMS and Verilog-AMS**
  - **International standards**
  - **Provide powerful programming languages**
  - **Tool independent**
  - **Users are free to develop their own methodology**
  - **Proprietary information is not needed.**
  - **NDA's are not required**
  - **Fast Simulations!**

What is being Modeled with IBISv4.1/VHDL-AMS

- **Case Study includes:**
  - **A 1 tap FFE Transmitter**
  - **Multiple levels of Pre-emphasis**
  - **Receiver equalization**
  - **Mixed mode model ranging from SPICE, S-parameter and transfer functions**
  - **Correlations with Lab measurements and HSPICE simulations**

IBIS v4.1/VHDL-AMS Driver Model

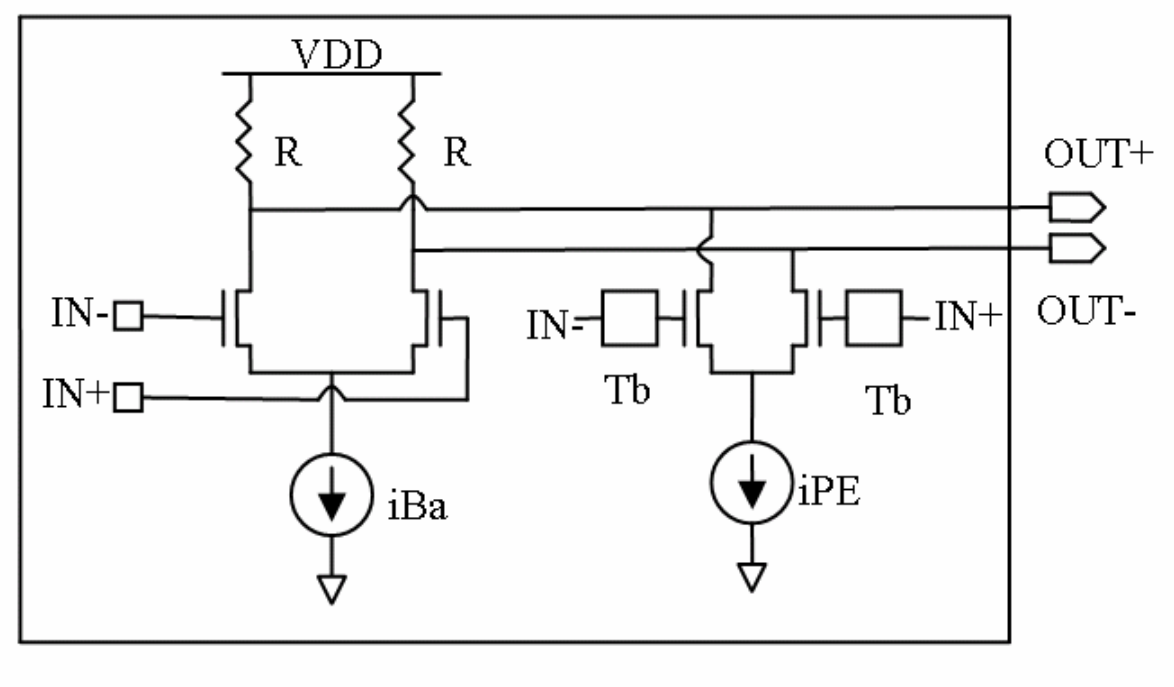


Fig.1 Model representation

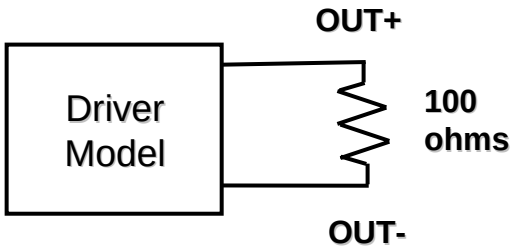
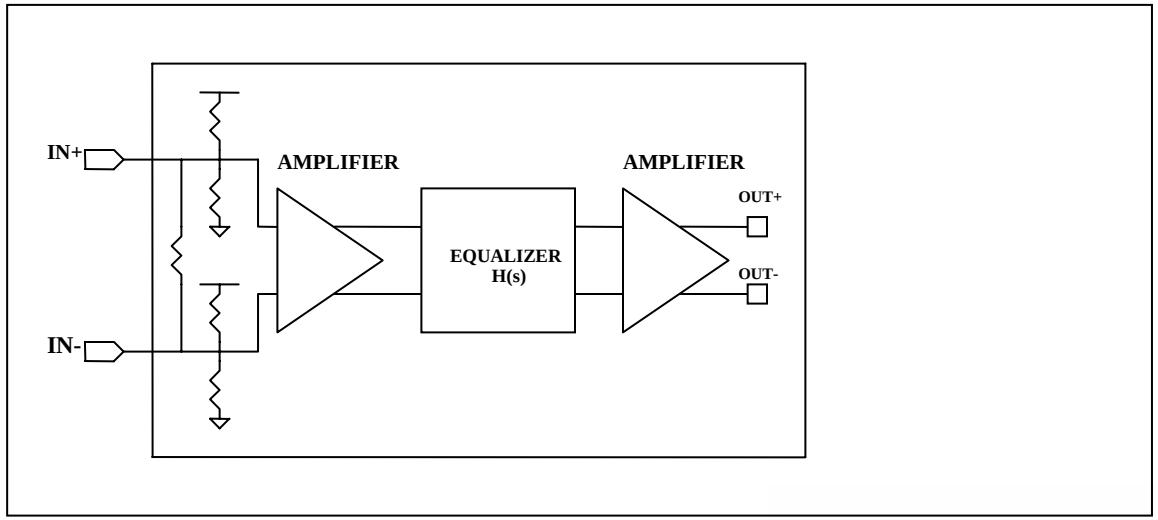


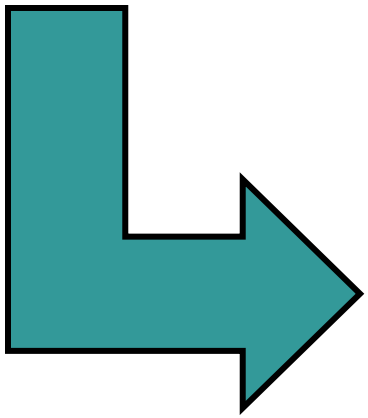
Fig.2 Loading condition

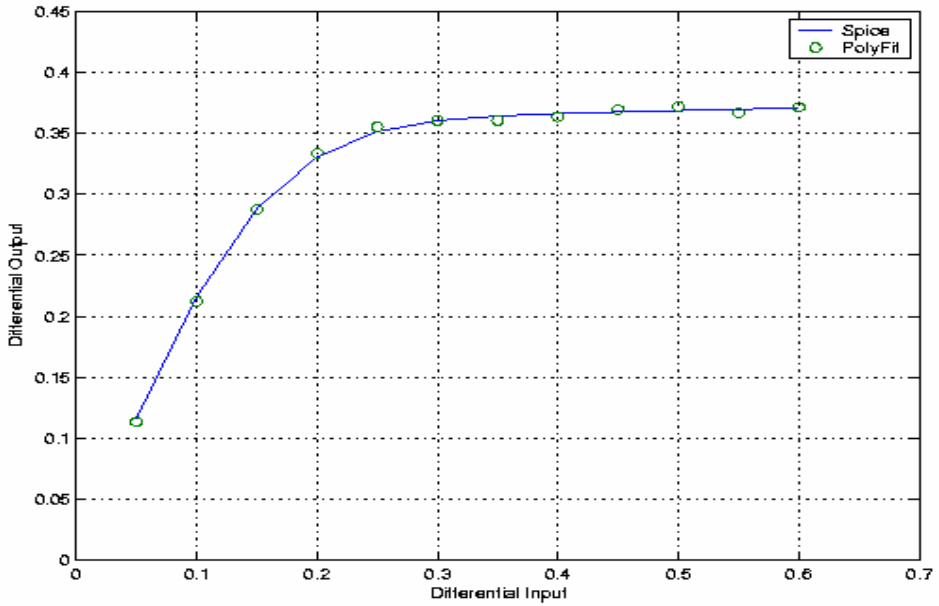
Hspice model provided by an ASIC vendor and translated into IBIS v4.1/VHDL-AMS

Hspice is a registered trademark of Synopsis, Inc.

IBISv4.1/VHDL-AMS Receiver building block







Waveform Measurements

PE=0

PE=1

PE=2

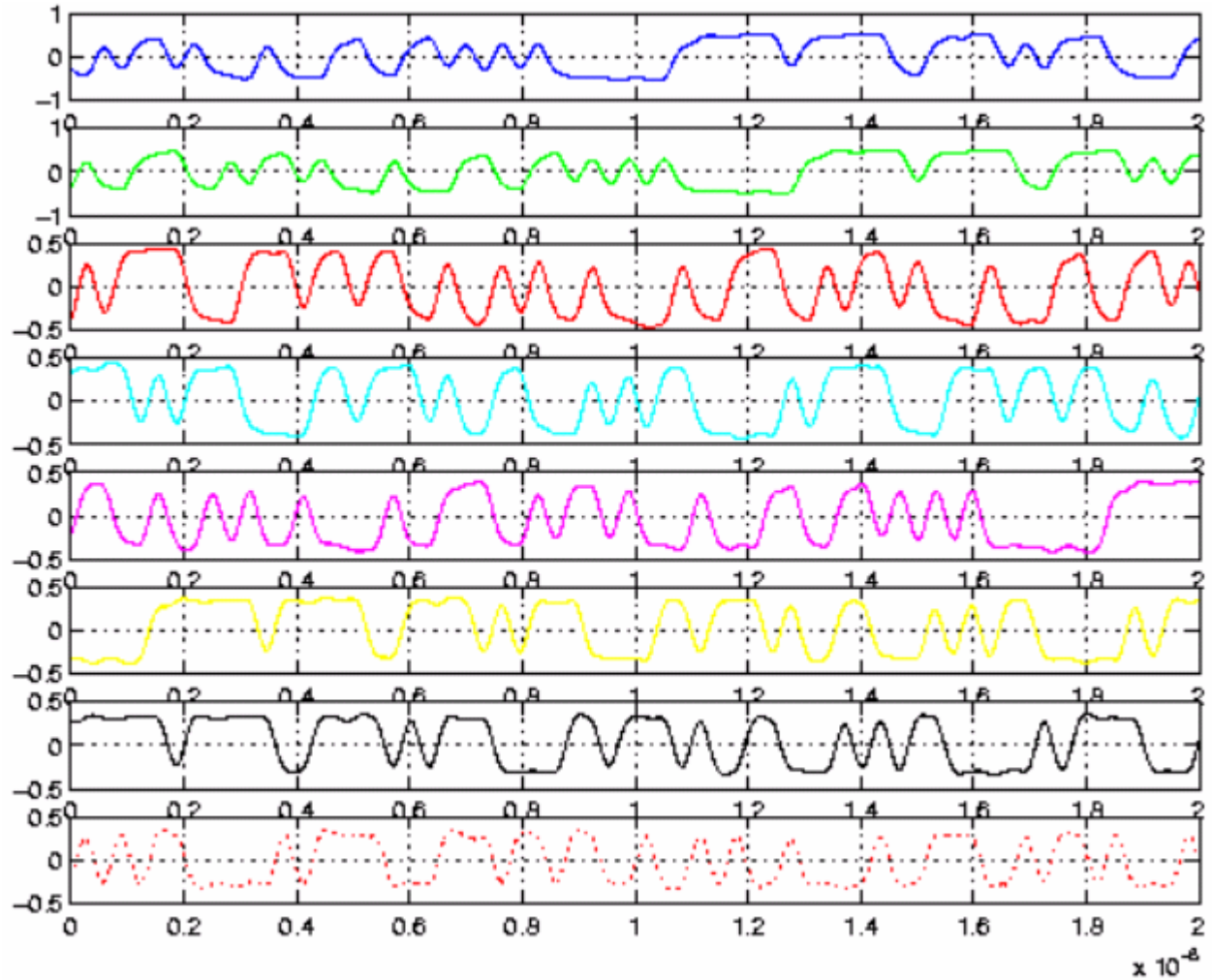
PE=3

PE=4

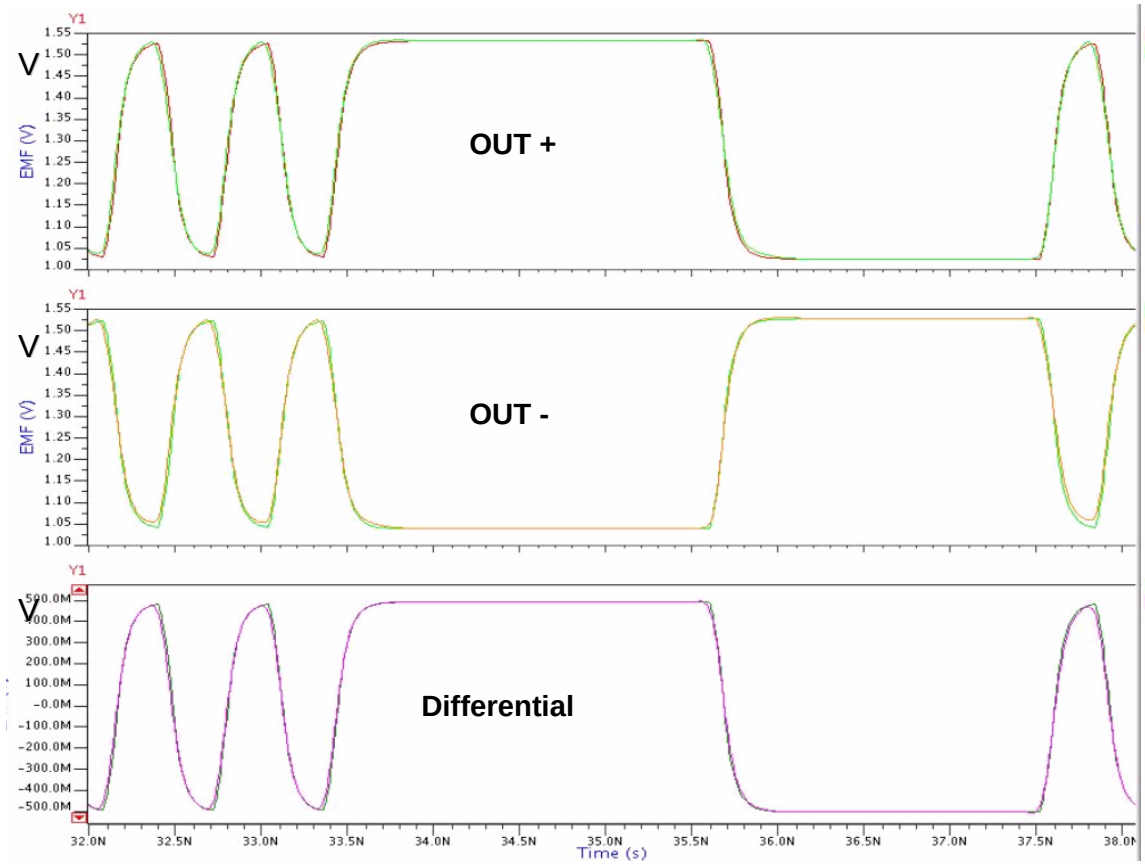
PE=5

PE=6

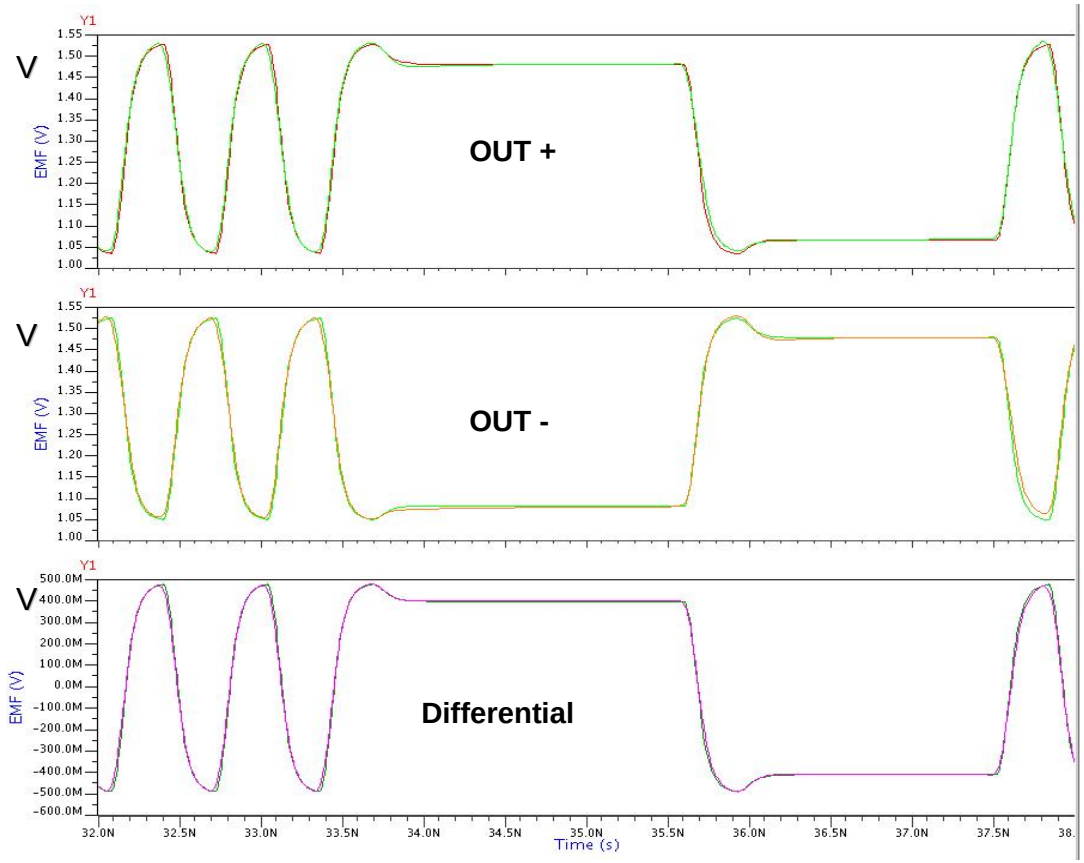
PE=7



Hspice versus IBIS v4.1 Model Correlation for PE=0 @ 3.125Gbs



Hspice versus IBIS v4.1 Model Correlation for PE=3 @ 3.125Gbs

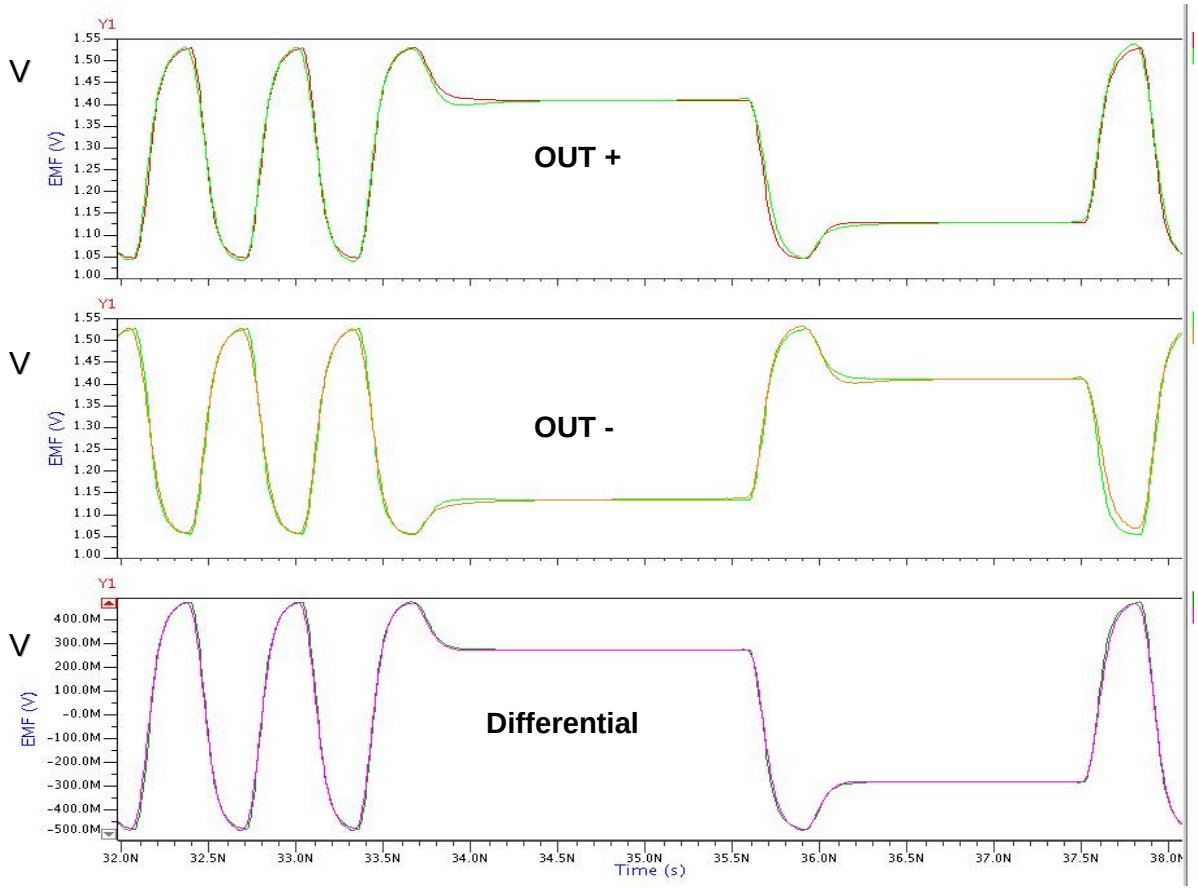


Hspice
IBIS v4.1/VHDL AMS
T(s)

IBIS v4.1/VHDL AMS
Hspice
T(s)

IBIS v4.1/VHDL AMS
Hspice
T(s)

Hspice versus IBIS v4.1 Model Correlation for PE=7 @ 3.125Gbs



Hspice

IBIS v4.1/VHDL AMS

T(s)

IBIS v4.1/VHDL AMS

Hspice

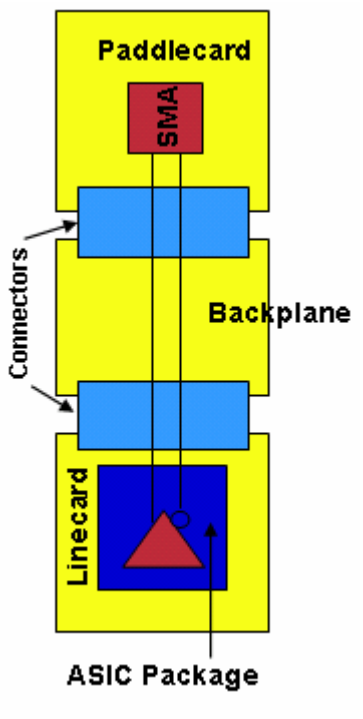
T(s)

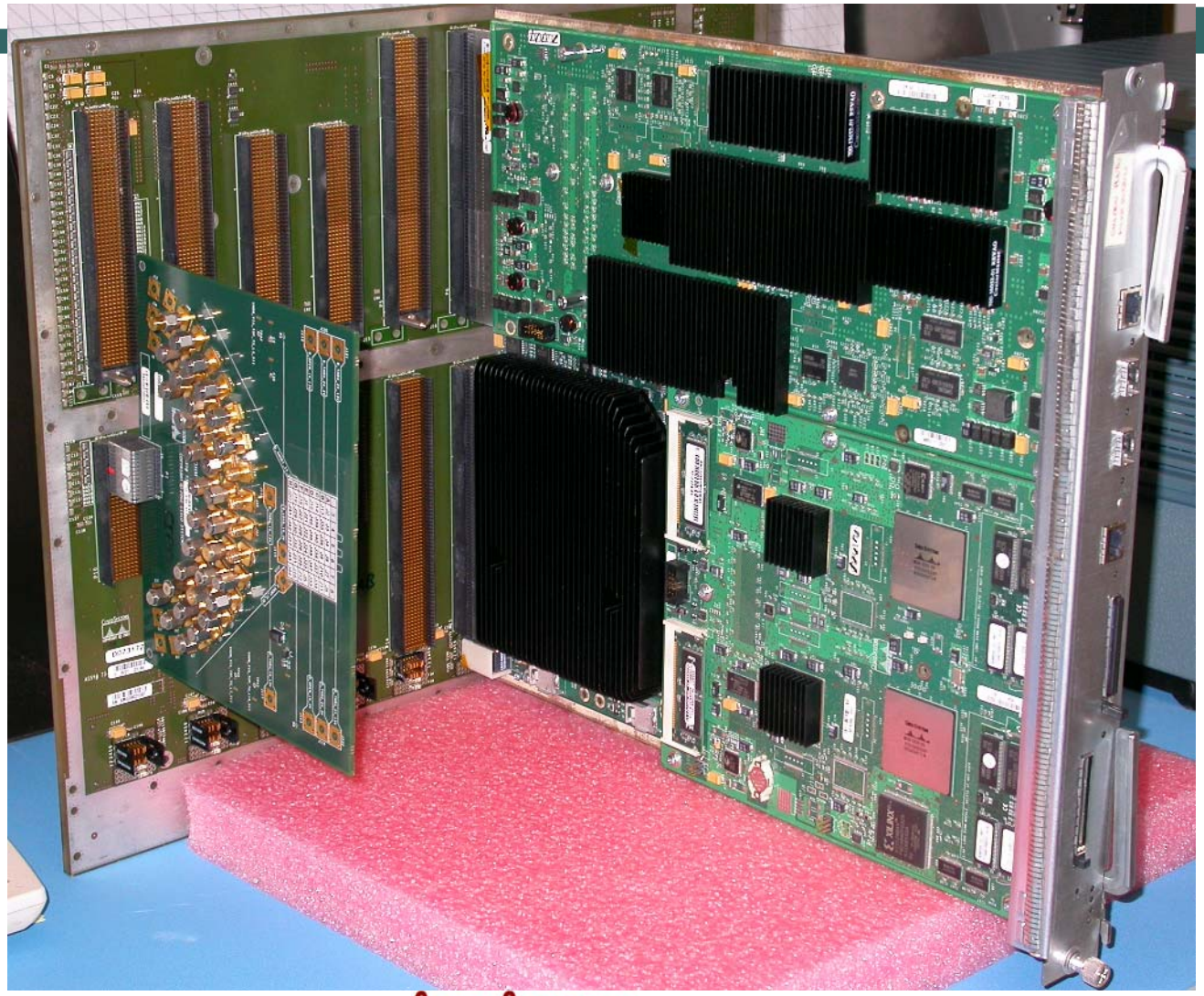
IBIS v4.1/VHDL AMS

Hspice

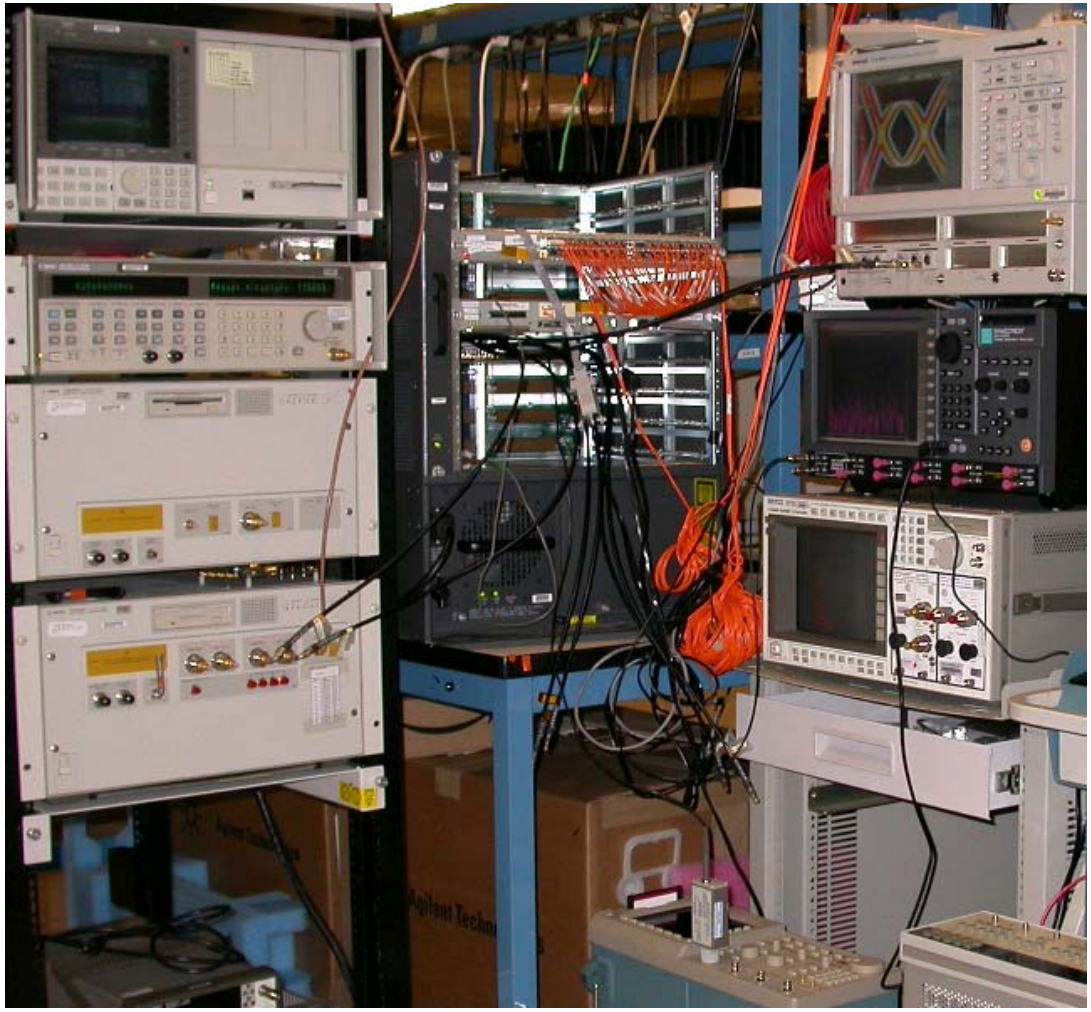
T(s)

Waveform Measurements

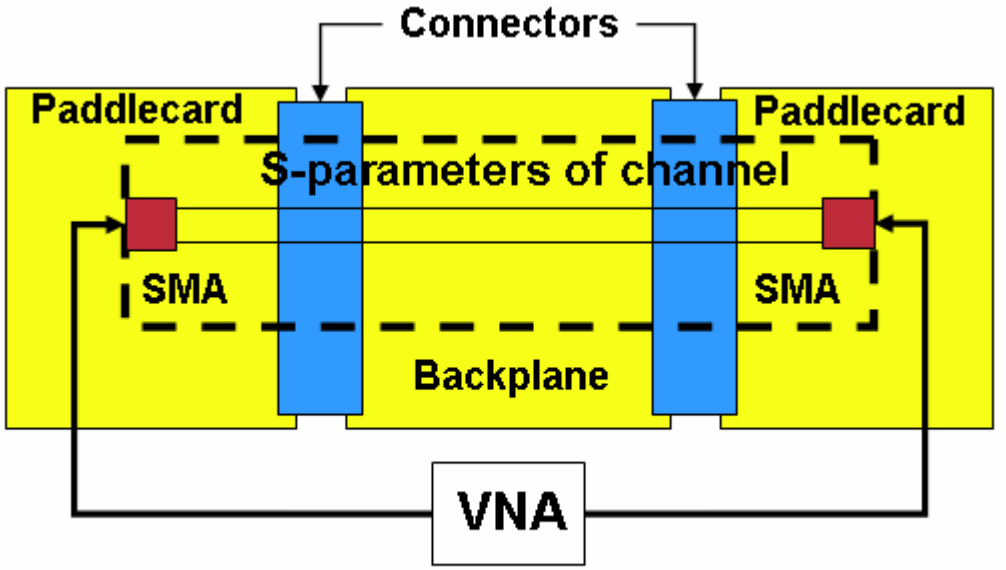




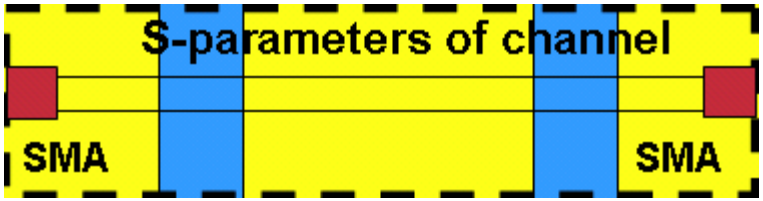
Lab Instrumentation



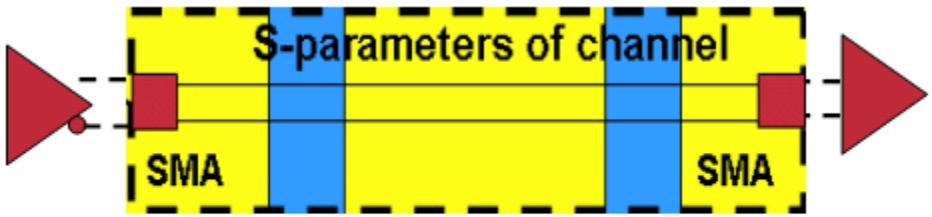
Channel S-Parameters Measurements



Agilent 8720ES 50Mz-20GHz S-Parameter VNA

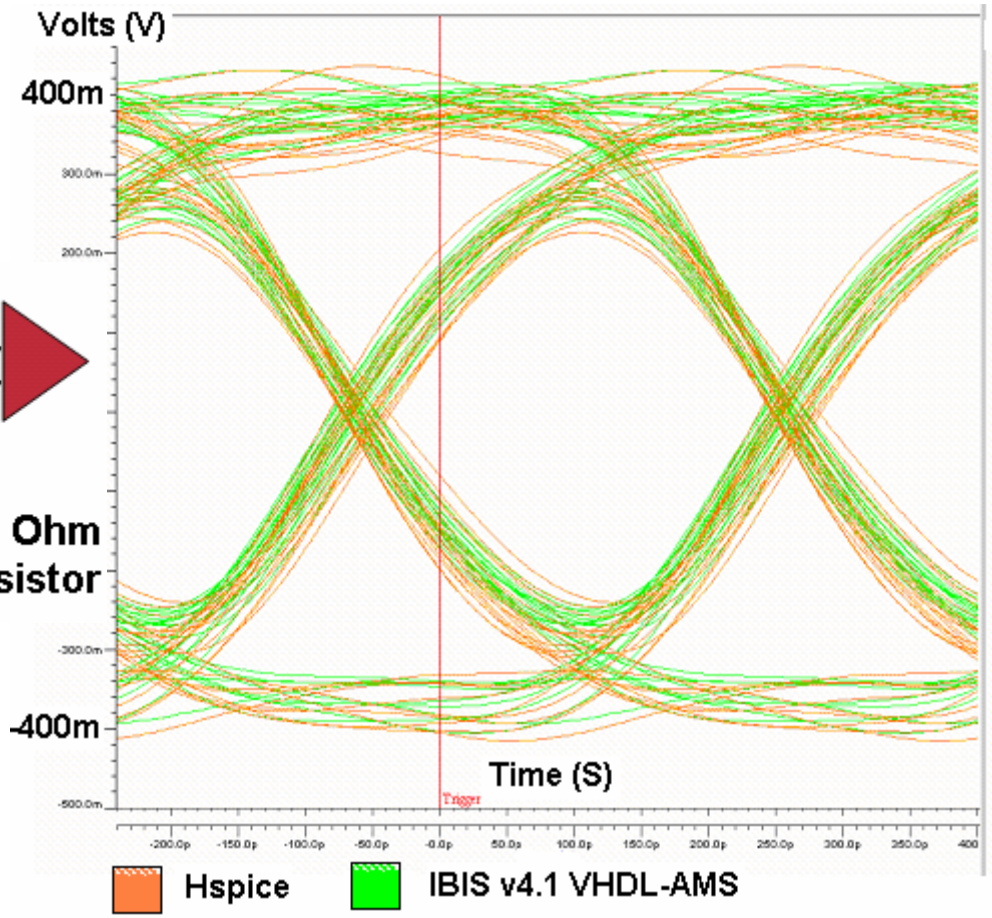


Correlation between Hspice and IBIS v4.1/VHDL-AMS using ICX

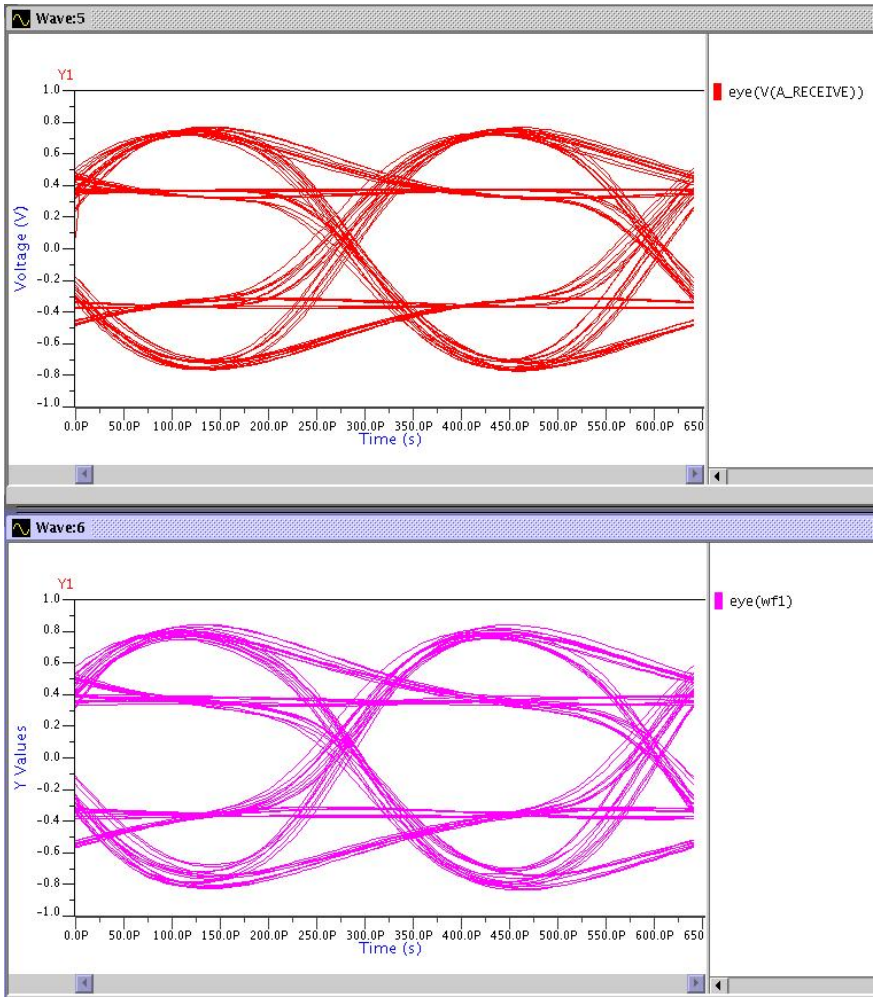


- IBIS v4.1/VHDL-AMS and
- Hspice driver models

100 Ohm resistor



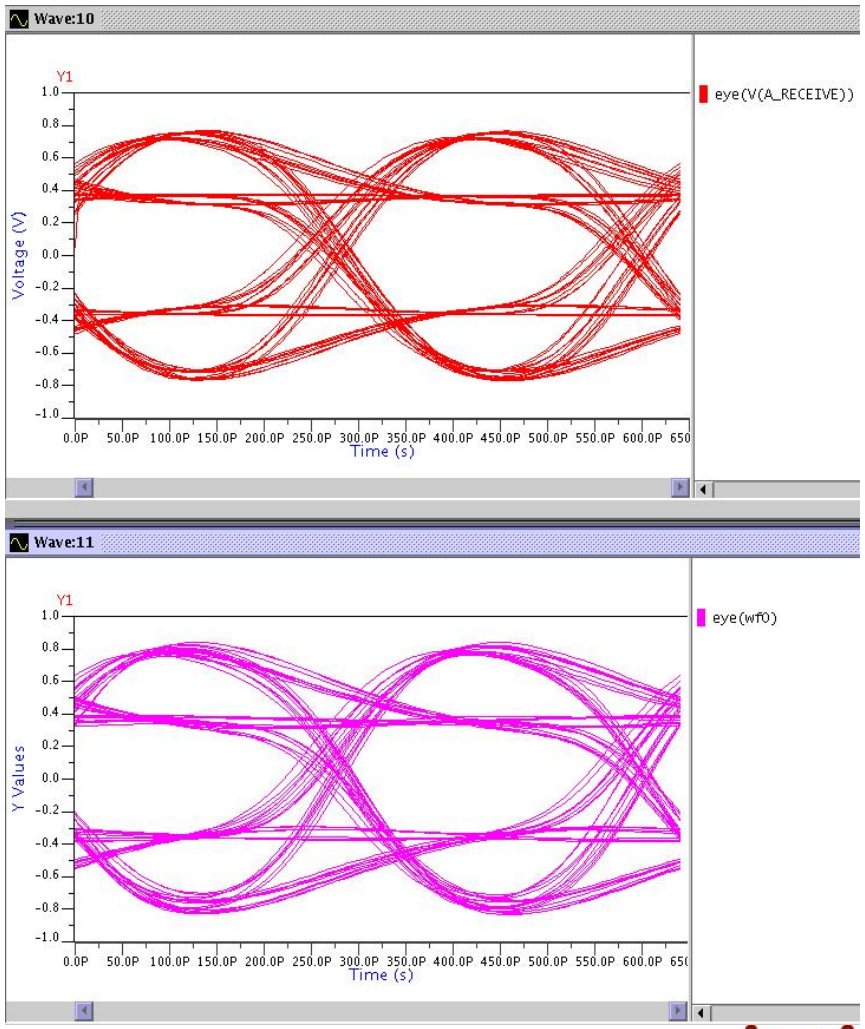
Eye pattern correlation with PE = 0



VHDL-AMS
Jitter = 60.27ps

HSPICE
Jitter = 61.08ps

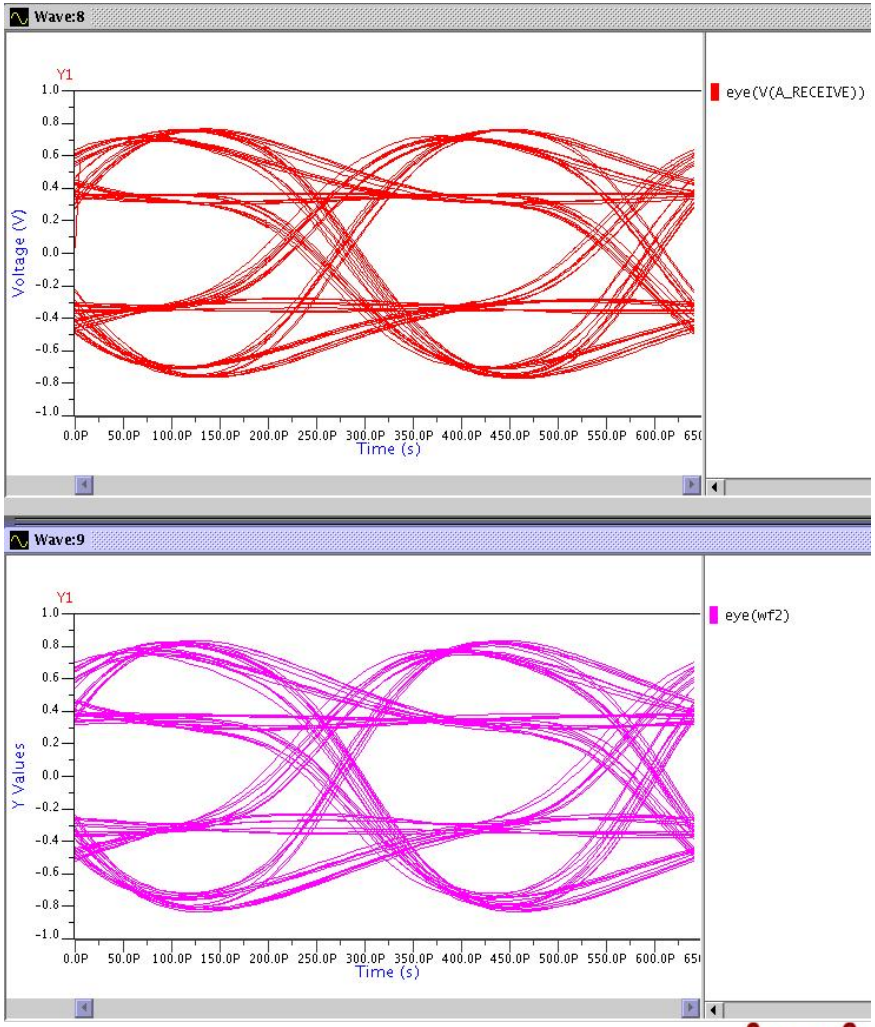
Eye pattern correlation with PE = 3



VHDL-AMS
Jitter = 77.83ps

HSPICE
Jitter = 76.60ps

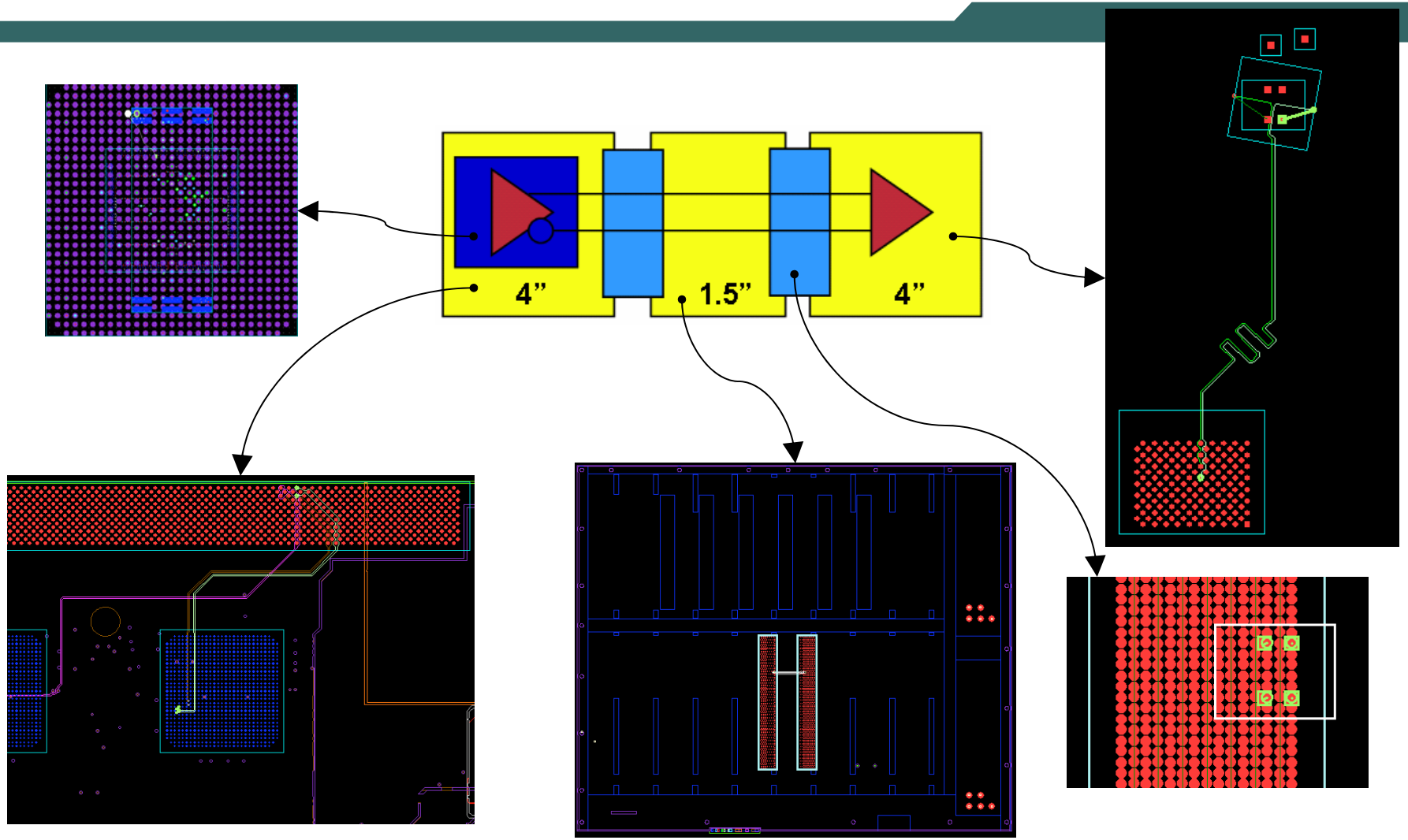
Eye pattern correlation with PE = 7



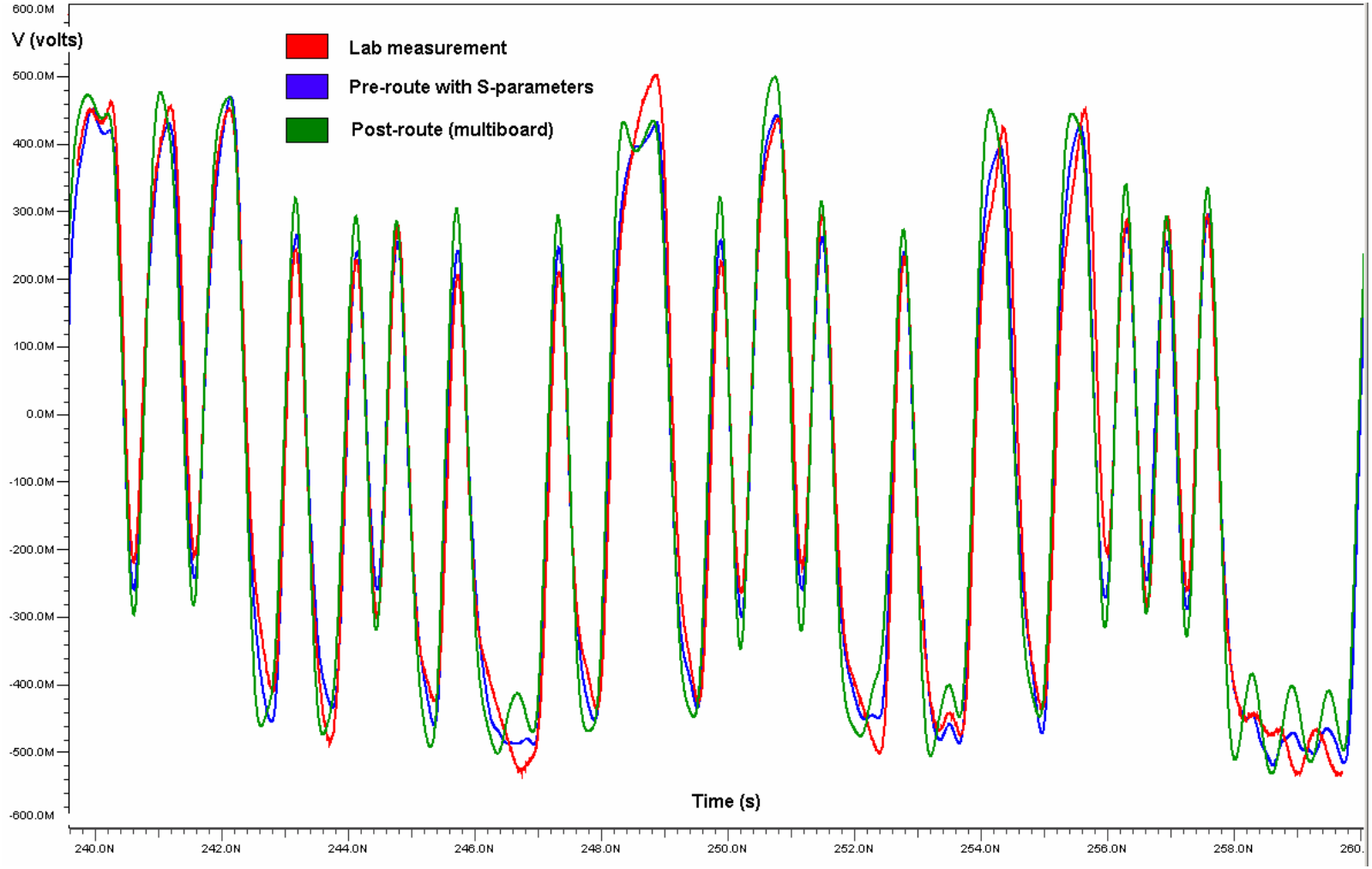
VHDL-AMS
Jitter = 108.34ps

HSPICE
Jitter = 108.85ps

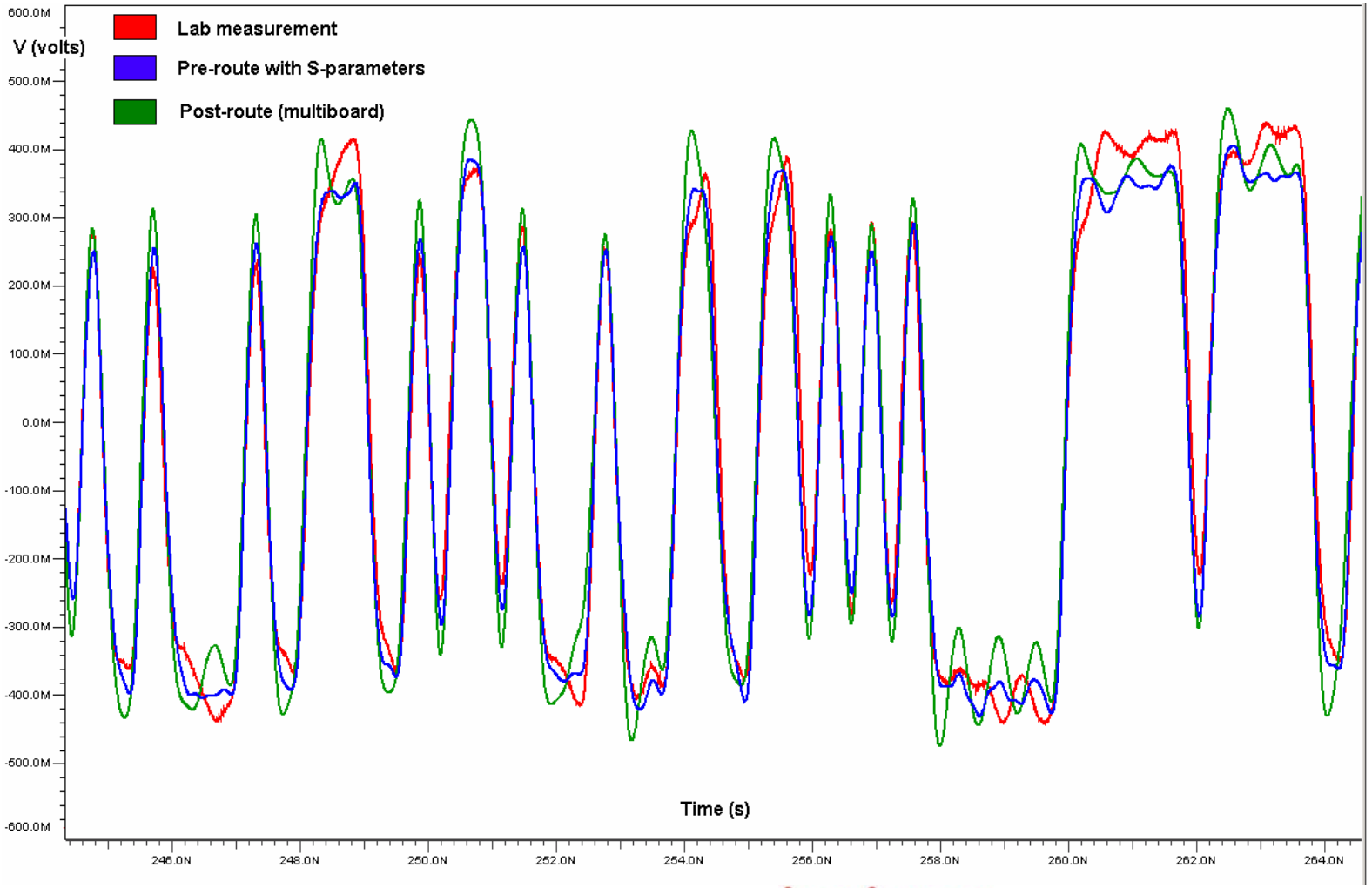
Multi-Board Verification with ISMB



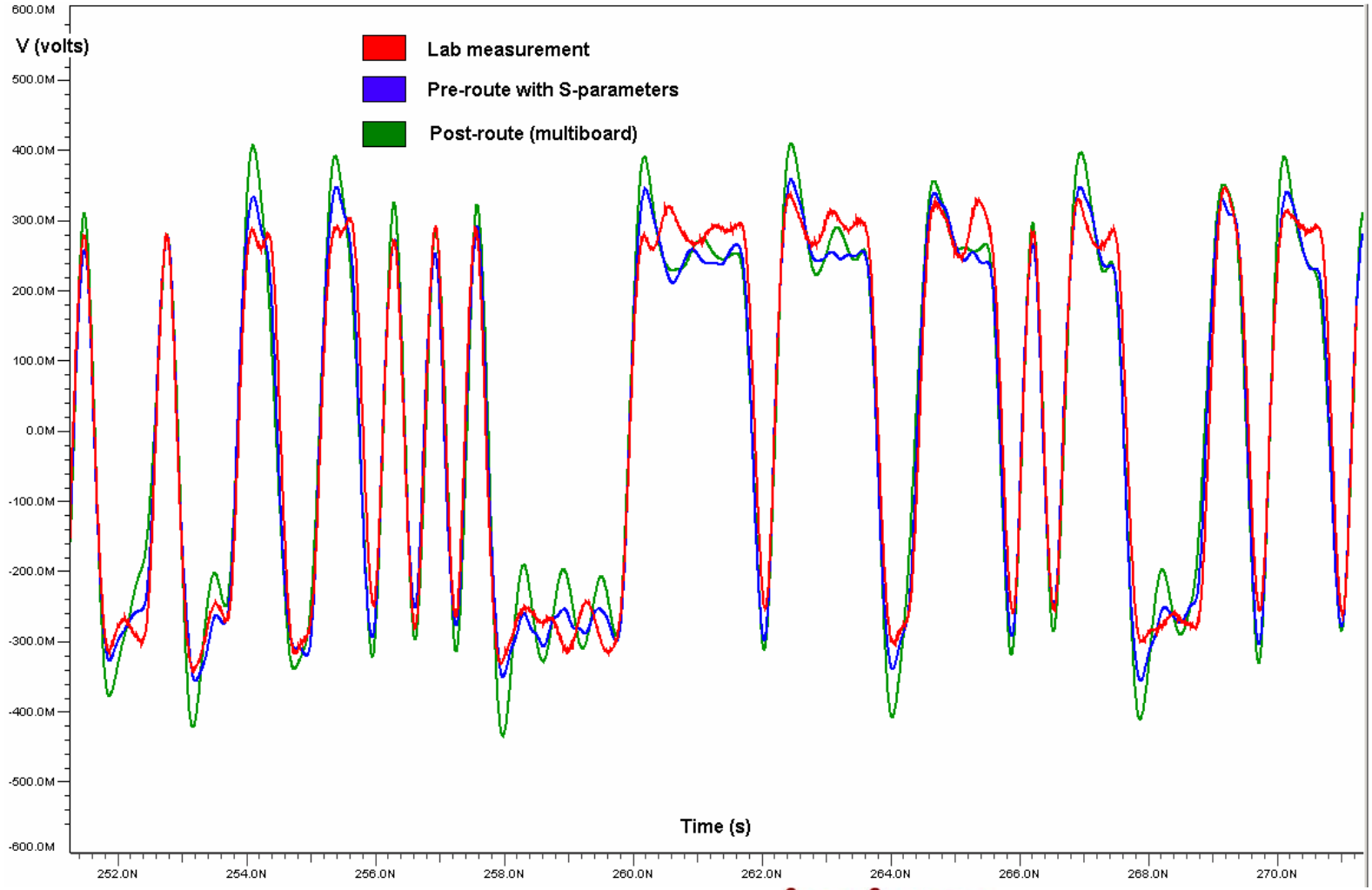
Correlation with PE=0



Correlation with PE=3



Correlation with PE=7



Performance Results

Preroute Simulation of 300ns (960 bits)

- **IBIS v4.1/VHDL-AMS Driver & 100 ohm termination resistor simulated for 23 seconds (average of 4 simulation runs)**
- **Hspice Driver & 100 ohm termination resistor simulated for 54.08 minutes (average of 4 simulation runs)**
- **141x performance improvement of IBIS v4.1/VHDL-AMS versus Hspice**

although no formal benchmarking was done.

Increasing the number of Spice elements (connector, receiver model, etc.) slows down performance. Much higher performance improvements were obtained

Platform: IBM Thinkpad with Pentium 4 @ 2 GHz – 1 GB RAM
Win XP, ICX Ver 3.4.01 Hspice Ver W-2004.09

Conclusions

- Good correlations between lab measurements and post-layout simulations
- Post layout multi-gigabit simulation is possible using IBIS v4.1/VHDL-AMS and ICX
- Easy conversion to ICX format, ICX is easy to use
- Fast simulations
- Opens the door for automation
- More work is needed on the methodology

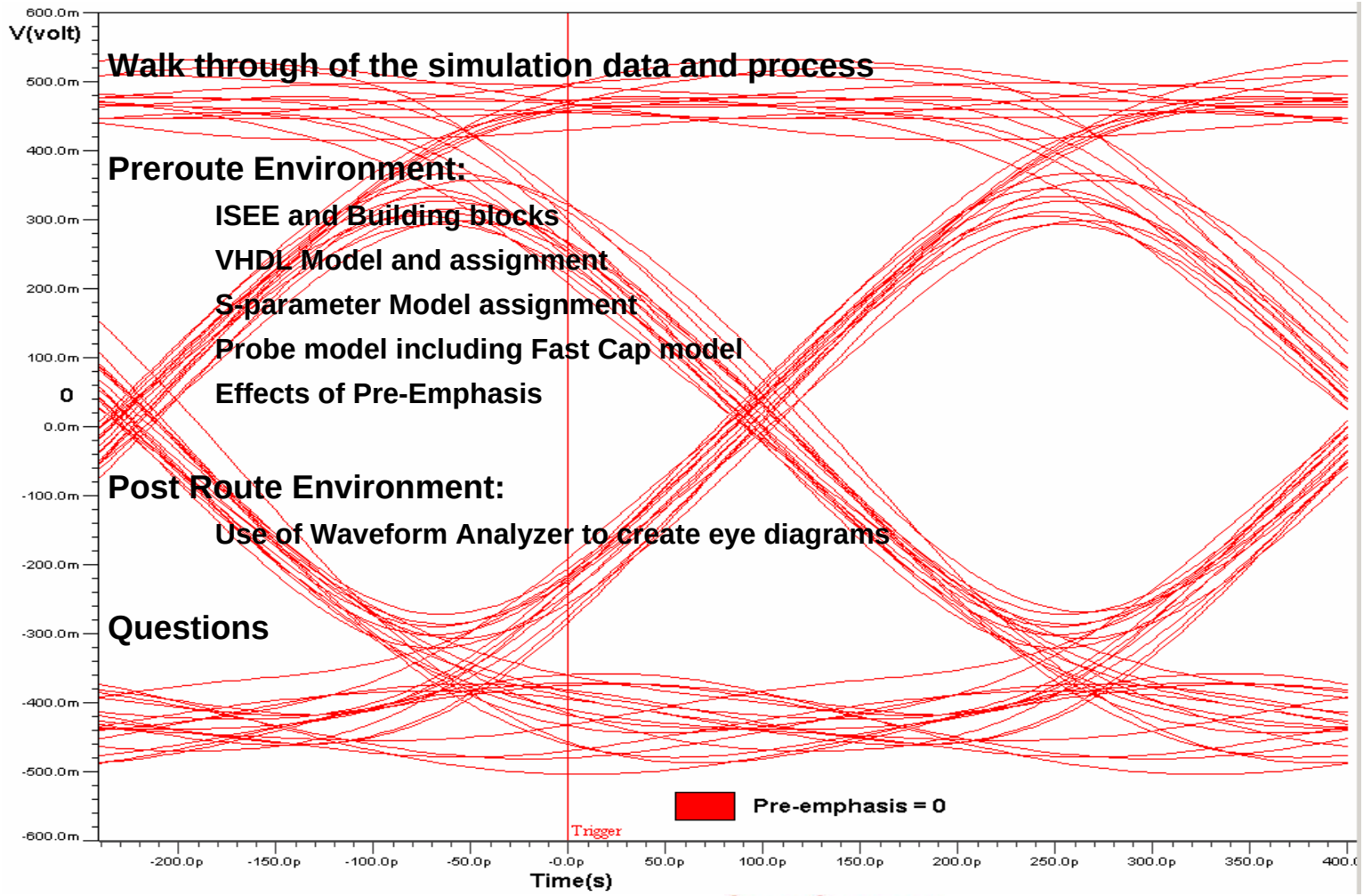
What's Next

- **There are many complex features that need to be modeled:**
  - **DFE (Decision Feedback Eq)**
  - **FFE (Forward Feedback Eq) – Multi-tap**
  - **CDR (Clock Data Recovery)**
  - **Higher Data rate and correlations**
  - **Target BER testing**
  - **Compliancy to specifications**

Part – II

Ian Dodd

Methodology Walkthrough



Walk through of the simulation data and process

Preroute Environment:

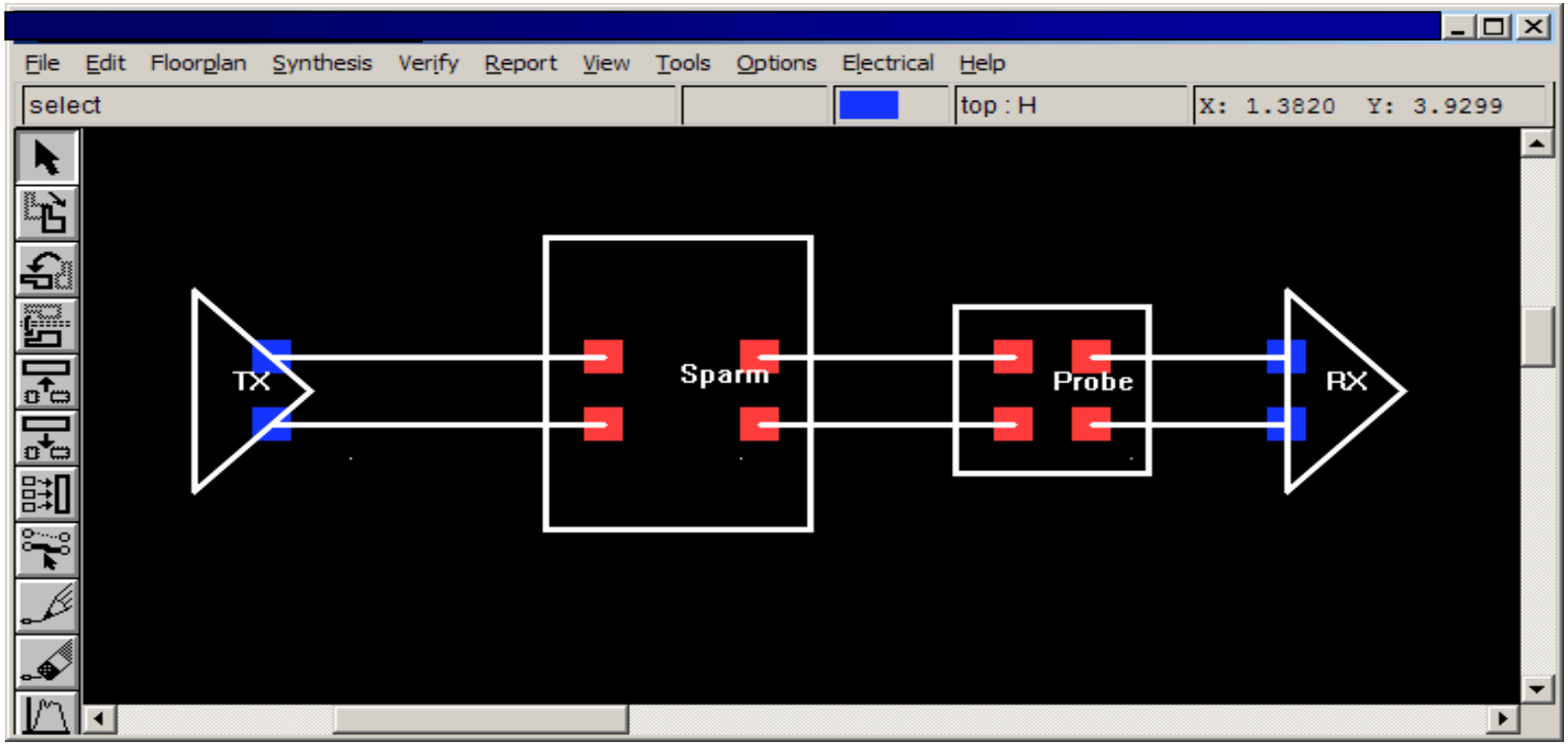
- ISEE and Building blocks
- VHDL Model and assignment
- S-parameter Model assignment
- Probe model including Fast Cap model
- Effects of Pre-Emphasis

Post Route Environment:

- Use of Waveform Analyzer to create eye diagrams

Questions

Pre-Route Analysis Using IS Electrical Editor



VHDL-AMS Model
Derived from Encrypted Hspice

S-Parameter Channel Model
Derived from Lab Measurements

VHDL-AMS Model

IBIS v4.1 Calling a VHDL-AMS Model

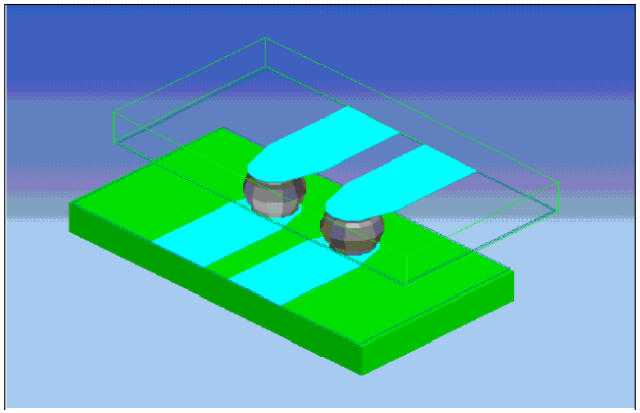

```
[Ibis Ver]              4.1
[File Name]             acap100n.ibs
[File Rev]              0.5
[Notes]
[Date] Fri Feb 25 15:41:42 2005
[Component]             acap100n
[Manufacturer]          Mentor Graphics ICX 3.4.01
[Package]
R_pkg 15.000000m        10.000000m          20.000000m
L_pkg 2.000000nH        2.000000nH          2.000000nH
C_pkg 0.100000pF        0.090000pF          0.110000pF
[Pin]  signal_name      model_name          R_pin L_pin C_pin
1      CAP1                                 NC
2      CAP2                                 NC
|
[Series Pin Mapping]    pin_2    model_name    function_table_group
1      2                dummy

| Calls to external circuits or [model]s
[circuit call] C_100n
port_map N1 1
port_map N2 2
[end circuit call]
|
[Model]                                 dummy
Model_type              Series
Polarity                Non-Inverting
Enable                                  Active-High
|                       typ                           min             max
C_comp                                  0.0F          NA              NA
                                        typ           min             max
[voltage range]         1.000000V       1.000000V     1.000000V
|
[R series]                              10.000000M    10.000000M      10.000000M
|
| Calling an external model in SPICE or VHDL-AMS language.
[External Circuit] C_100n
language VHDL-AMS
corner typ ../../VHDL-AMS/source/acap100n.vhd acap100n(adaptive)
ports n1 n2
[End External Circuit]
[End]
```

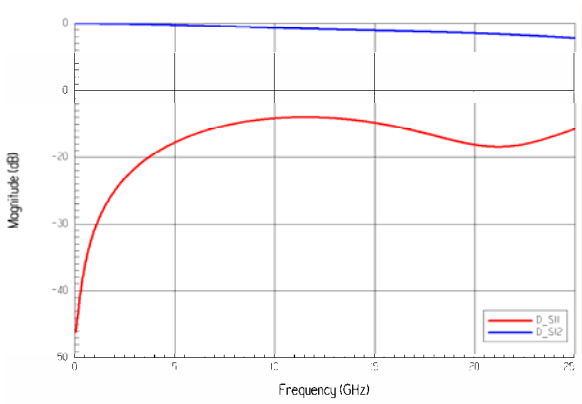
```
| Calls to external circuits or [model]s
[circuit call] C_100n
port_map N1 1
port_map N2 2
[end circuit call]
```

```
| Calling an external model in SPICE or VHDL-AMS
language.
[External Circuit] C_100n
language VHDL-AMS
corner typ ../../VHDL-AMS/source/acap100n.vhd
acap100n(adaptive)
ports n1 n2
[End External Circuit]
```

What Are “S-parameters”

- **A set of parameters describing the scattering and reflection of traveling waves when a network is inserted into a transmission line.**
- **For a two port network, (assume use of matched loads)**
  - **S11 is the reflection coefficient of the input**
  - **S22 is the reflection coefficient of the output**
  - **S21 is the forward transmission gain**
  - **S12 is the reverse transmission gain (from output to input).**





Differential HFSS model and the frequency response from Ansoft Workshop

Example S-Parameter File

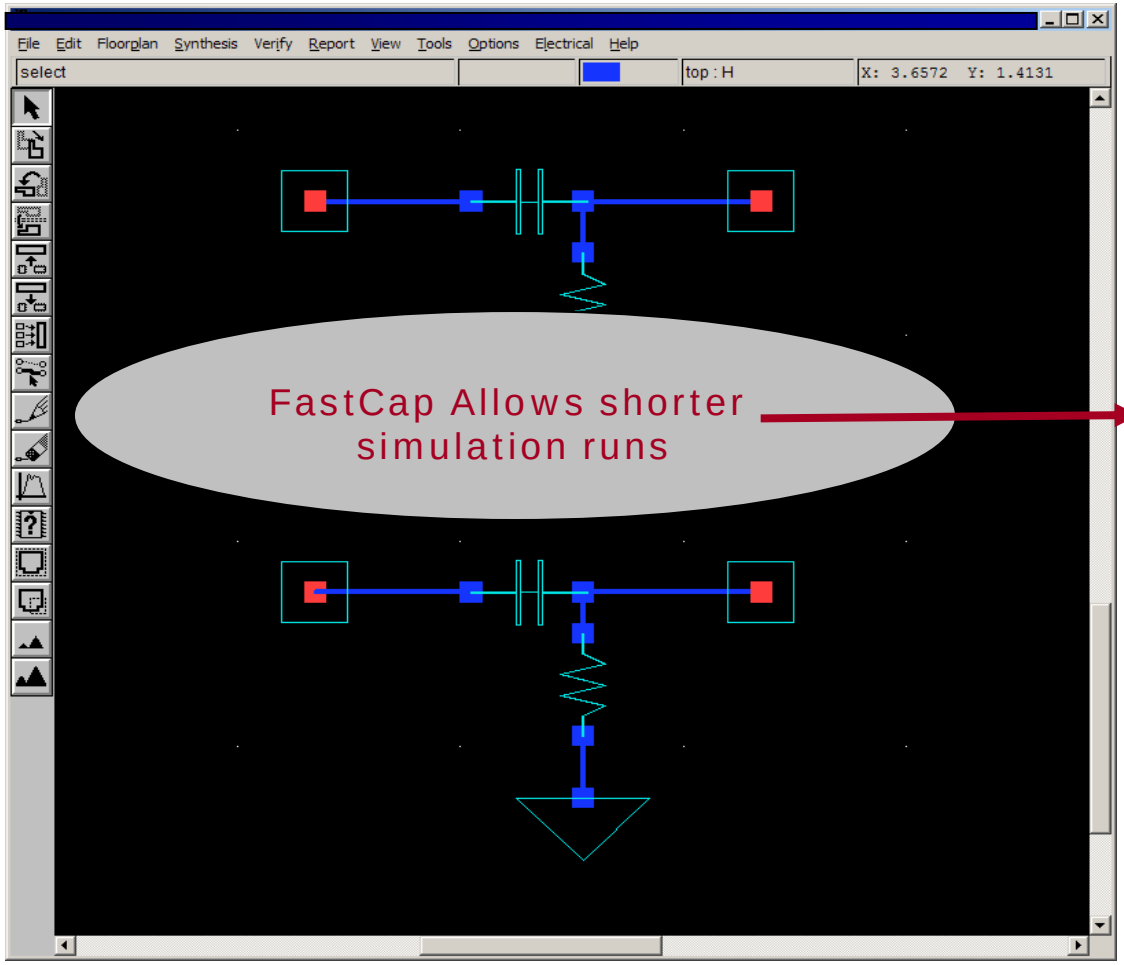

```
! Usage in a simulation setup
!    touchstone file
! --------------------------
# hz S ma R 50
        1      0.0            0.0          0.0            0.0          0.9999
               0.0            0.0          0.0            0.0          0.0
               0.9999         0.0          0.0            0.0          0.0
               0.0            0.0          0.9999         0.0          0.0

    100000000    0.0154476809     82.2545777     0.0131366321     88.624048     0.999845152
          0.0129659314     77.7358032     0.0155877494     85.9614378     0.00452329414
           0.999554273    -3.45502166    0.00449924533    -99.1371049     0.0154588225
          0.00458916699    -84.9518806     0.999326297    -3.75124983     0.0129114688

    134673370    0.020763747     81.8242185     0.0176610608     86.1400779     0.999667003
          0.0173633274     78.3262784     0.0209745823     84.0292102     0.00608486166
           0.999384822    -4.6524466    0.00605104768    -100.477963     0.0207717652
          0.00612909172    -90.0717476     0.999177303    -5.05157111     0.0173764593

    169346740    0.0260669868     80.9953092     0.0221724583     84.0108839     0.999439636
          0.0217576711     78.0718736     0.0263467906     82.1895232     0.00764496637
           0.999176617    -5.84934459    0.00759958984    -102.13755     0.0260720781
          0.00768046846    -94.0003469     0.998979744    -6.35152733     0.0218307243

    204020110    0.0313528888     79.9682583     0.0266660477     82.0586593     0.999161512
          0.0261400592     77.3946994     0.0317011432     80.3954462     0.00920216095
           0.998914082    -7.04566468    0.00914371473    -103.953986     0.0313551214
          0.00923759438    -97.3229465     0.99873206    -7.65111334     0.0262718076
```

IBIS Calling an S-Parameter Model


```
[IBIS Ver]     4.1
[File name]    sParConn.ibs[File Rev]     1.0
[Date]         12 NOV 04
[Source]       None.
[Notes]        calls a SPICE subcircuit that
               instantiates an S-parmeter set of a connector.
|
[Component]    SConn
[Manufacturer] UNKNOWN
|
[Package]
|              typ          min          max
R_pkg          0            NA           NA
L_pkg          0            NA           NA
C_pkg          1pf          1pf          1pf
|
[Pin]  signal_name   model_name    R_pin  L_pin  C_pin
1      dcp           NC            NA     NA     NA
2      dcn           NC            NA     NA     NA
15     bpn           NC            NA     NA     NA
16     bpp           NC            NA     NA     NA
|
[Diff Pin] inv_pin vdiff tdelay_typ tdelay_min tdelay_max
  1       2      0       0
  16      15     0       0
```

```
[Series Pin Mapping] pin_2 model_name
1 16  R_1G_ohm
2 15  R_1G_ohm
|
[circuit call] hsd5ab
port_map 101 1
port_map 102 2
port_map 2402 15
port_map 2401 16
[end circuit call]

[external circuit] hsd5ab
language  SPICE
corner typ  sParamConn.cir  SPARAMCONN
ports 101 102 2401 2402
[end external circuit]
|
```

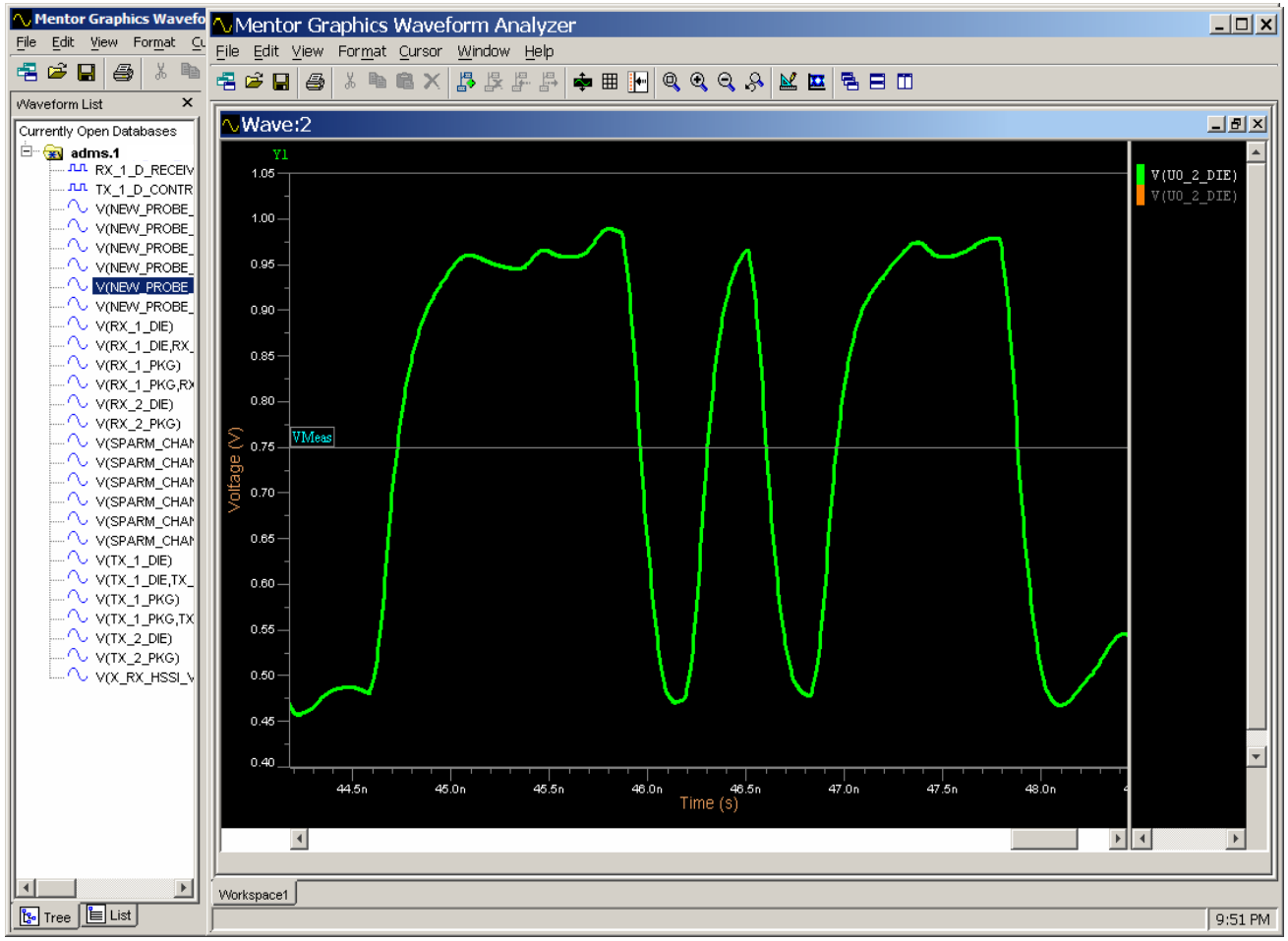
Spice and VHDL-AMS Probe Model




```
* SPICE IMPLEMENTATION
.SUBCKT recv_probe4port   in_pos in_neg pos1 neg1

c1 in_pos  pos1  100p
r1 pos1 0  50
c2 in_neg  neg1  100p
r2  neg1  0 50

.ENDS
```

```
VHDL-AMS Implementation
entity cDiffAutoFastSettling is
  generic (
    cap     : capacitance := 100.0e-9 );   -- Nominal capacitance [F]

  port (
    terminal p1, p2, p3, p4 : electrical);

end entity cDiffAutoFastSettling;

architecture adaptive of cDiffAutoFastSettling is
  quantity v across i through p1 to p2;
  quantity v34 across i34 through p3 to p4;
  signal cap_signal : capacitance := cap/1000.0;
begin
```

Pre-Route Waveform
De-Emphasis = 0

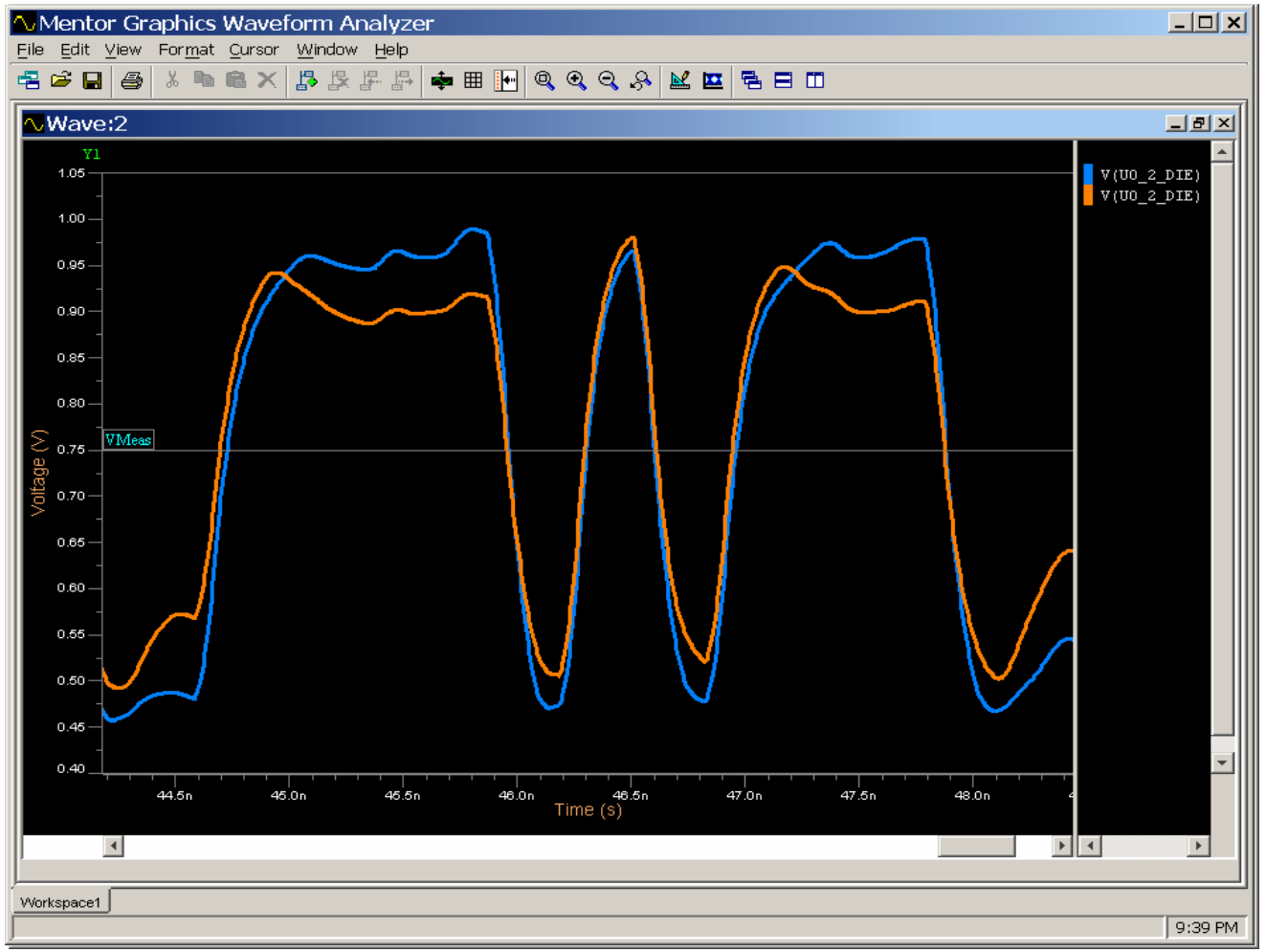


Passing Parameters to VHDL-AMS

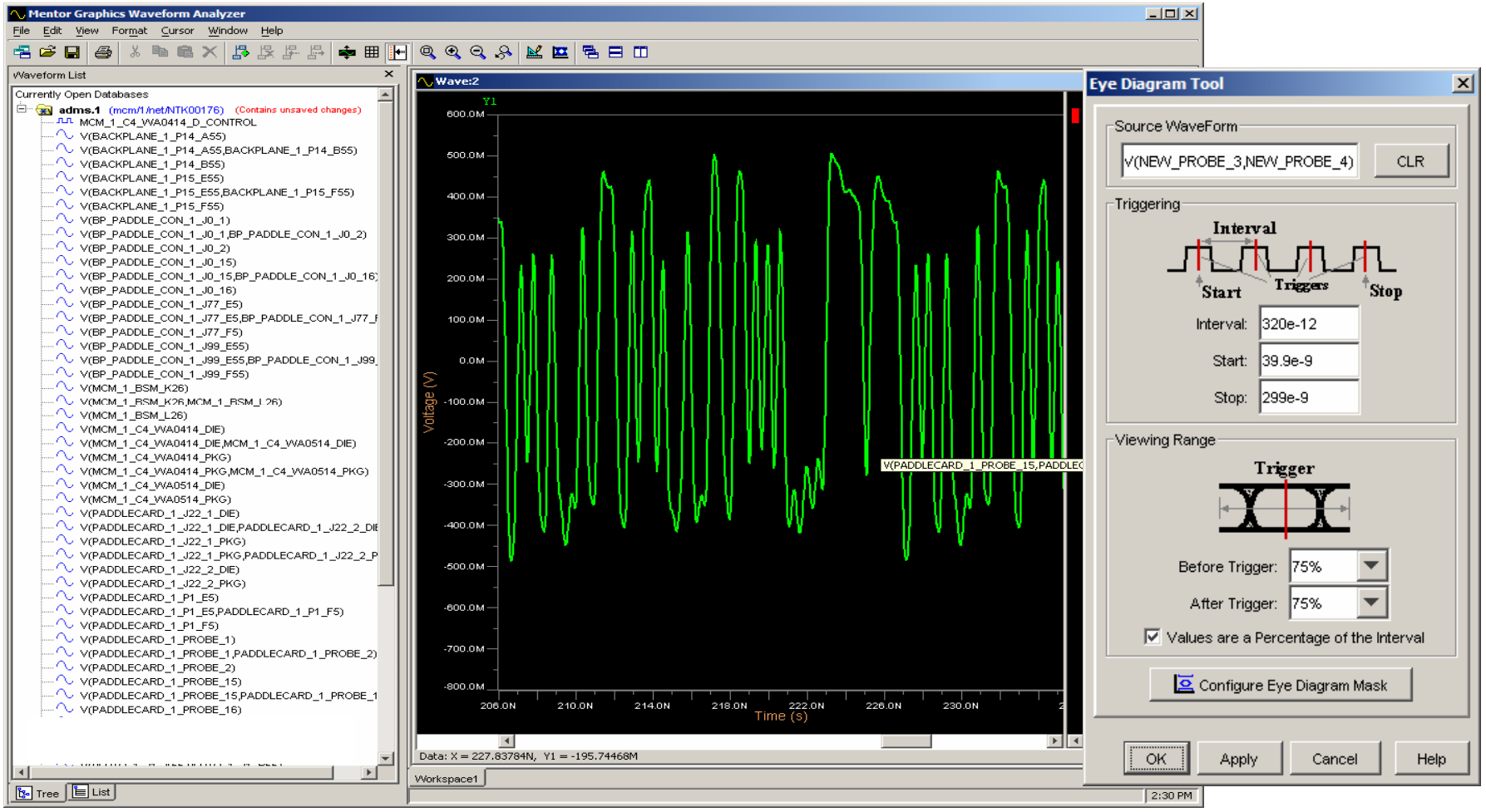
* Global parameter file from ICX
* These parameters set the amplitude
* and Pre-Emphasis levels

```
.TEMP 55
* UI 320
.PARAM UI=320.0p
* amp
.PARAM amp=15
* pre-emphasis
*.PARAM  pemph=3
.PARAM  pemph=7
*.PARAM  pemph=0
```

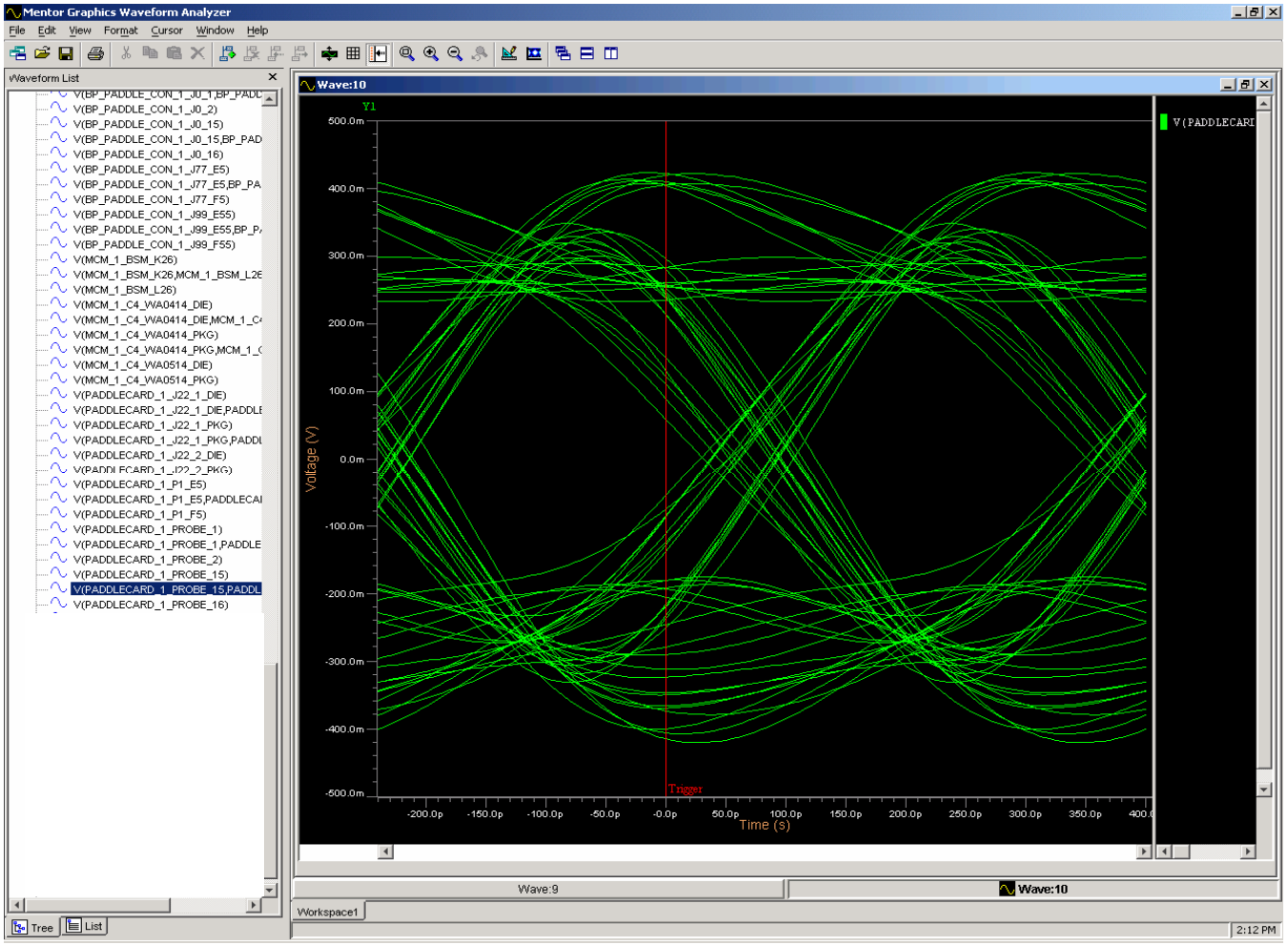
De-Emphasis = 7 at Driver



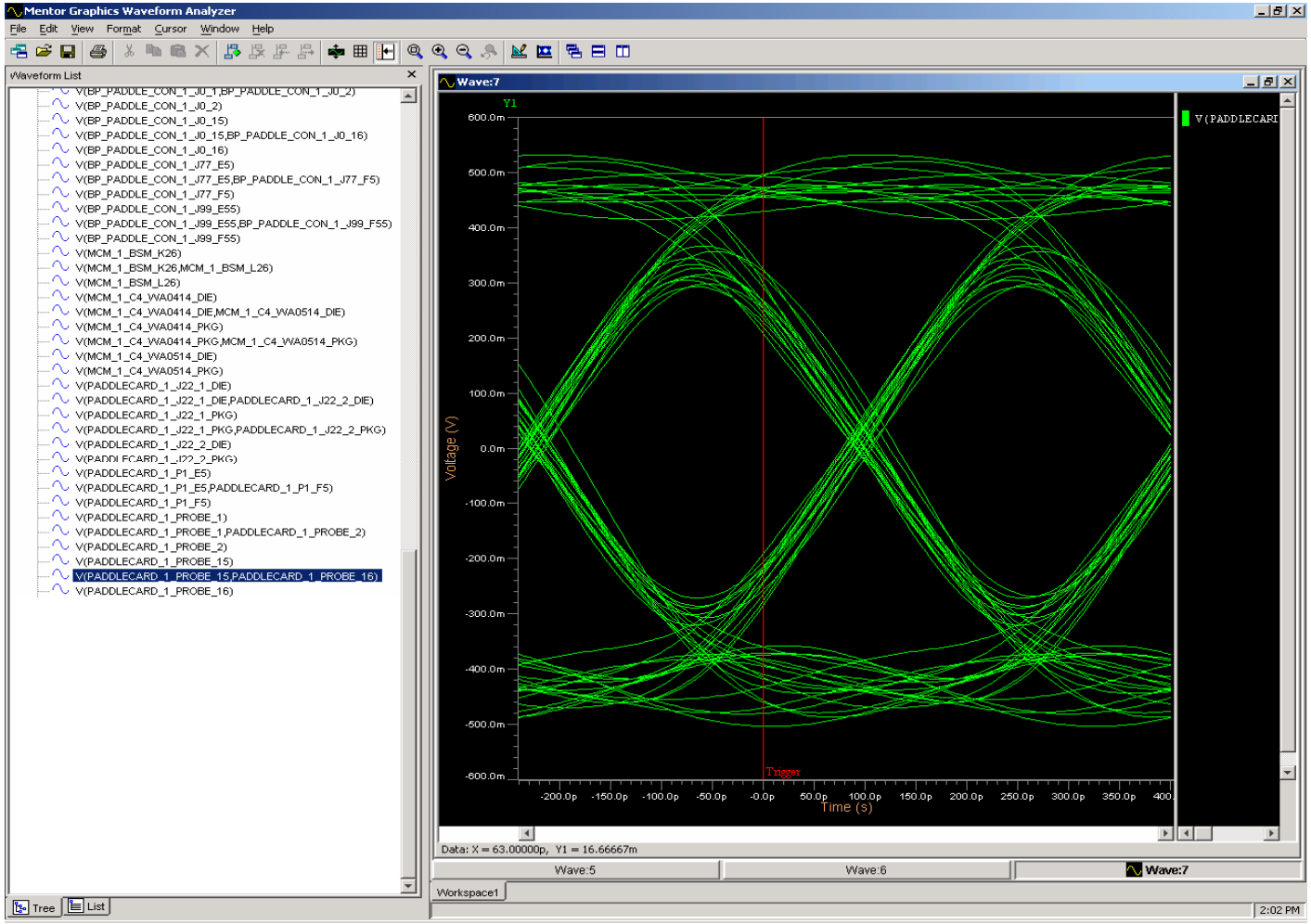
Post Route Eye Diagrams



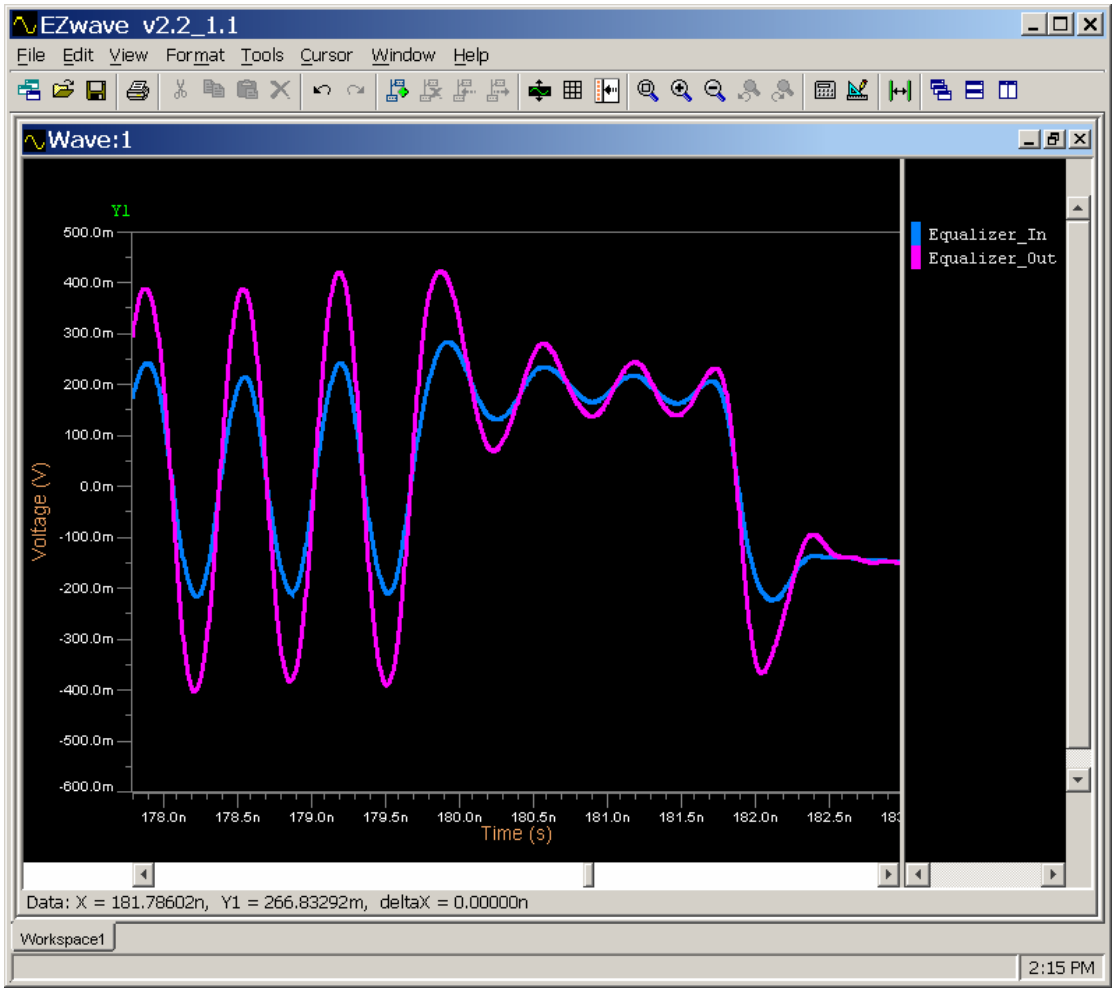
Post-Route Eye Diagram
De-Emphasis = 7



Post-Route Eye Diagram
De-Emphasis = 0



Results of Equalization



Converting Hspice model into VHDL-AMS

Ashenden et al, The System Designers Guide to VHDL-AMS. This comes with examples for use in educational (free download) version of Mentor's SystemVision.

Fitzpatrick and Miller, Analog Behavioral Modeling with the Verilog-A Language, comes with CD containing examples and software.

Information sources include the VHDL and Verilog AMS web sites (http://www.eda.org/), as well as the EDA tool vendor sites (Mentor, Cadence, etc.).”

Dr. Lynne Green, “Looking for information on AMS Modeling” SI-List email, 2/23/2005

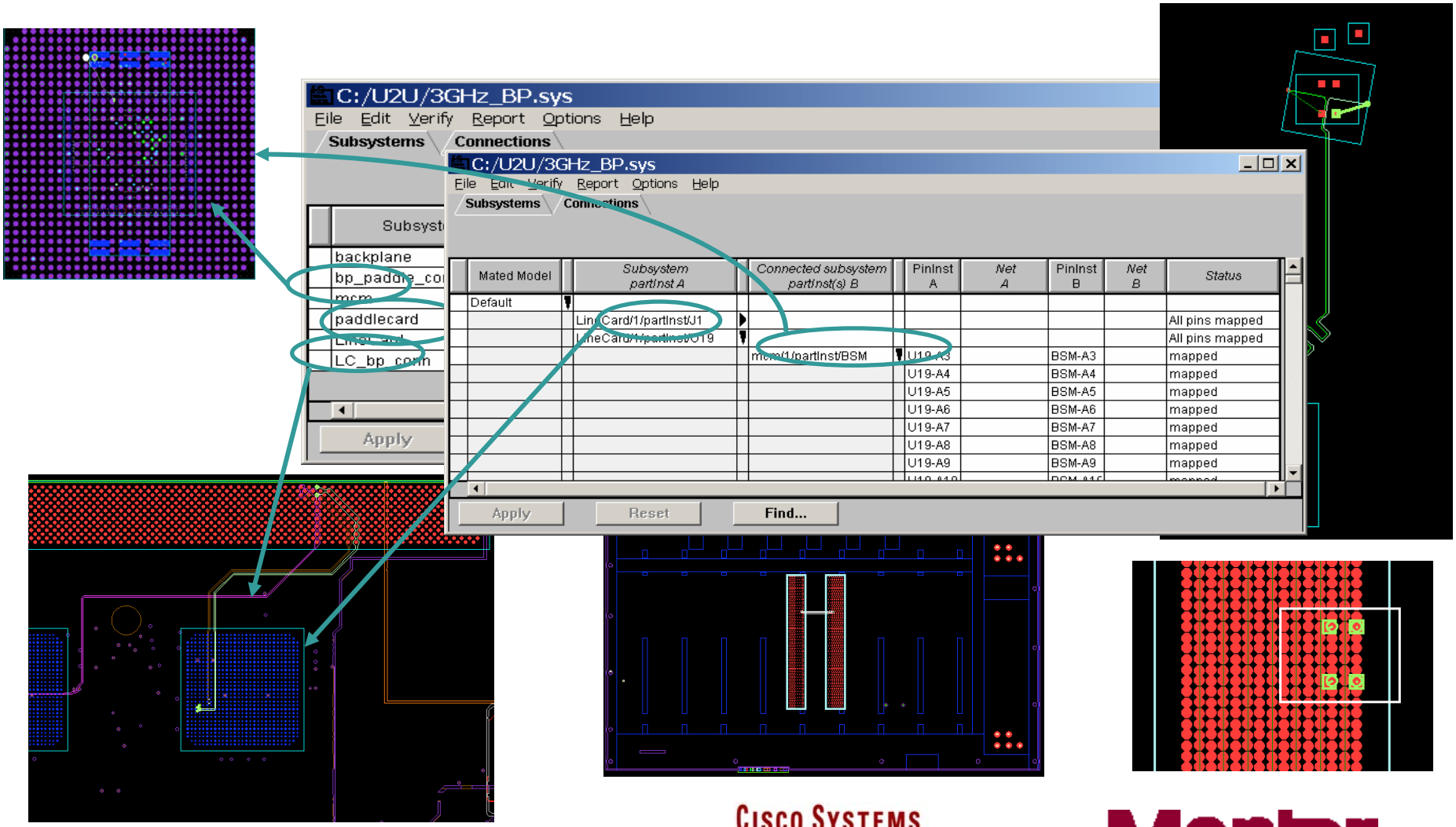
References

- **IBIS website: http://www.eigroup.org/IBIS/Default.htm**
- **IBISv4.1 spec: http://eda.org/pub/ibis/ver4.1/**
- **VHDL-AMS website: http://www.eda.org/vhdl-ams**
- **Mentor website: http://www.mentor.com**
- **“Utilizing TDR and VNA Data to Develop 4-Port Frequency Dependent Models” Jim Mayrand, Mike Resso, Dima Smolyansky, DesignCon 2004**

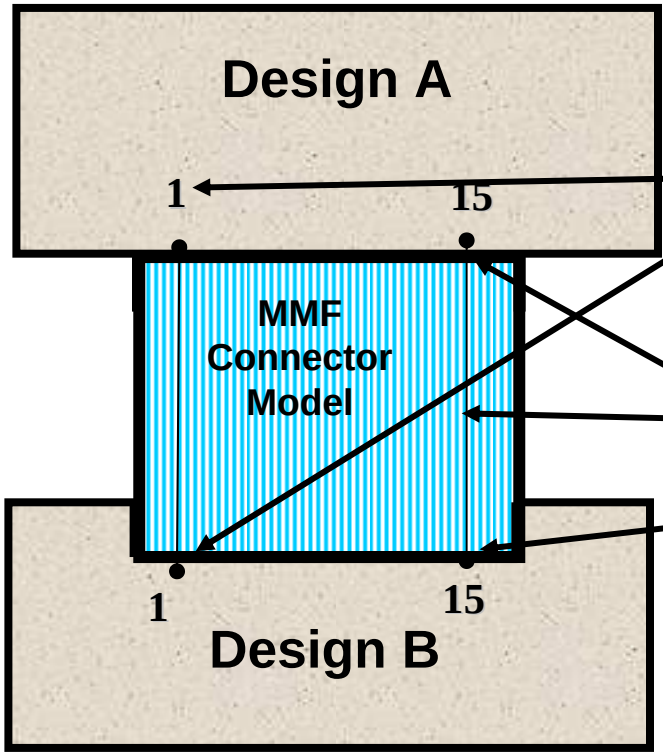
Question and Answer

Backup Slides

Multi-Board Verification with ISMB

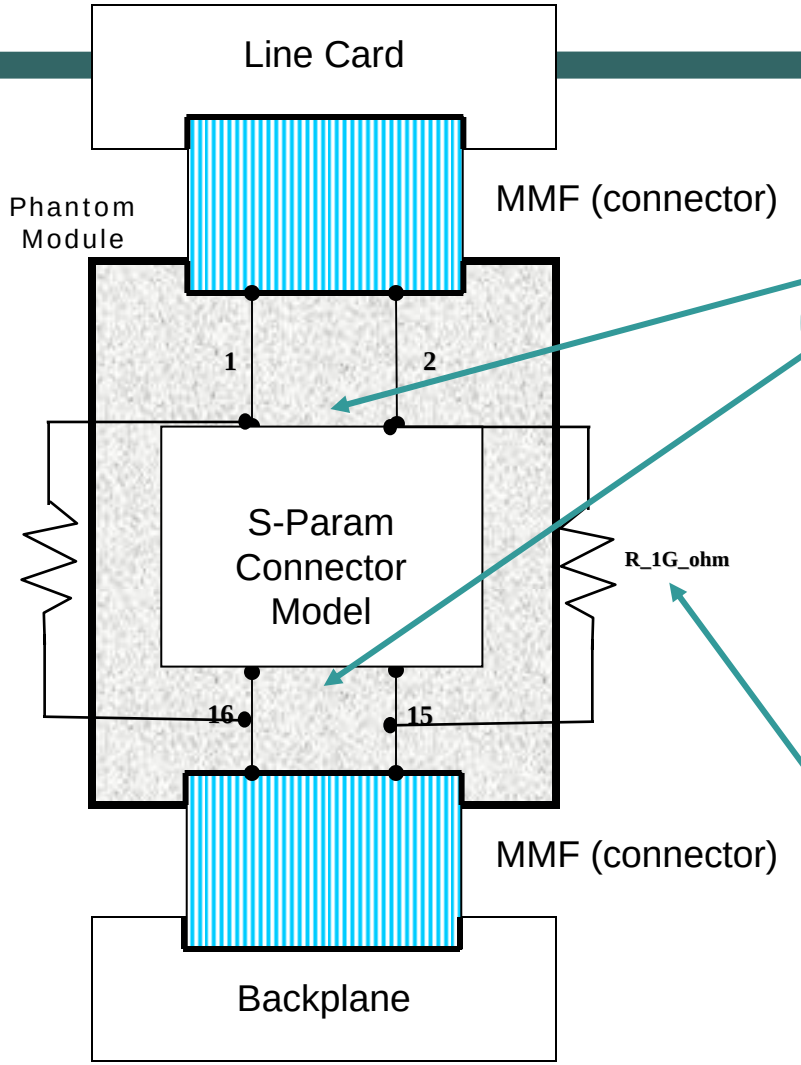


Typical ISMB Connector Model




```
CPad_1 = 1.1p
CPad_2 = 0.6p
[Manufacturer] ICXEngineering
[Number of Sections] 3
[Number of Pins] 7
[Pin Numbers]
1               1
Len=0 R=1m  L=7.1nH  C=1.2pF /  | lumped pin parasitic adjacent to A1
Len=39.37 R=22m L=11.7nH  C=2.77p /  | 39.37" of 65 ohm cable @ 180ps/in
Len=0 R=1m  L=9.75nH  C=2.31p /  | lumped parasitic of module connector

2               2
Len=0 R = 0.008 L = 7.3e-9 C = 2.7e-12 /
Len=0 R = 0.09  L = 8.3e-9 C = 3.7e-12 /
Len=0 R = 0.010 L = 6.3e-9 C = 1.2e-12 /

3               3               Len=0 R = 0.008 L = 7.3e-9 C = 2.7e-12 /
4               4               Len=0 R = 0.008 L = 7.3e-9 C = 2.7e-12 /
5               5               Len=0 R = 0.008 L = 7.3e-9 C = 2.7e-12 /
…               …               Len=0 R = 0.008 L = 7.3e-9 C = 2.7e-12 /
15              15              Len=0 R = 0.008 L = 7.3e-9 C = 2.7e-12 /

[End Connector Model]

[End]
```

ISMB Connector Workaround




```
[IBIS Ver]      4.1
[File name]     spara_LC_con_4port.ibs
[Notes]         calls a SPICE subcircuit that instantiates an S-parmeter model
|[Component]     SConn_LC_4port
|
[Pin]  signal_name   model_name    R_pin  L_pin  C_pin
1      dcp           NC            NA     NA     NA
2      dcn           NC            NA     NA     NA
15     bpn           NC            NA     NA     NA
16     bpp           NC            NA     NA     NA
|
[Diff Pin] inv_pin vdiff tdelay_typ tdelay_min tdelay_max
   1      2      0         0
   16     15     0         0
[Series Pin Mapping] pin_2    model_name      function_table_group
1 16  R_1G_ohm
2 15  R_1G_ohm
[circuit call] hsd5ab
port_map A1 1
port_map B1 2
port_map A2 16
port_map B2 15
[end circuit call]

[external circuit] hsd5ab
language  HSPICE
corner typ LCCON.cir LCCONN
ports A1 B1 A2 B2
[end external circuit]

[Model]         R_1G_ohm
Model_type      Series
Polarity        Non-Inverting
[R series]          10e9          10e9          10e9
[End]
```