Power Integrity Proposal Regarding BIRD 95

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Agenda

- Part One – Power Integrity Proposal

- Part Two - Study:
  - Is [Composite Current] good enough for improving PI/SSN simulation using IBIS?

Part One – Power Integrity Proposal

- Issues with BIRD 95
- Proposed direction

Issues with BIRD 95

Is "Pin-level" the best approach?

- Proposed additions to go under the [Model] keyword (buffer level)
- Power/ground parasitics can be different for different instantiations of the same buffer type on a component; should not really group together with the buffer model
- On-die power/ground parasitic networks are essentially a "grid", difficult/impossible to break out into individual IO-specific elements
- Is this truly scalable to multiple drivers switching?
- Does it really help answer the question of interest:
  - ***"What is the effect seen when multiple drivers on the same rail switch simultaneously?"***

Issues with BIRD 95 (cont)

[Composite Current] "messy" as defined now

- Currently defined at the [Model] level
- This current is load dependent; better approach may be to define a Pre-Driver circuit.
- Combined together with the existing IBIS buffer model
  - TV curves already "open to simulator interpretation"
  - building more on top of existing TV curve definition is problematic
- Should define the pre-driver as an independent and separate (but associated) circuit entity
  - leave existing IO structure as-is for compatibility
  - maintains consistency with what IBIS has done so far
  - pre-driver simply absent if not tied to same rail as IO buffer

Proposed Direction

- Break the Power Integrity problem up into 2 separate areas of focus
  - Power delivery
  - SSN
- Attack “top down” from [Component] level instead of “bottom up” from the [Model] level
- Use IBIS to enable the flow of required information to the SI community so they can do analysis

Power Delivery

Enable systems companies to better design their board-level Power Distribution System (PDS)

- Typically a frequency domain approach, focused on planes and caps
- Start out at the **[Component]** level
  - list out each of the power rails on the component (ex. 2.5v IO, 1.8v core, etc.)
  - provide the current profile and operating frequency for each of these rails
- This would enable SI engineers to figure out initial decoupling schemes for parts
- Could then look “across the board”, including specific stack-up and make decoupling trade-offs at the PCB level
- Can expand to the package, then to the chip level in the future
  - address different frequency bands
  - will require additional information from IC suppliers

SSN

Enable IC & systems companies to better understand and combat the effects of SSN

- Typically a time domain approach, focused on high speed signals and drivers
- Start out at the **[DC Grid]** level
  - "DC grid" defined by IO power and ground pin groups per the **[Pin Mapping]** keyword
  - specify a [Grid Model] for each unique DC grid
    - some ports on the [Grid Model] have power or ground pin names, to correspond to external power and ground pins of the [Component]
    - some ports on the [Grid Model] have signal pin names, to correspond to specific IO buffer connections
  - specify the "C_bypass" for specific DC grid pairs, for on-chip capacitance

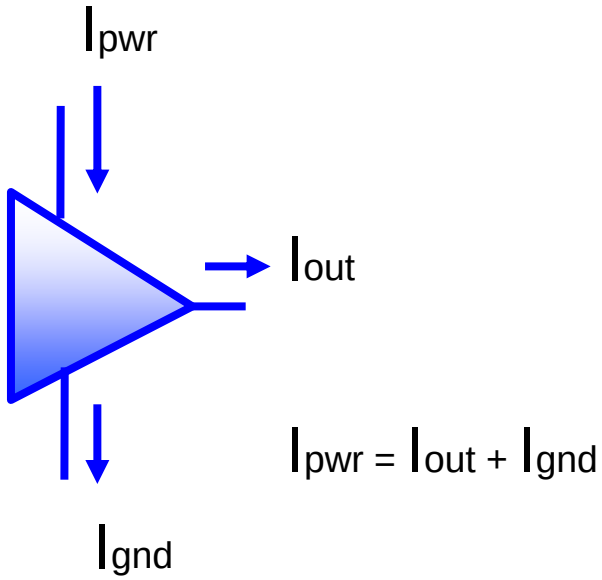
SSN (cont)

- Refine the IO model
  - specify a separate [Pre Driver Model] for each driving IO buffer
  - specify the parasitic capacitance for the specific IO model pwr-gnd feeds (if known)
- Give the **[Switching Schedule]** (or statistical probability) of how many drivers may actually switch together
- Can easily add detailed package and board-level models to analysis
- Cooperation from IC suppliers will be ***crucial*** in enabling this flow of information.
- This would provide the pieces needed to start understanding SSN effects

Part Two – Study: Is [Composite Current] good enough for improving PI/SSN simulation results using IBIS?

- Static Currents
- Is [Composite Current] good enough for PI/SSN simulations?
  - Ground Bounce Current
  - Current vs. Time Table (IT)
  - Current profile in Single (Individual) condition vs. in Multiple driver (network) condition
- Conclusions

Static Currents



Assumptions:

- Static Analysis
- Individual block
- Known I_{out}

I_{pwr} – Total current from power

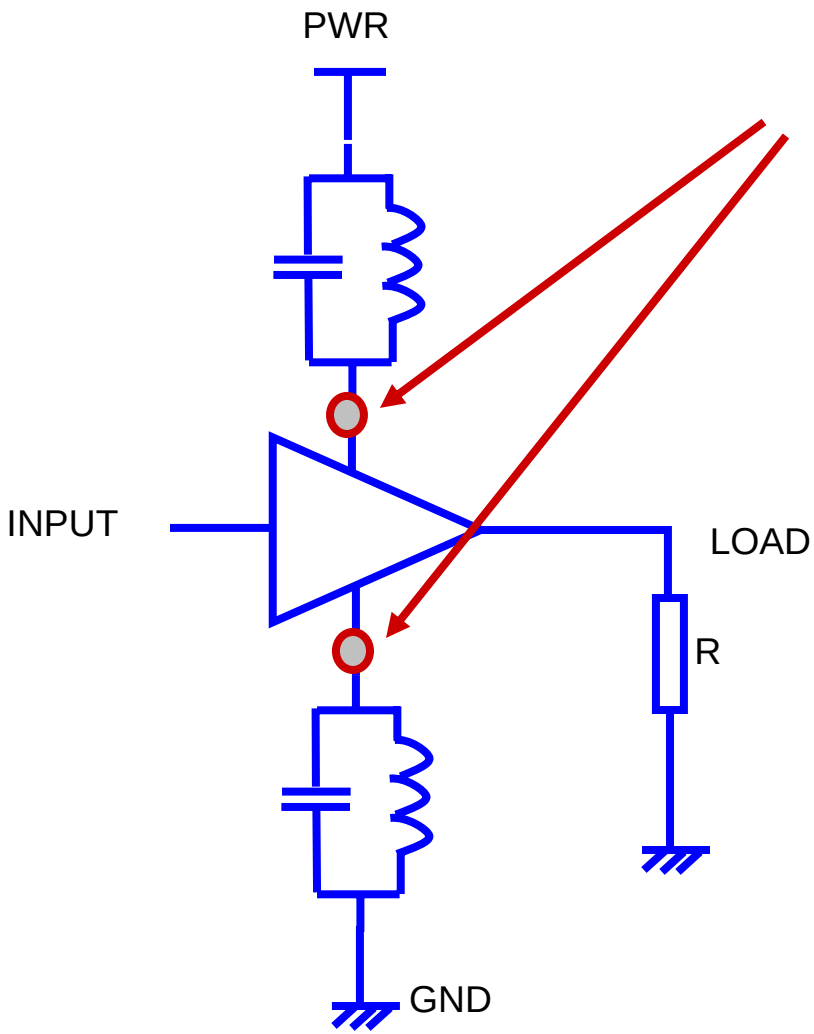
I_{gnd} – Total current to Ground

I_{out} – Current to Output

Test Setups

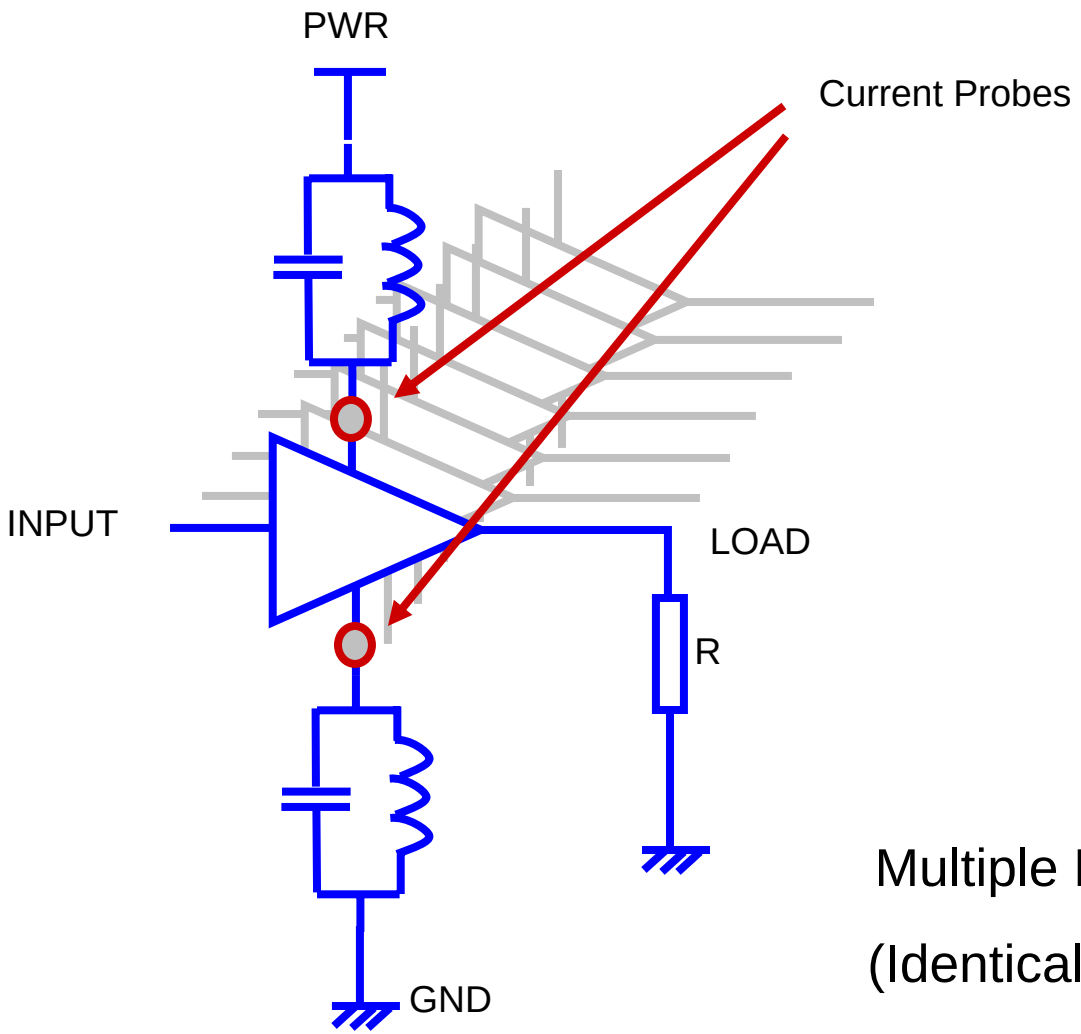
- Tests
  - HSpice simulations with transistor level models
  - Tests for a 1.8v single end, serial structure (4 cells back to back), no internal feedback
    - Single Driver alone and in a Multi-Driver Network
    - Multiple Drivers in Network
    - Loads: 50, 100 and 250 Ohm to Node 0, “Pure” Resistors
    - Stimulus: PULSE (0 1 -3.33333e-016 2.95e-009 2.98667e-009 3.71667e-009 1.33333e-008)
    - Power Parasitics: L (2nH) and C (2pF)
    - Ground Parasitics: L (2nH) and C (2pF)

Single Driver Case



Single Driver Test Circuit

Multiple Driver Case



Multiple Driver Test Circuit

(Identical 7 drivers parallel)

Ground Bounce Current

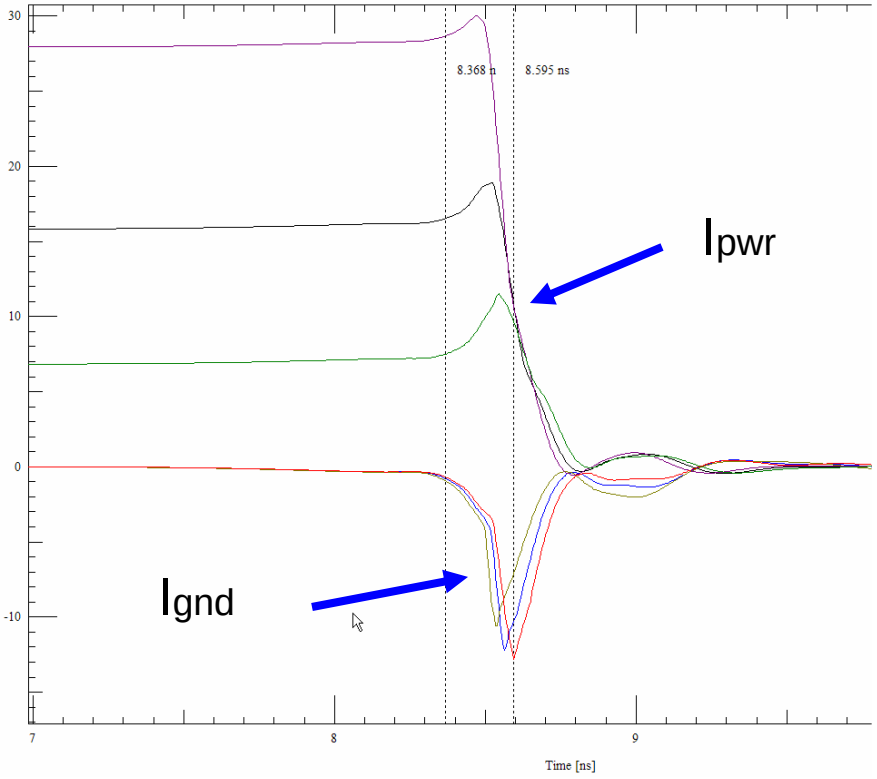
- Is Ground Bounce Current directly synchronized with Power Bounce Current?
- Does current IBIS give correct Output Current when Power/Ground current switching?
- Can we use Static assumptions to model this behavior?

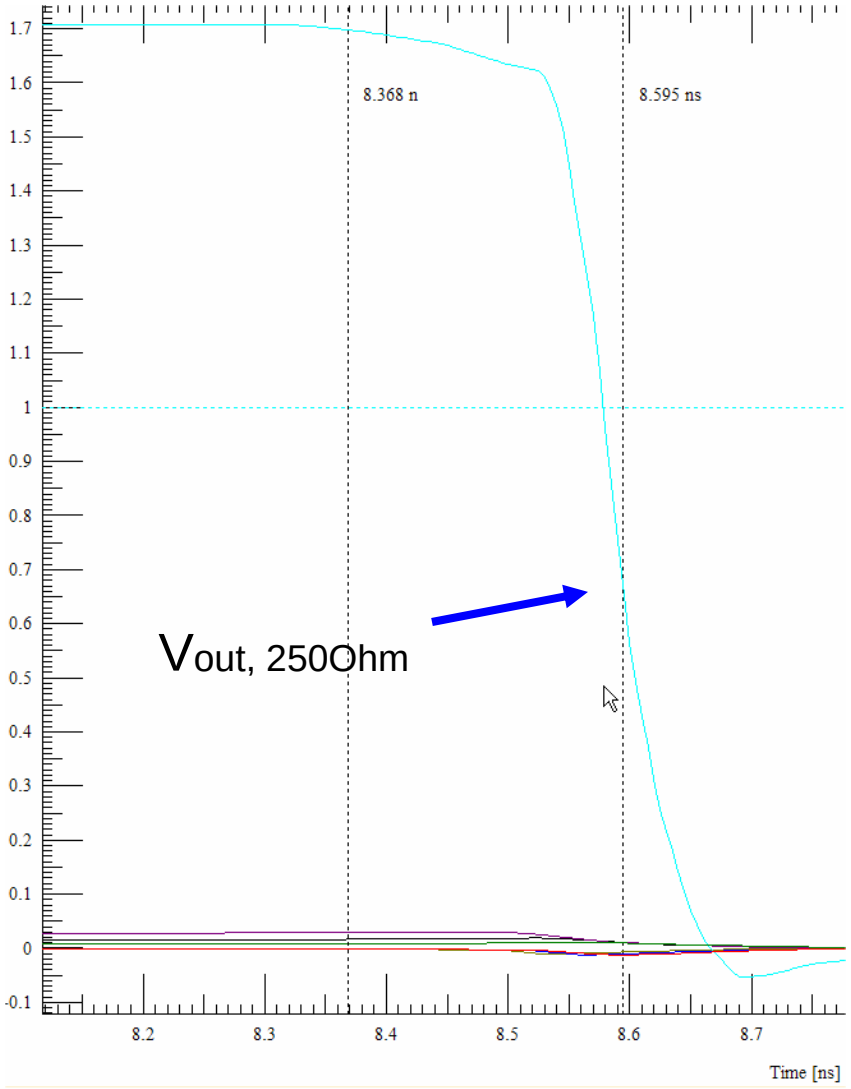
Ground Bounce Current

1 driver active in the 7-driver network

Falling edge, 50, 100, 250 Ohm loads

(Waveform captured at Active Driver)





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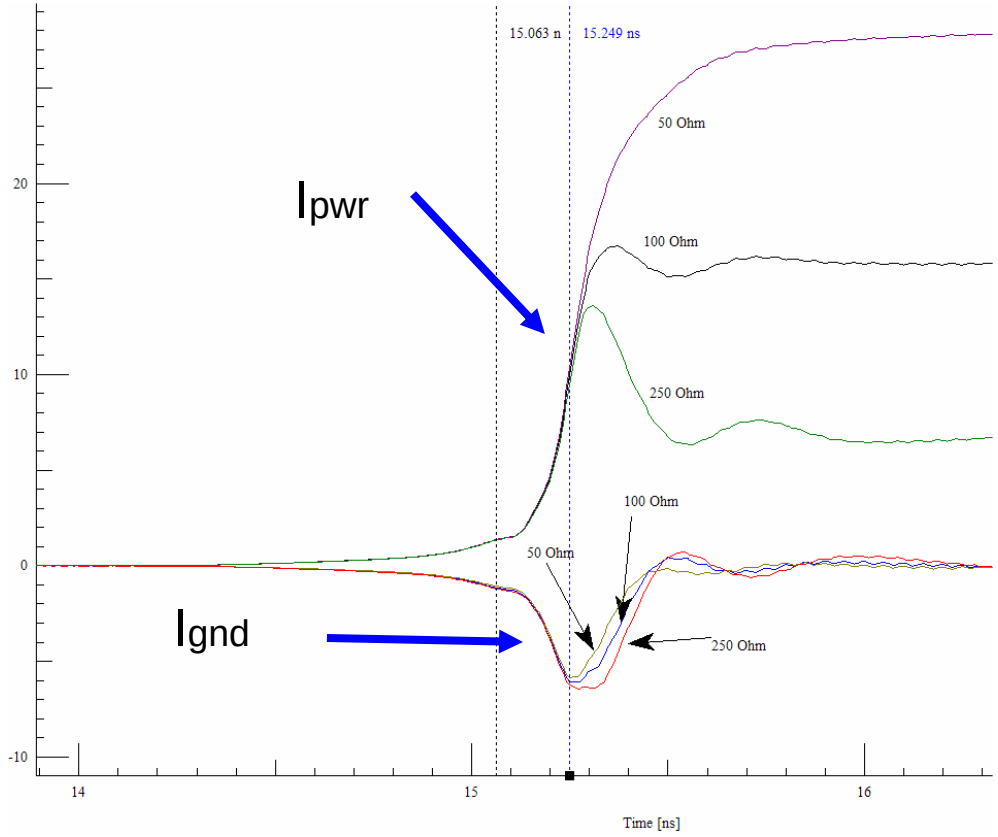
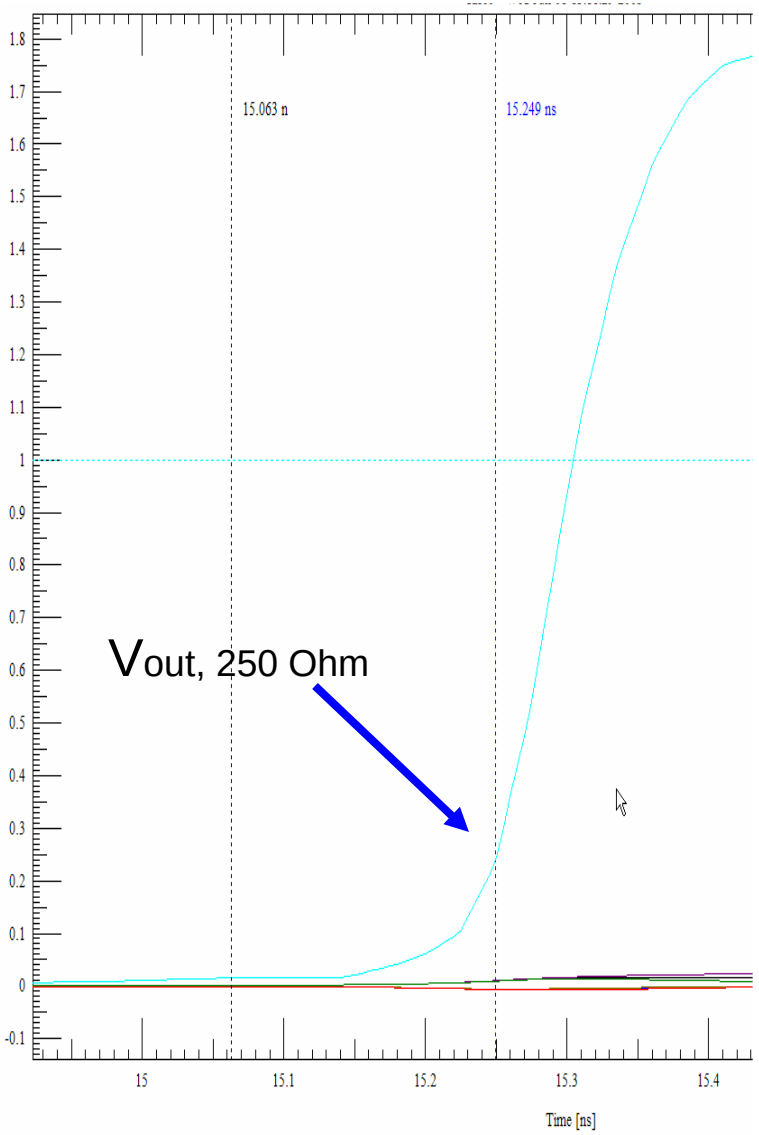
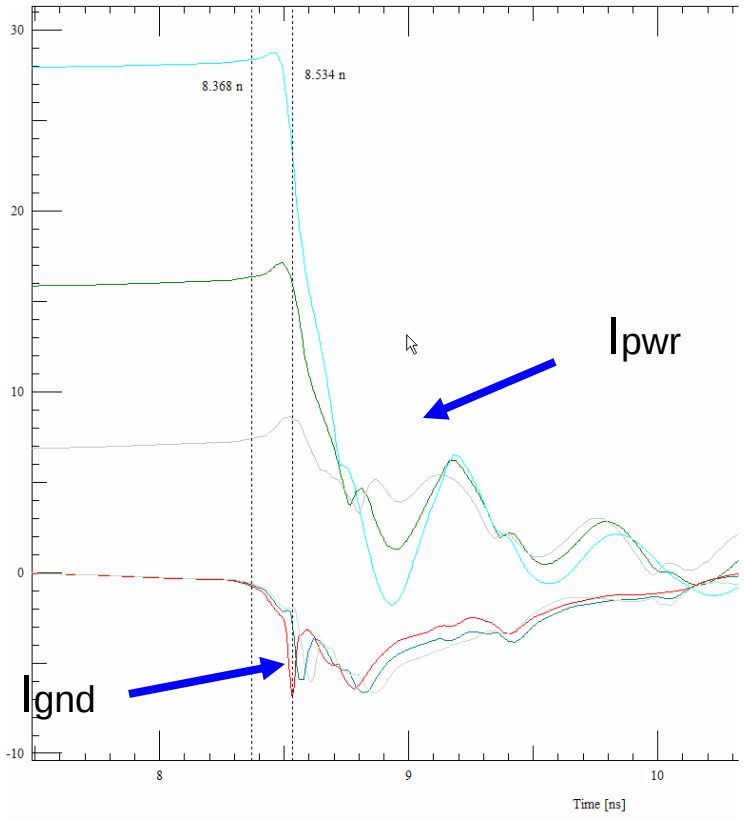


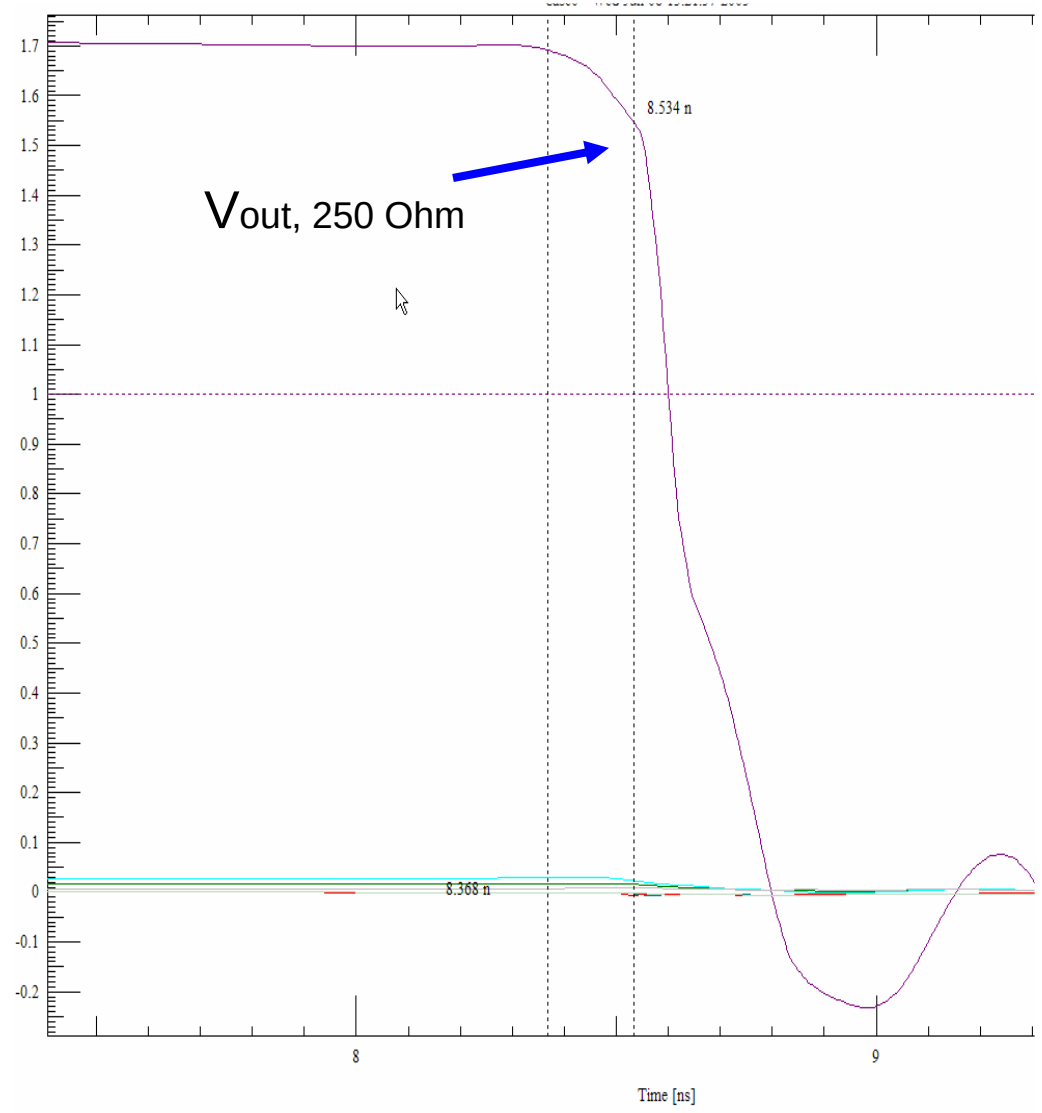


Ground Bounce Current

7 drivers active in the 7-driver network

Falling edge , 50, 100, 250 Ohm loads





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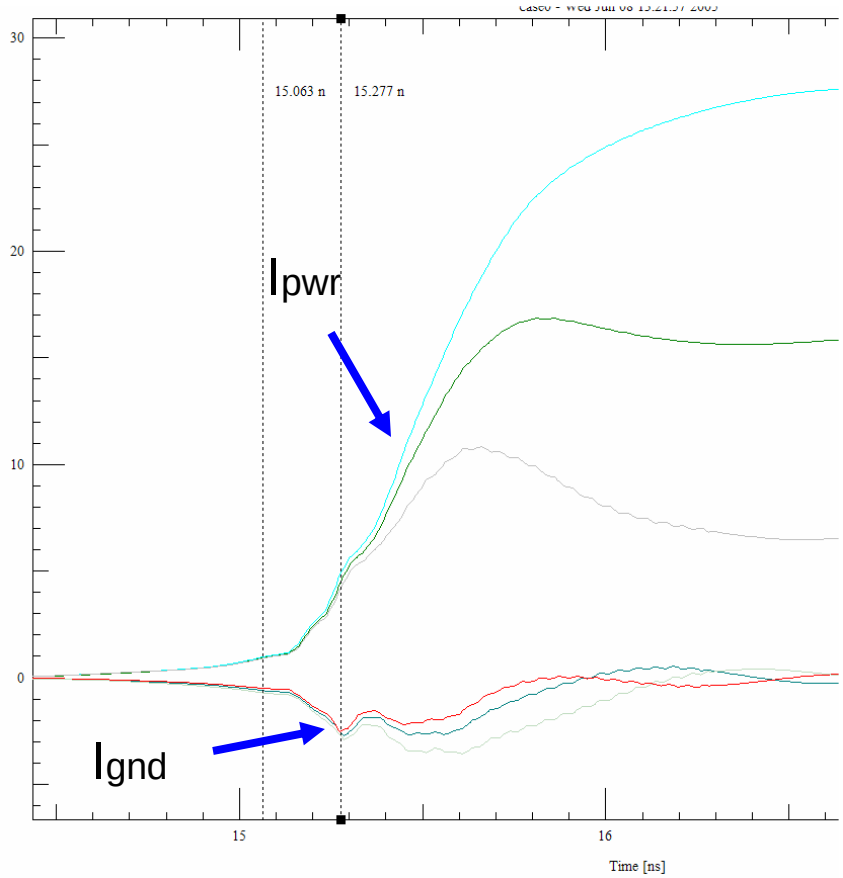
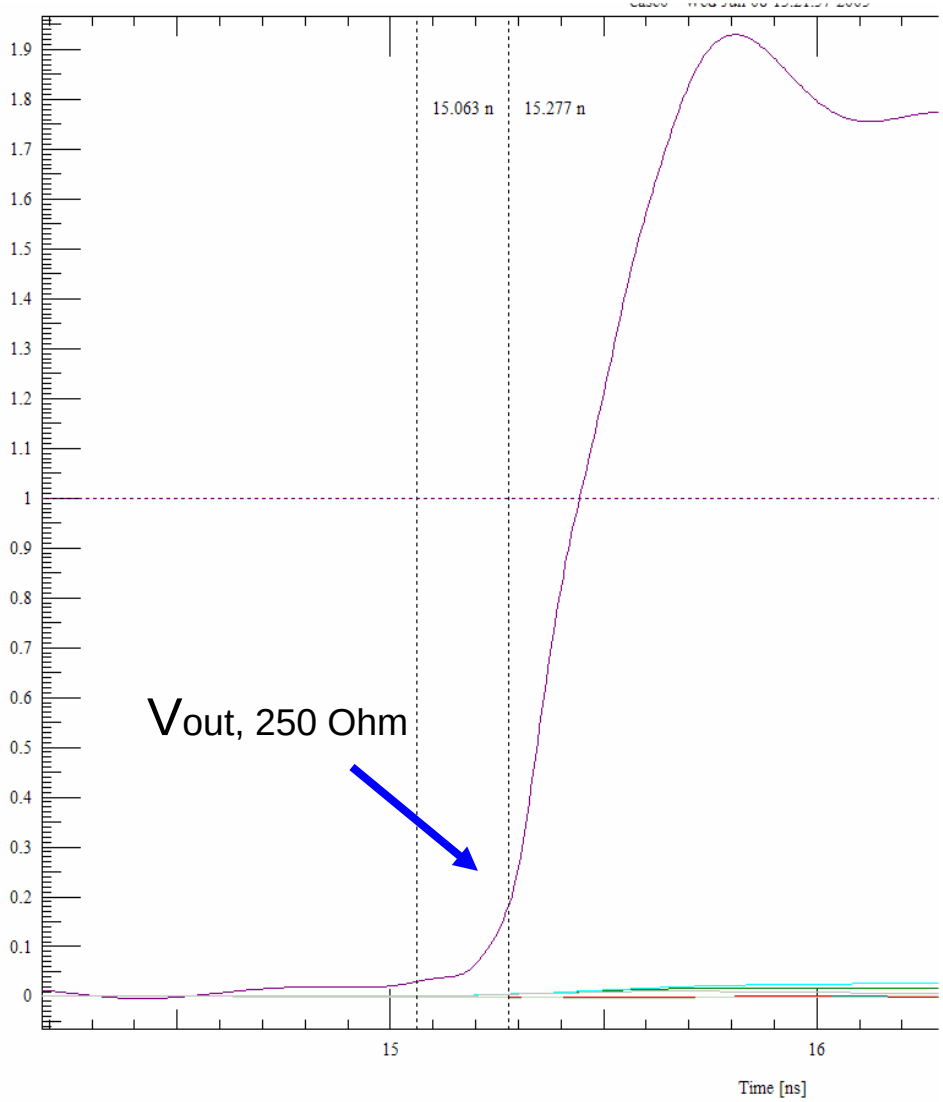
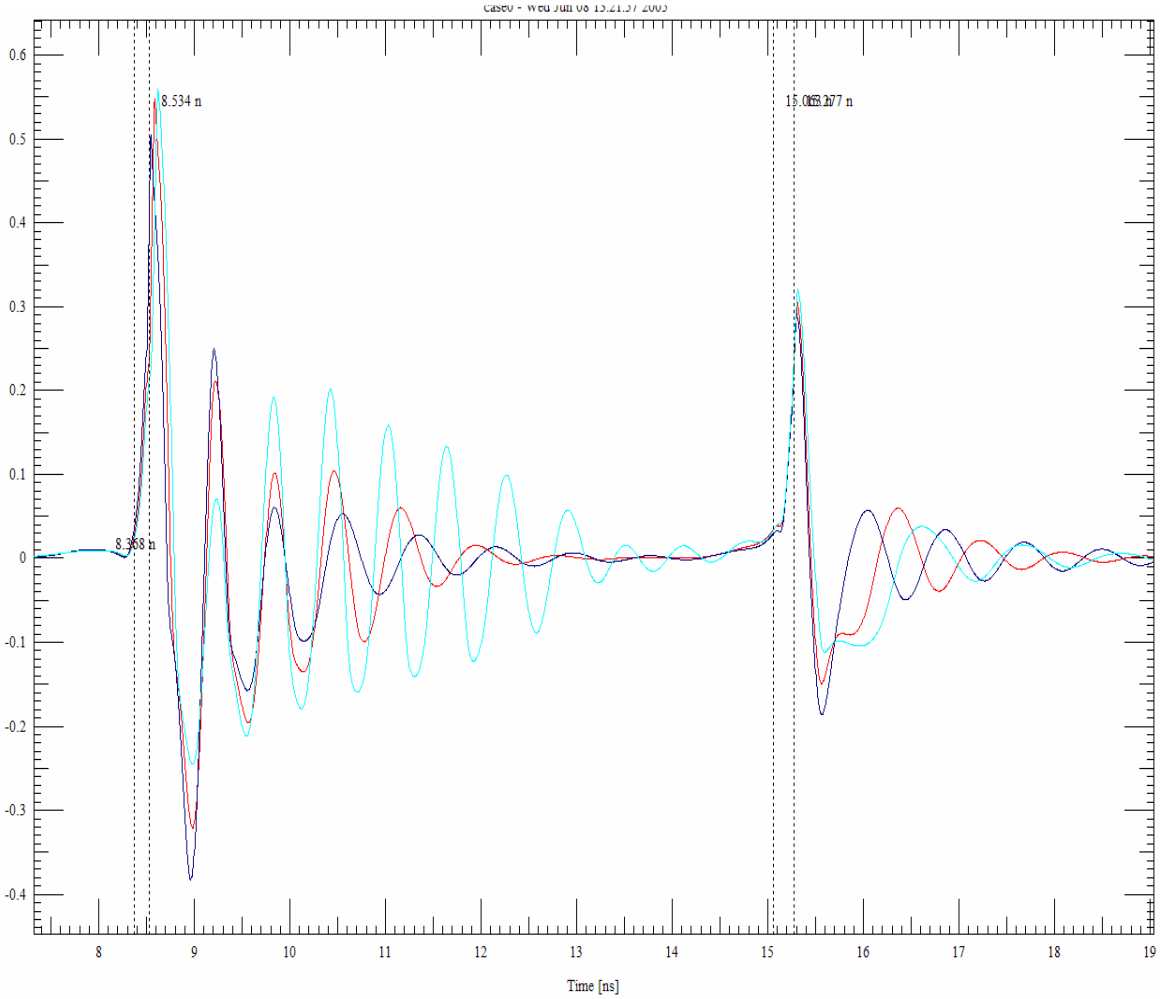




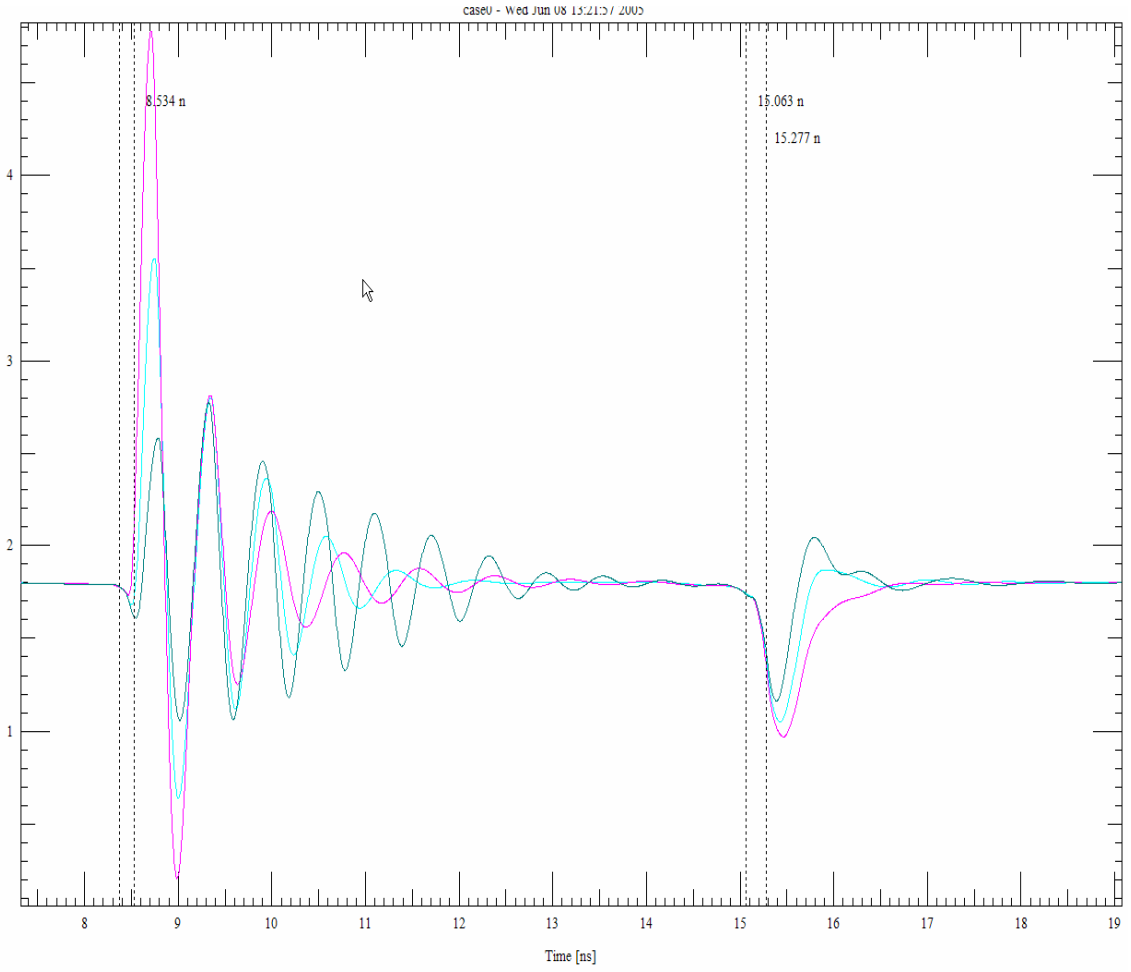
Ground Bounce Voltage



7 drivers active in 7 driver network

50, 100, 250 Ohm loads

Power Bounce Voltage



7 drivers active in 7 driver network

50, 100, 250 Ohm loads

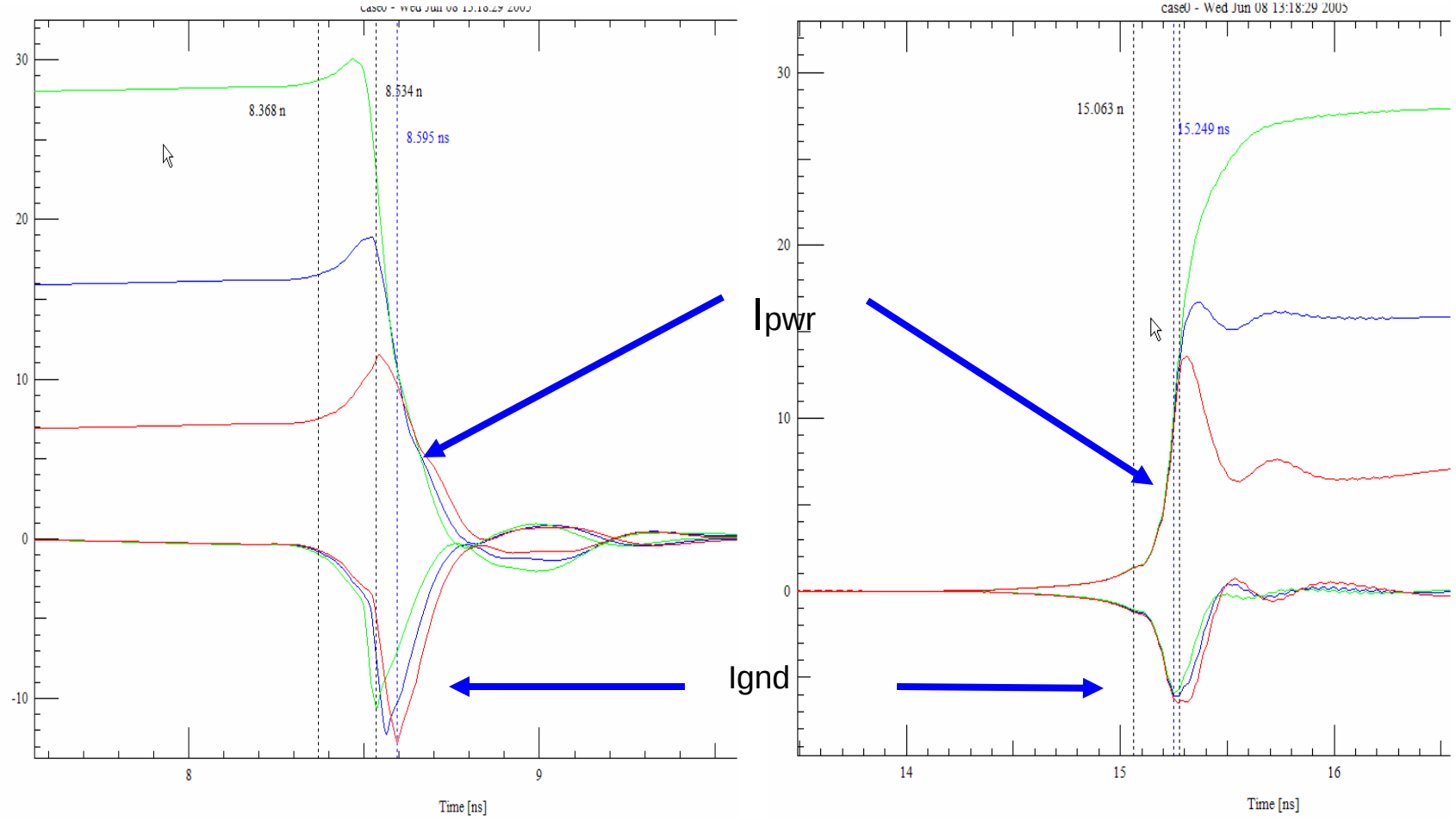
IT Tables

- Can IT tables be used as the “Profile” for SSN?
- Can this scale cleanly to different load conditions?

IT Tables

1 driver active in 7-driver network

50, 100, 250 Ohm loads



IT Tables

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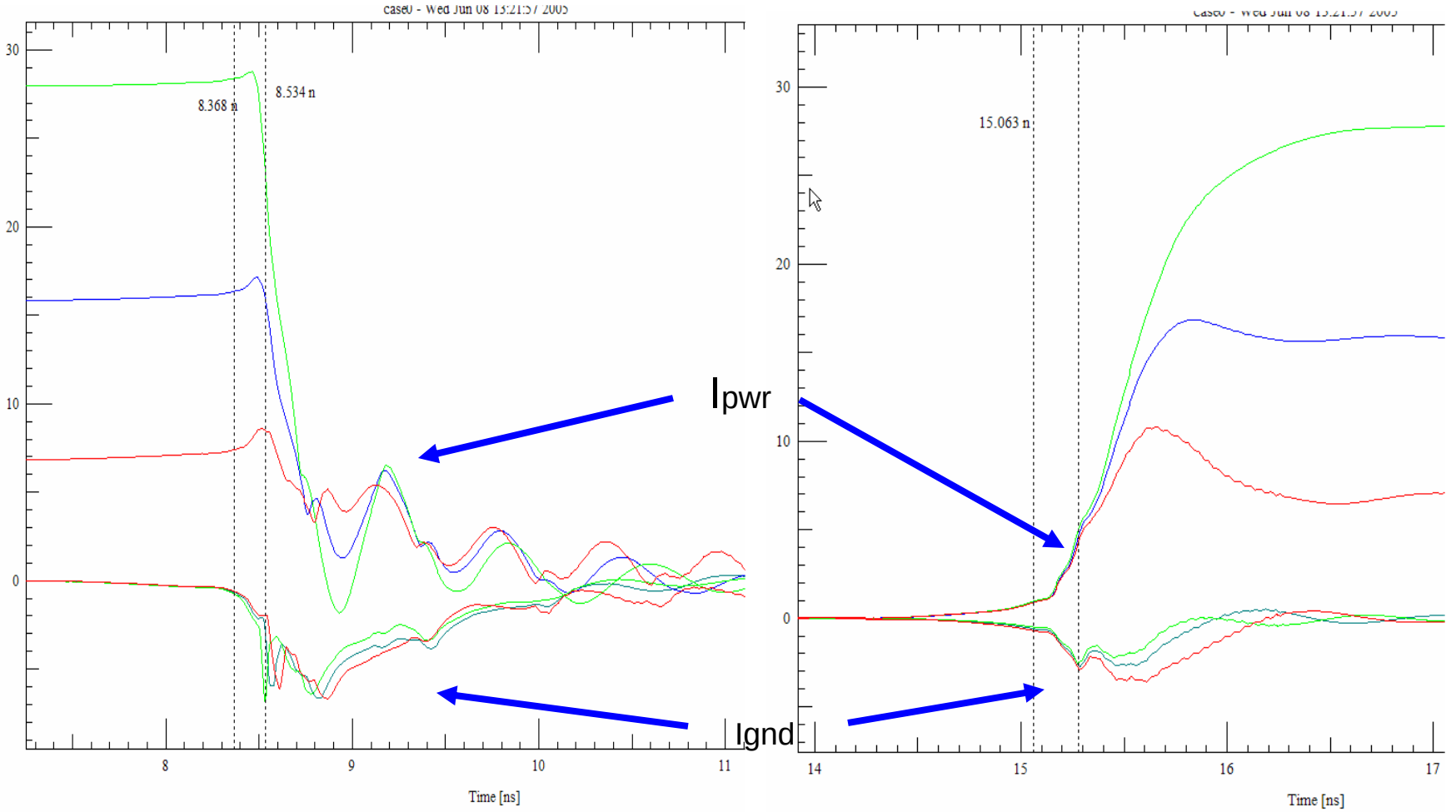


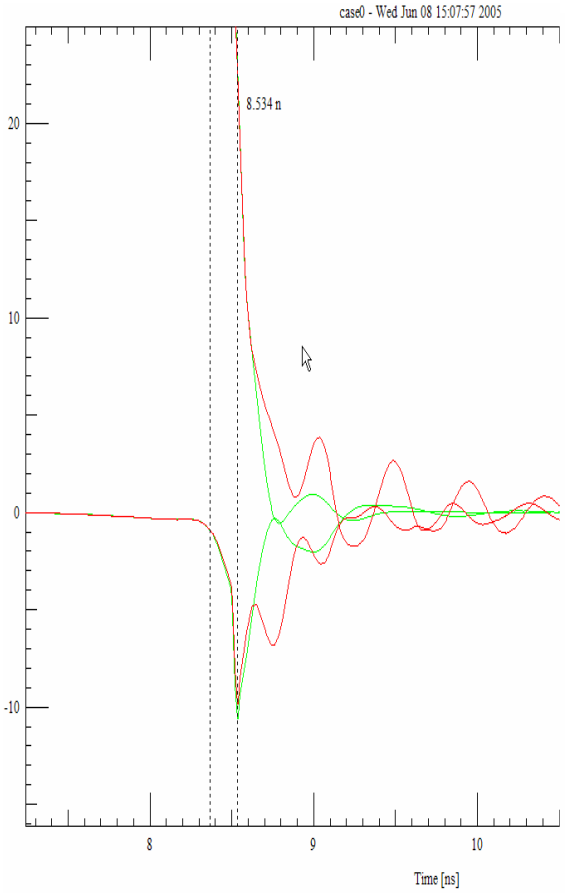
Individual Profile vs. Profile in the Network

- Can the individual profile for one driver be applied to the network case?

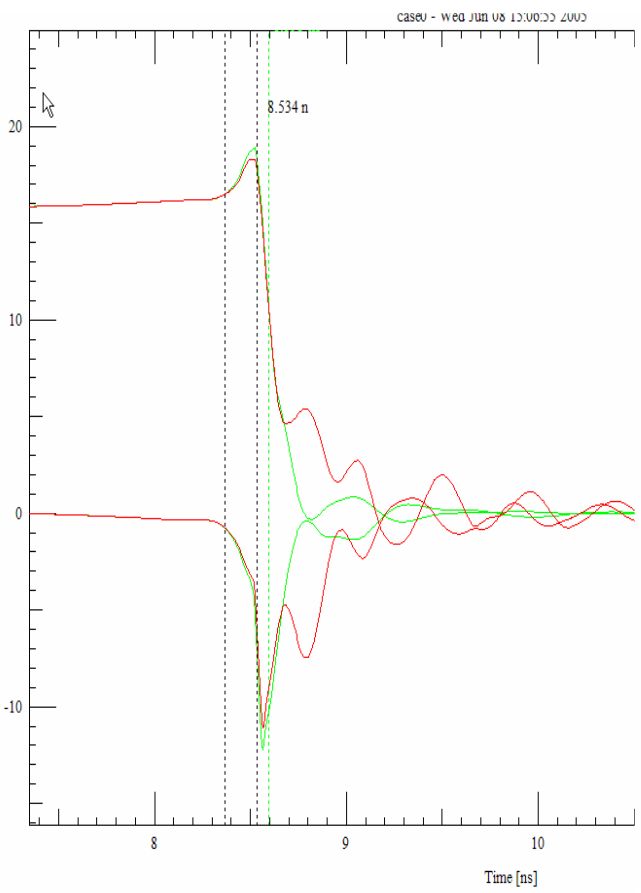
Individual Profile vs. Profile in the Network

Falling

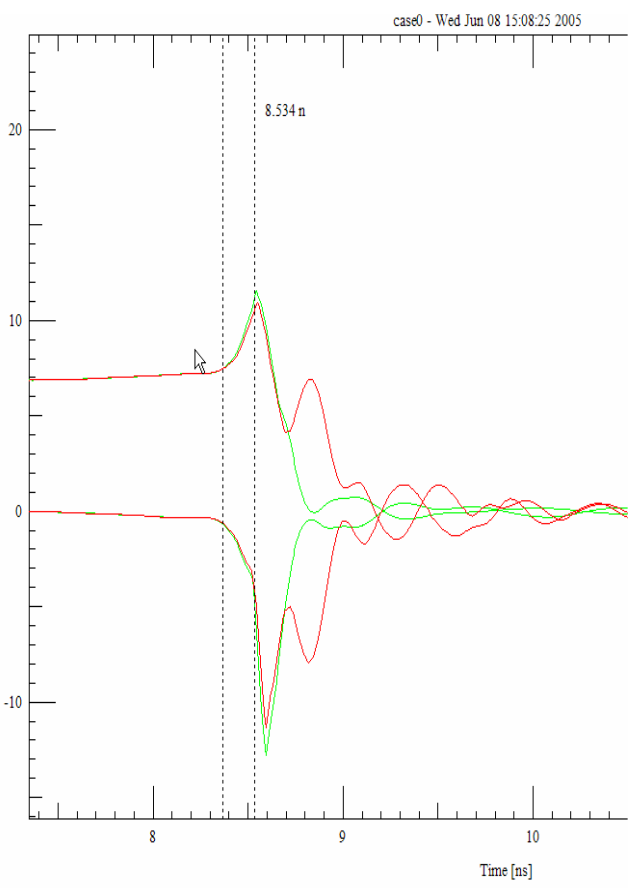
50 Ohm



100 Ohm



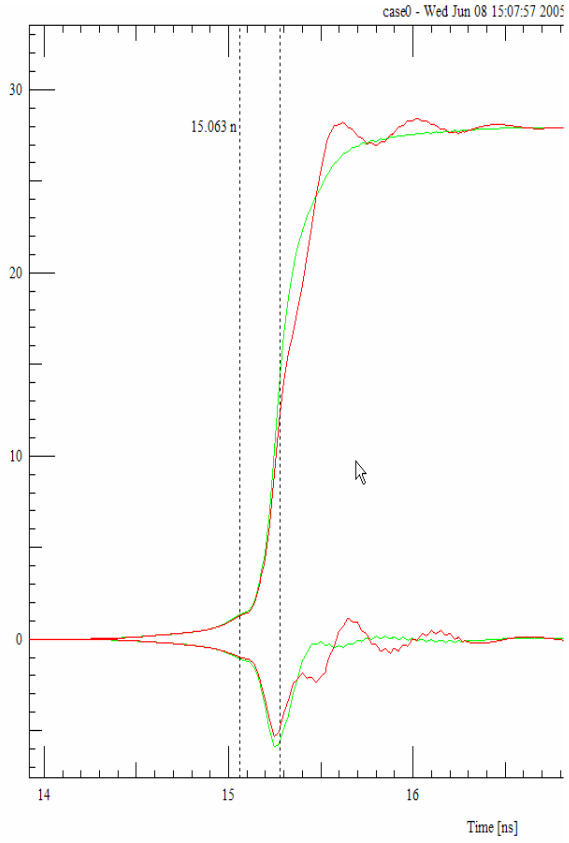
250 Ohm



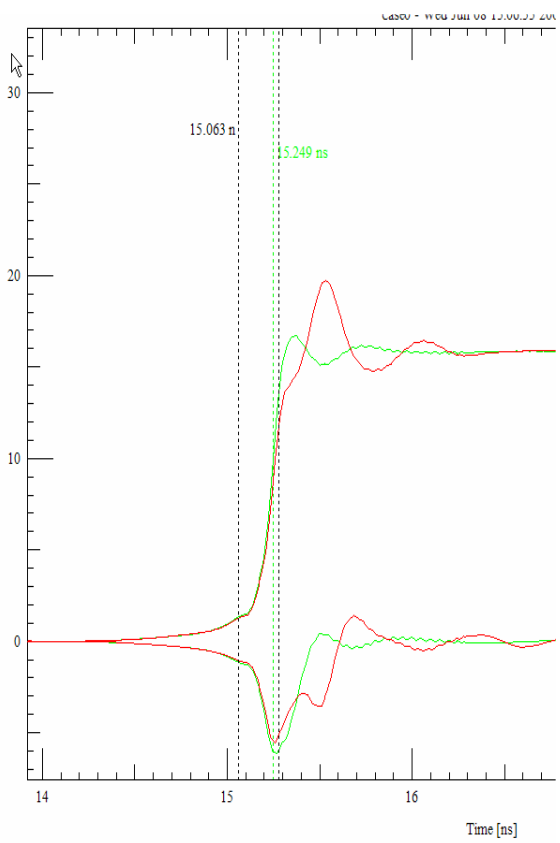
Individual Profile vs. Profile in the Network

Rising

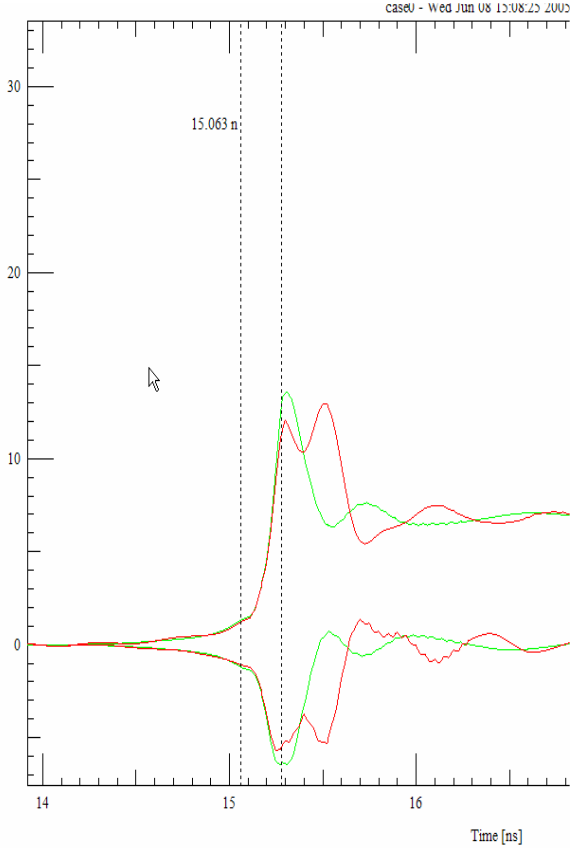
50 Ohm



100 Ohm



250 Ohm



Conclusions

- Ground Bounce Current Should be considered in the Profile
  - These are not “Static” entities
  - Active devices might store energy somewhere inside the “black box”
  - Otherwise, leaves ground current profile “open to interpretation”
- IT curves seem insufficient to be the sole Profile Data
  - Difficult to scale volatile IT curves for different loading & network conditions
- Profile data should be captured in the context of its Network
  - There are significant differences between “individual” profile and “network” profile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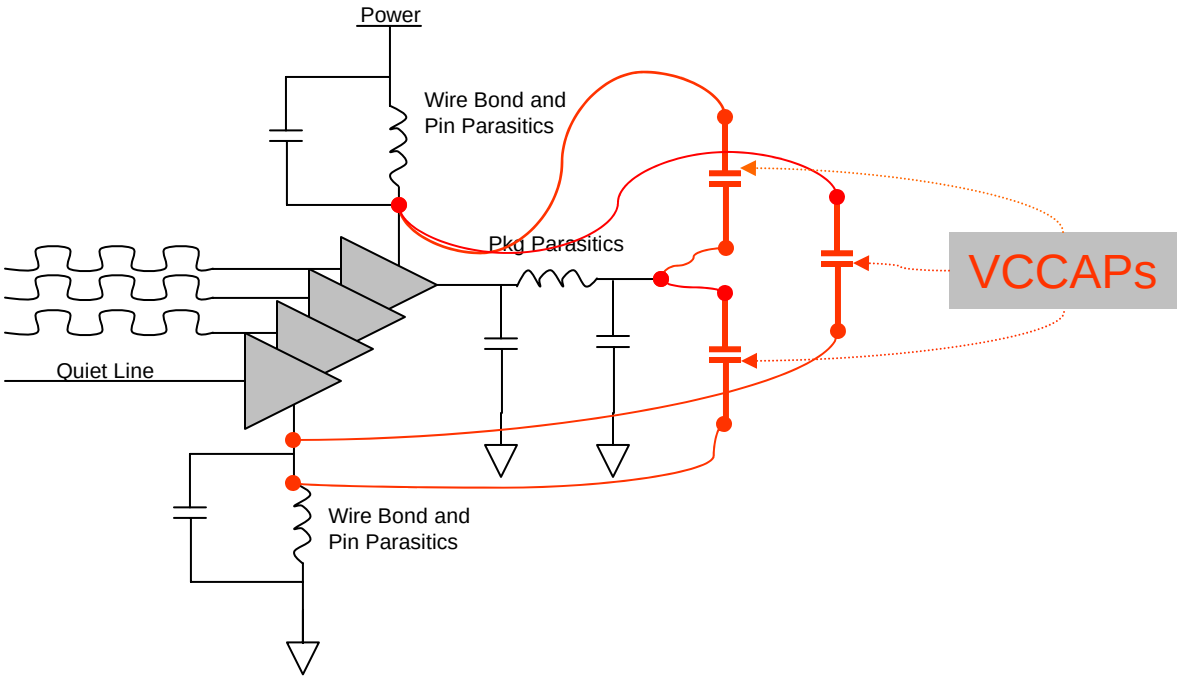
BACK UP SLIDES

Ambrish Varma's VCCAP Slides

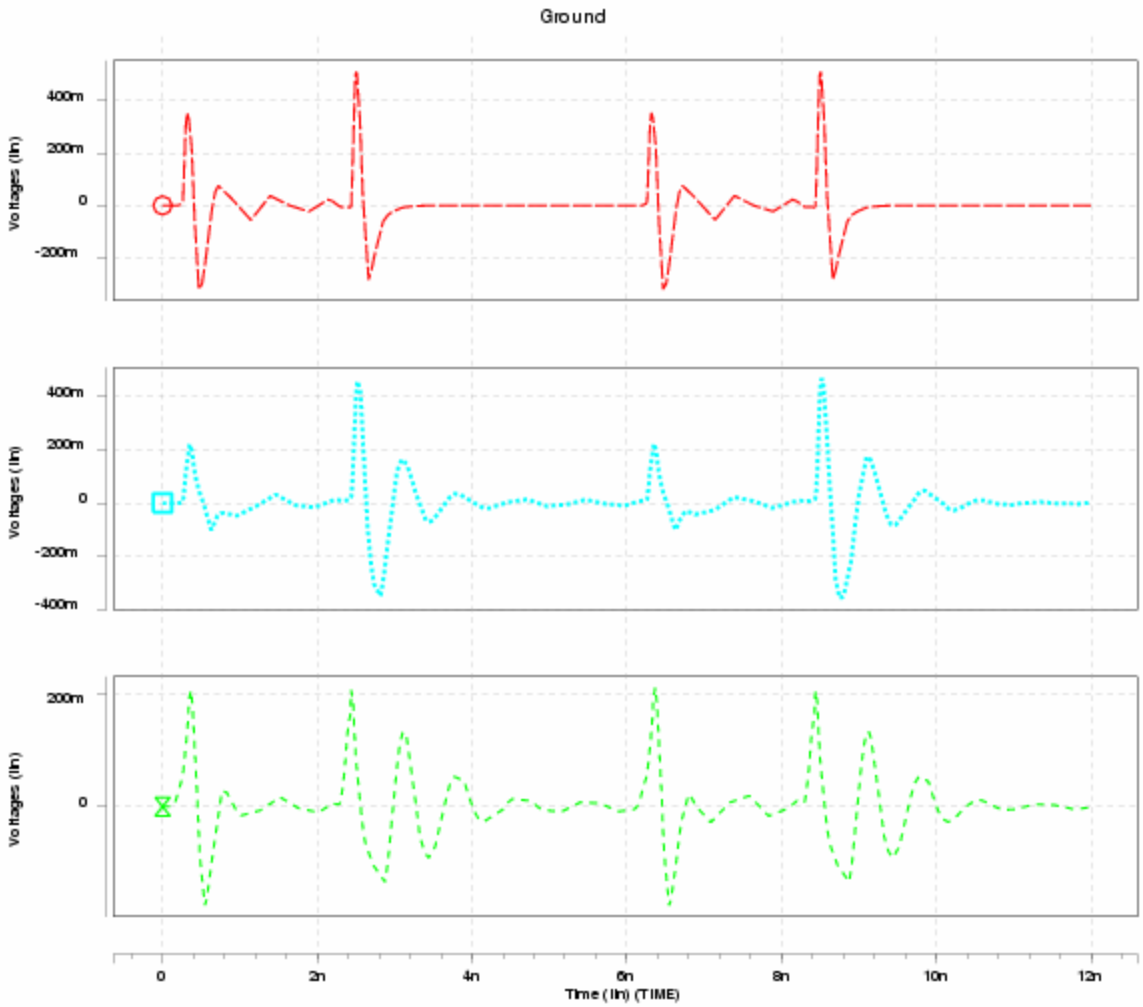
A possible solution for Buffer (Pin) Signature in SSN/PI

A Solution



- **No Changes to the IBIS spec**
- **Considerable improvement in SSN noise representation**
- **Depends on the buffer**
- **Customizable, depends on the end user**
- **Implemented for Voltage and Current mode drivers**

Ground

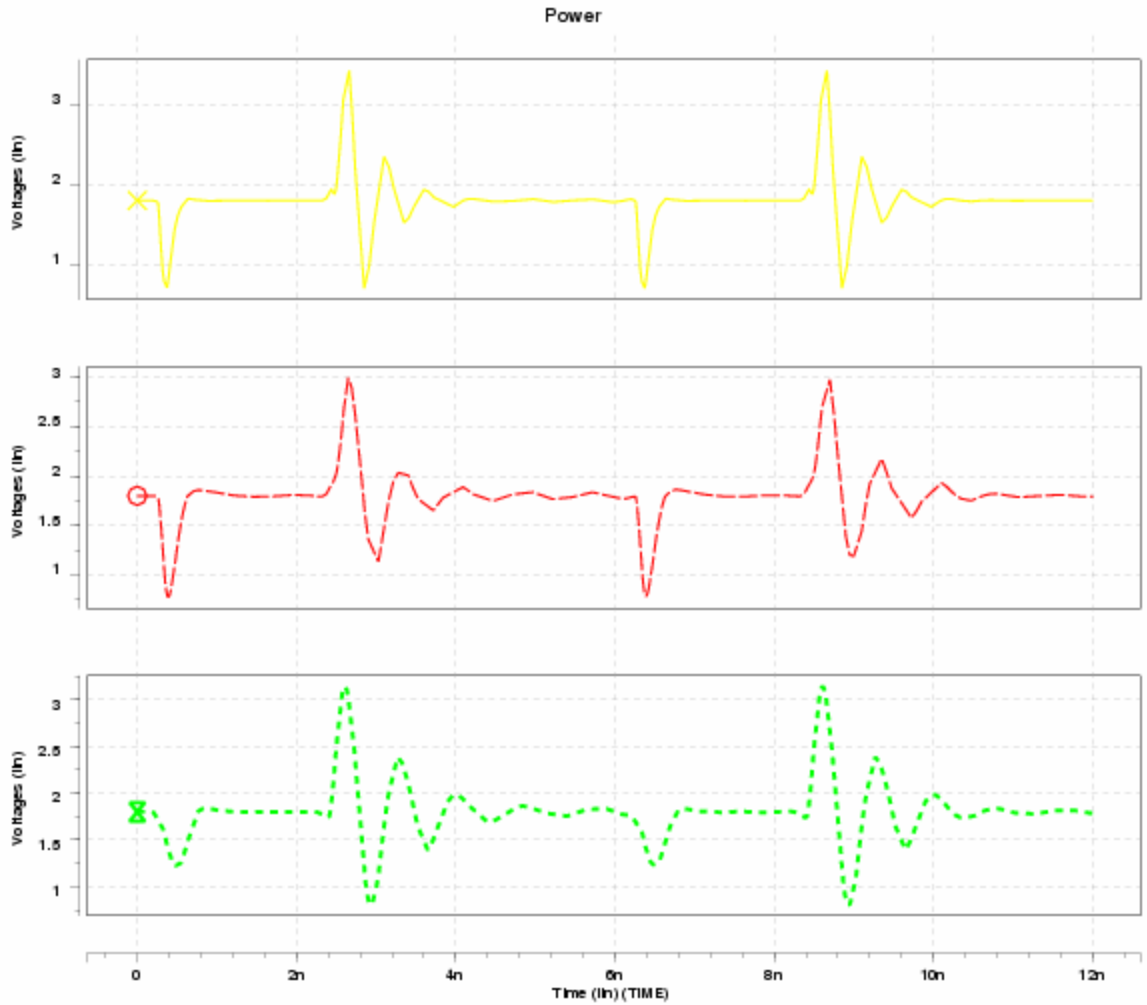


Plain IBIS

IBIS With VCCAPS

HSPICE

POWER

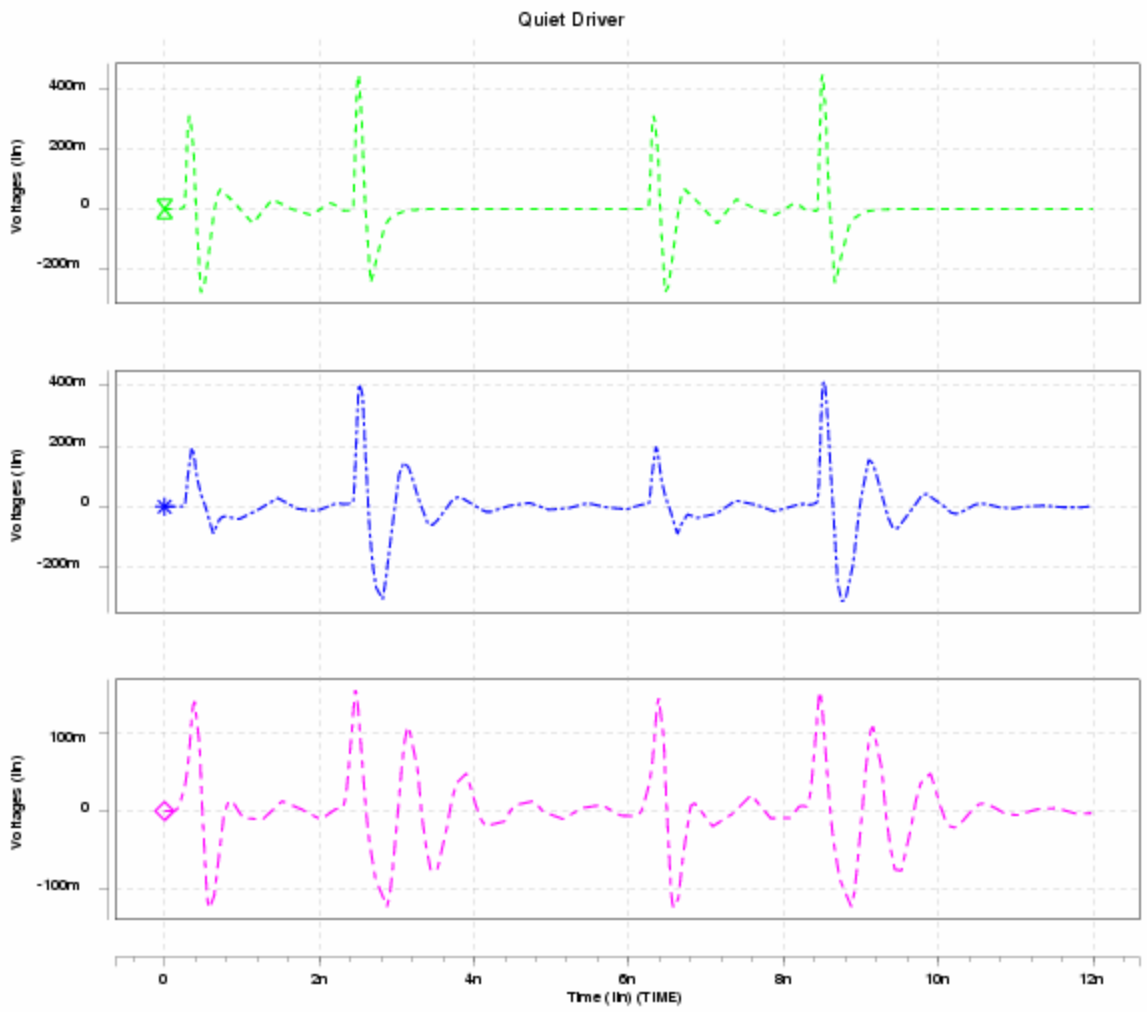


Plain IBIS

IBIS With VCCAPS

HSPICE

Quiet Driver



Plain IBIS

IBIS With VCCAPS

HSPICE