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# Multi-buffer SSN Simulation using BIRD95

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- Implementation Steps
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# Review of the key points in BIRD95.5

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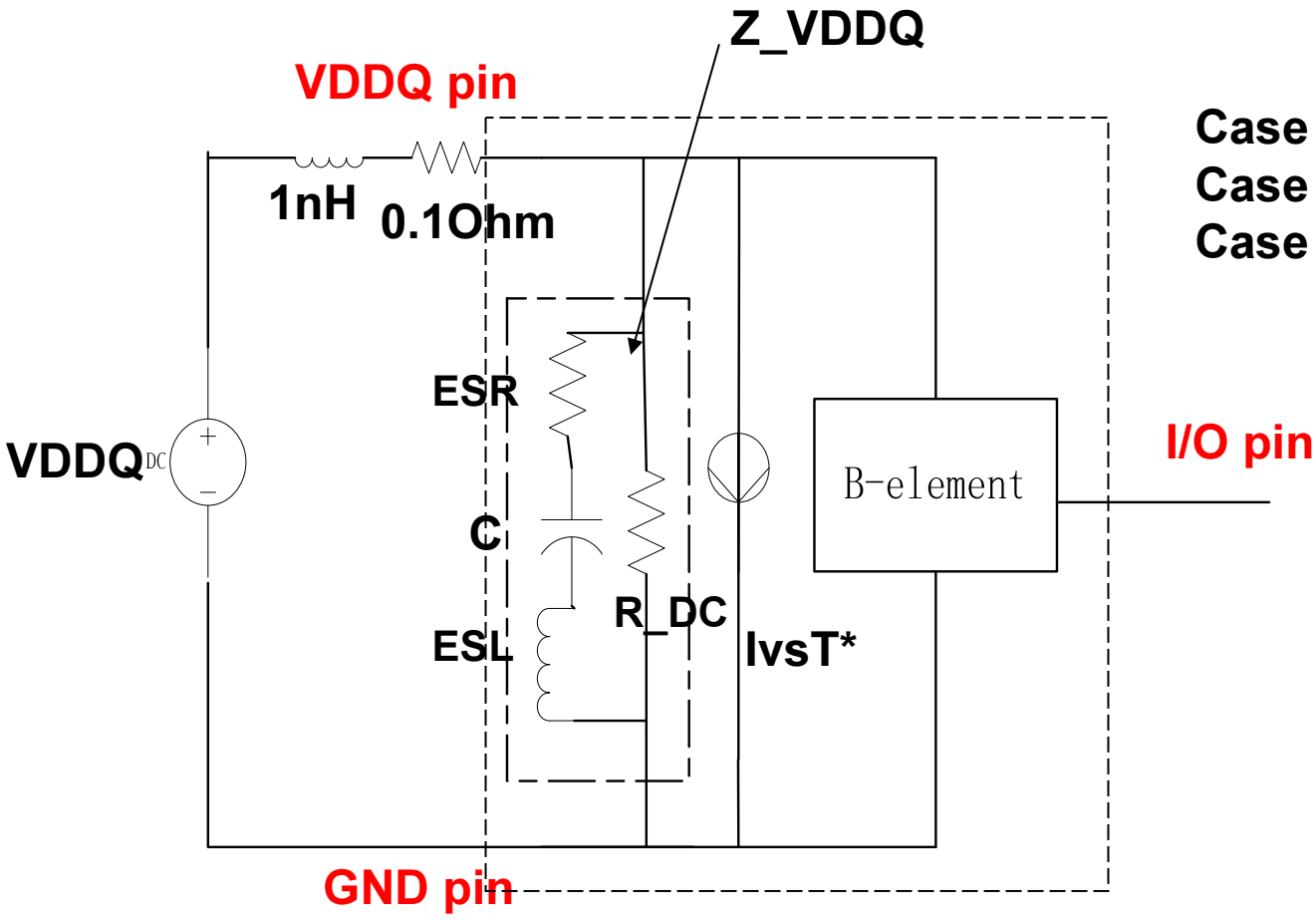
- Added [Composite Current] keyword to represent the total current flow through buffer VDDQ node
- Used Series Model Type keywords for On-die parasitic associated with VDDQ (possibly ICM model can be used in the future)
- Gate Modulation will be address by BIRD97
- X-bar current could possibly be addressed by another BIRD

# *BIRD95* Implementation Schematics






**Case 1: B-element only**
**Case 2: B + IvsT***
**Case 3: B+IvsT*+Z_VDDQ**

**Note: IvsT* is different with IvsT table in BIRD95, but it is derived from IvsT table**

# Definition of IvsT and Z_VDDQ

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- IvsT is the total current from the VDDQ which is connected to ideal DC voltage source
- Six IvsT tables (3 different I/O loadings associated with rising/falling edges) are not required, but recommended
- Z_VDDQ is the frequency-dependent impedance derived with the correct DC voltage applied at VDDQ pin and open-load condition
- Z_VDDQ information is proposed to be provided through ICM model

# IvsT* and parasitic components

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- IvsT*=IvsT (*BIRD95* table)-IvsT**
- IvsT** is the total current from the VDDQ by using existing IBIS model with Z_VDDQ connected in parallel.
- All currents here are under ideal power supply and standard loading conditions.
- Two sets of IvsT* associated with rising and falling edge were derived by averaging different loading conditions in our examples. More complicated model could be derived from 6 IvsT* tables to compensate the load variation effects.
- ESR, ESL, C and R_dc can be extracted from Z_VDDQ to match the impedance in frequency domain
- The ESR, ESL, C and R_dc is just one example of the possible circuits to match Z_VDDQ. It could cover majority I/O buffers' on-die parasitic components.

# Multi-buffer SSN Simulation

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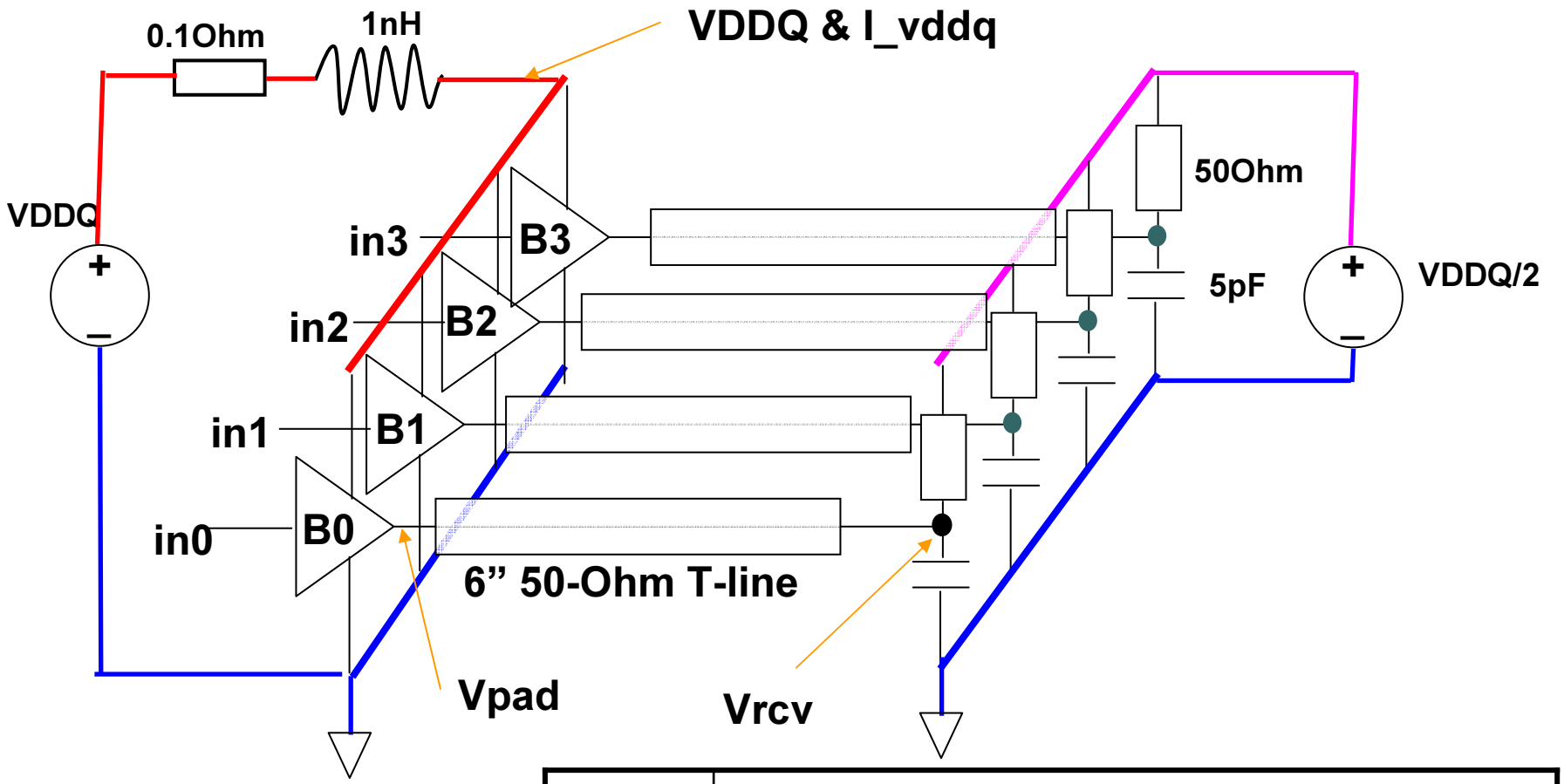
- An impedance-controlled 1.8V HSTL output buffer is used as an example
- IBIS model is extracted from HSPICE transistor model
- HSPICE B-element is used to simulate the IBIS model
- *BIRD95* IvsT info is implemented with ideal current source in parallel with B-element
- 4 identical buffers are used to simulate the SSN noise
- 5 different switching modes are studied
- Non-standard load (6” 50Ohm transmission line with 5pF and 50Ohm resistor to VDDQ/2 at receiver) is used in simulations.

# Simulation schematics



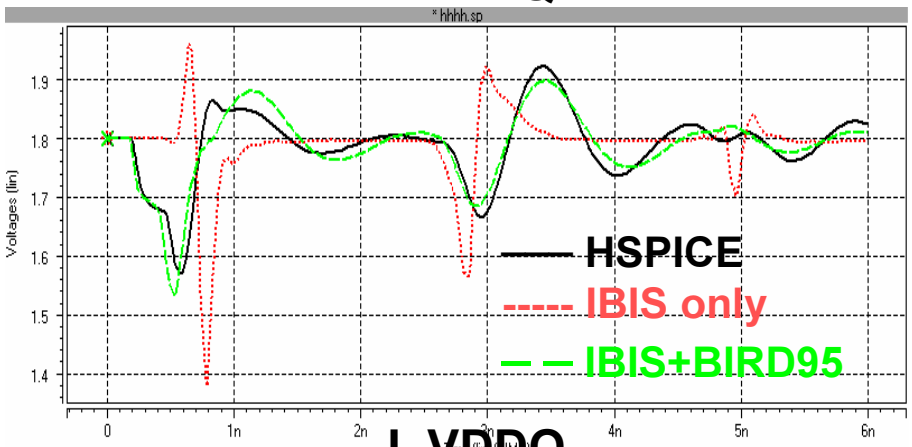



| | Input date pattern | | | | |
|---|---|---|---|---|---|
| in3210 | HHHH | HHHL | HHLL | HLLL | LLLL |

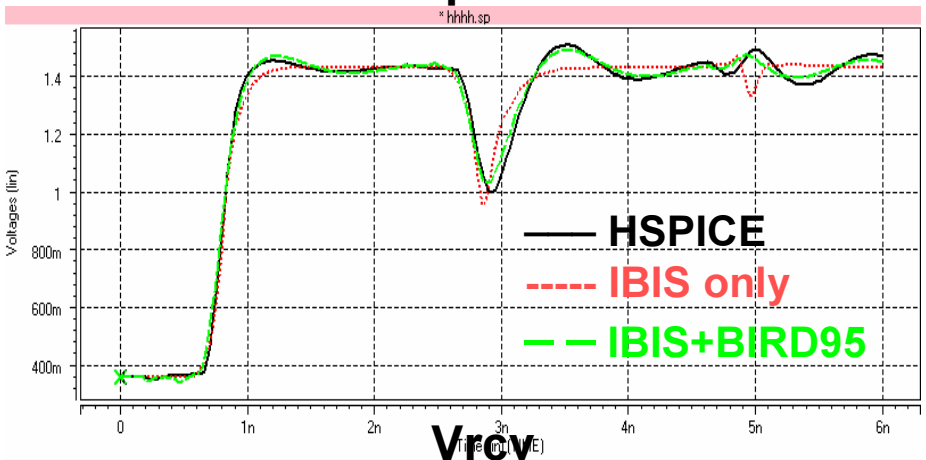
# Case with input pattern of HHHH



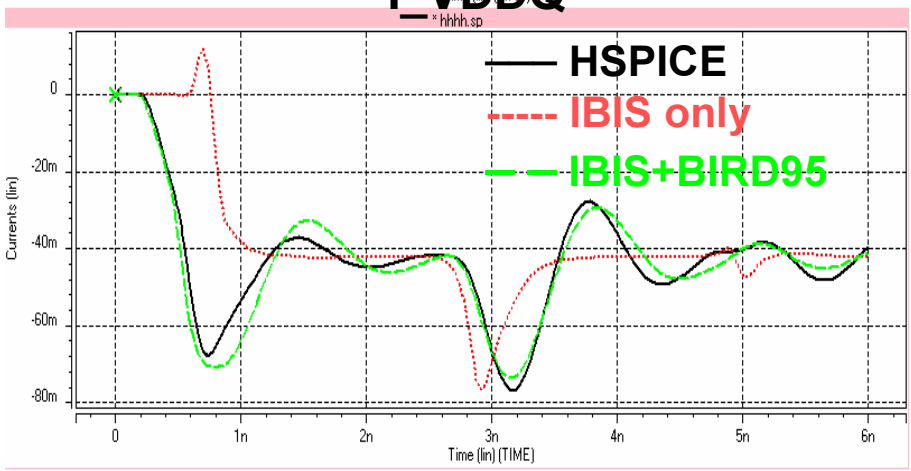
VDDQ



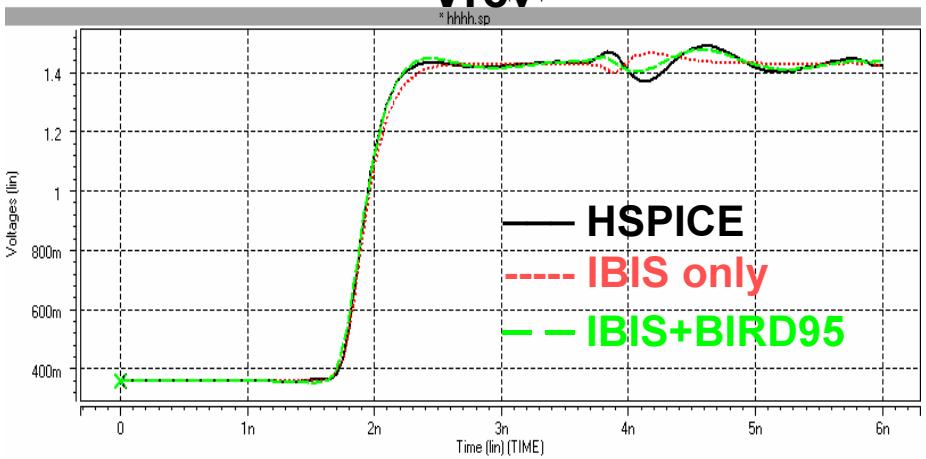

Vpad




I_VDDQ



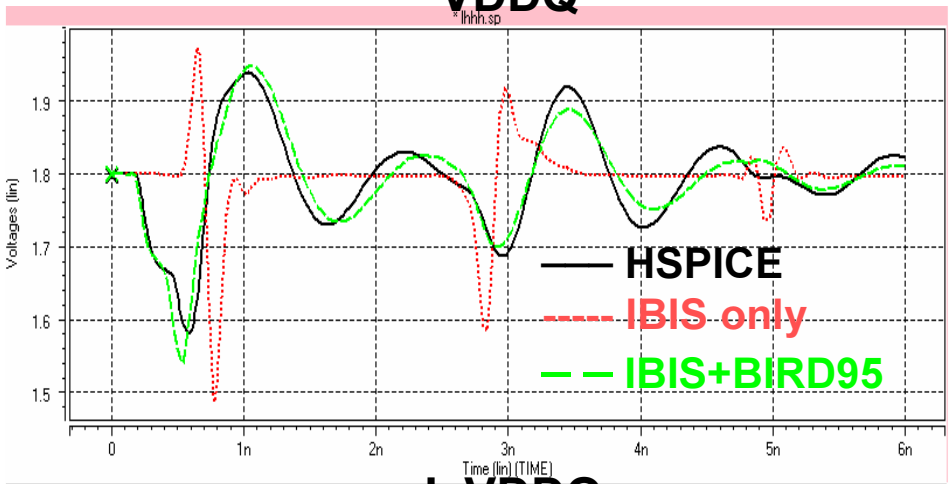

Vrcv



# Case with input pattern of HHHL



VDDQ

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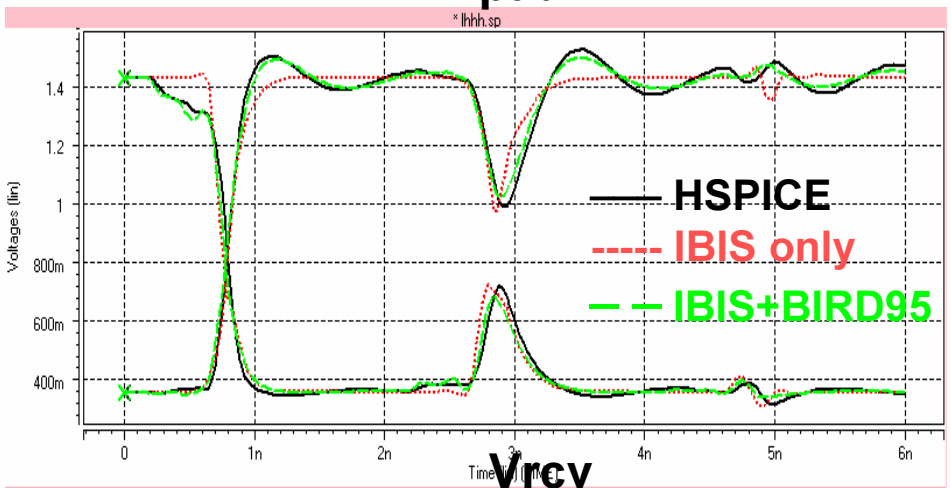
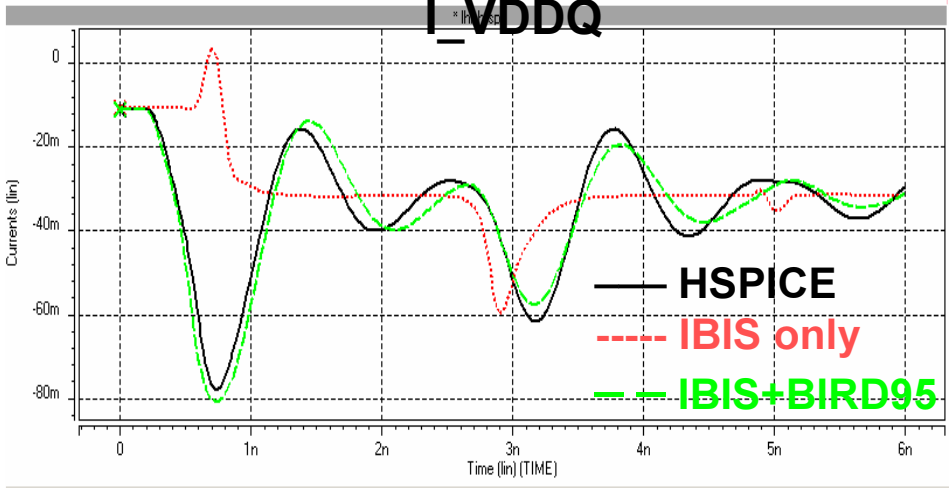
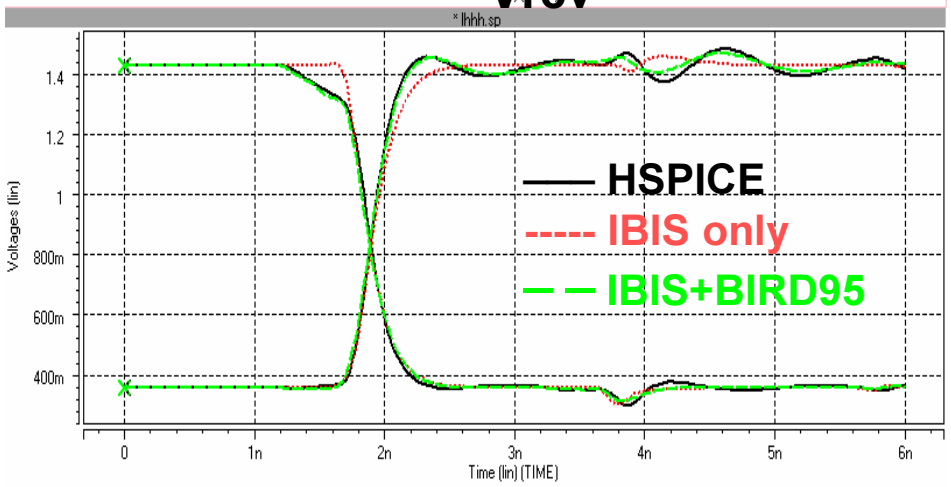



I_VDDQ



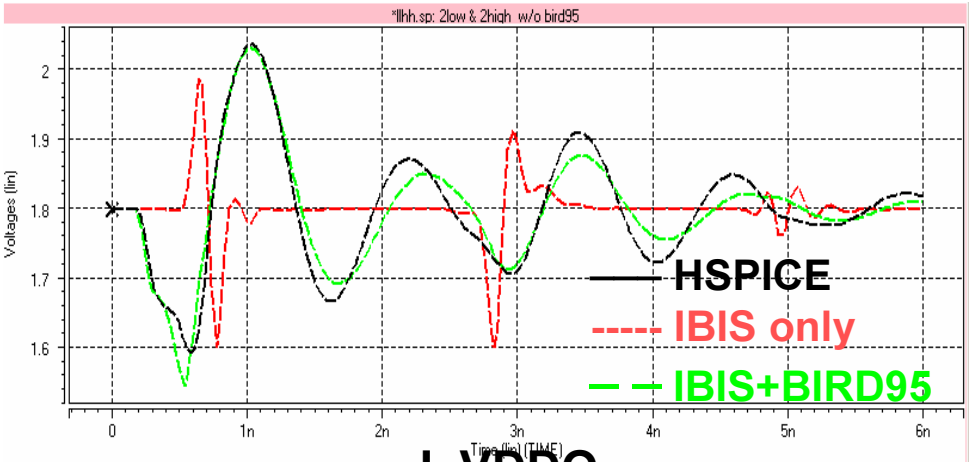

Vrcv



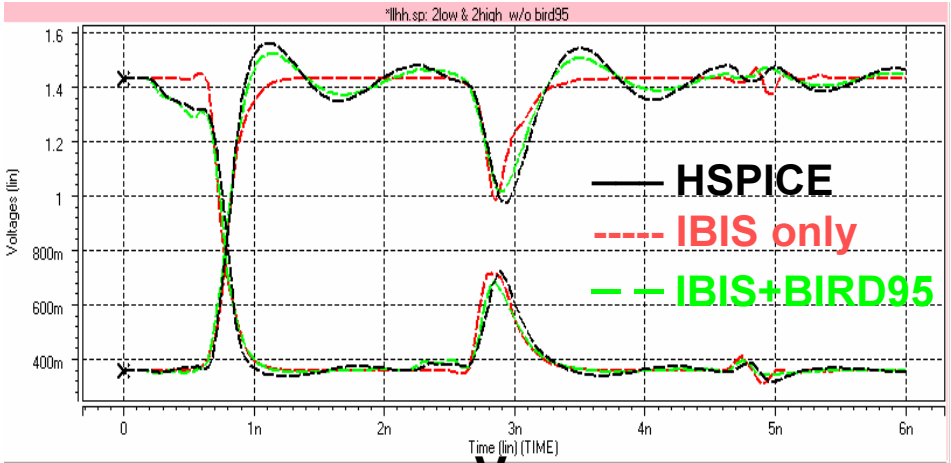
# Case with input pattern of HHLL



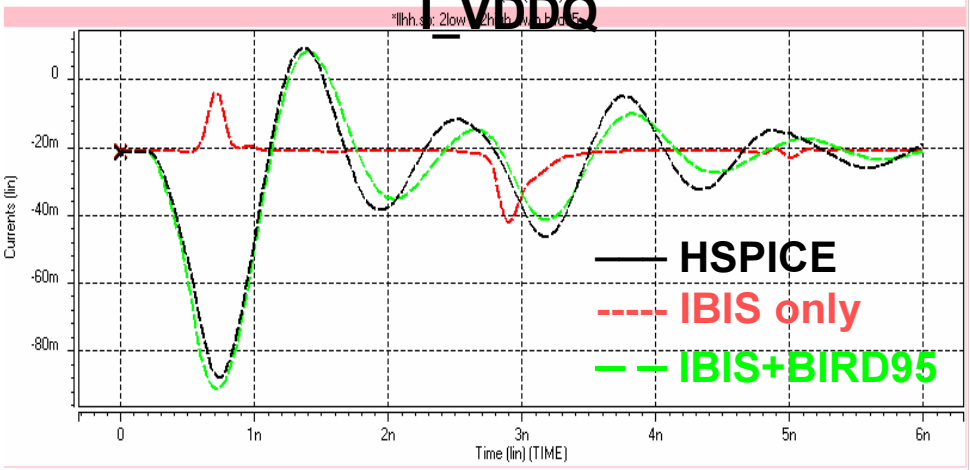
VDDQ



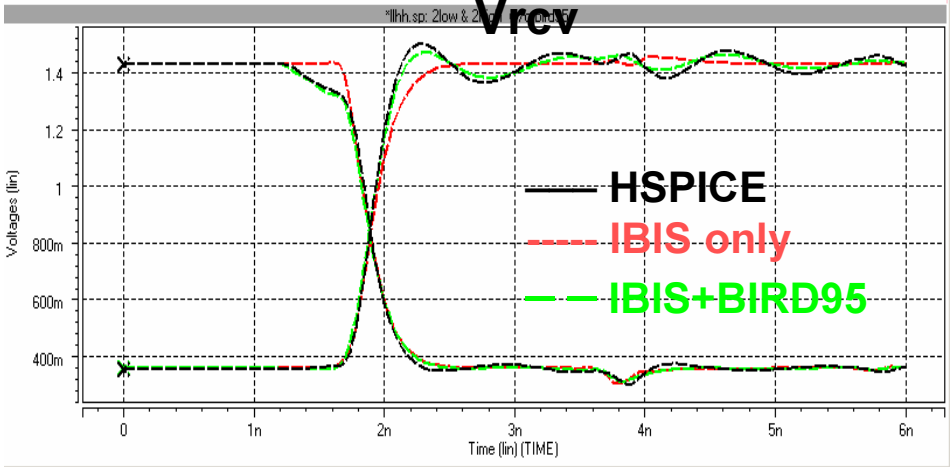

Vpad




I_VDDQ



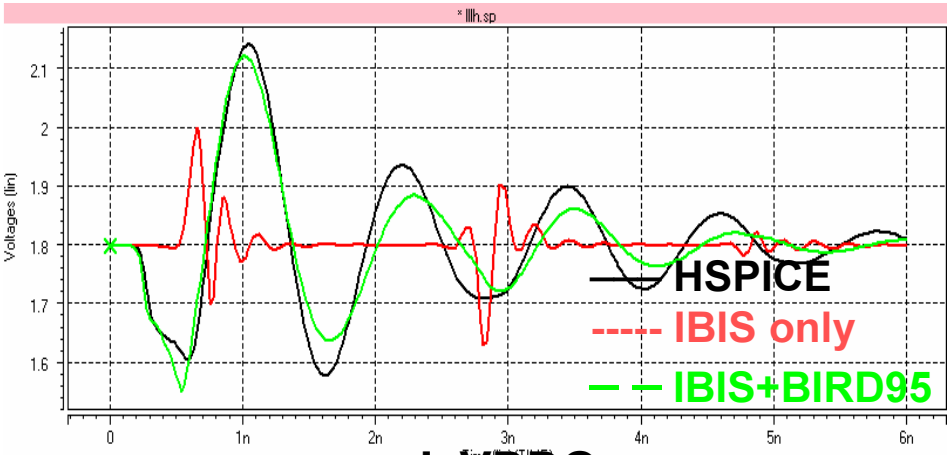

Vrcv



# Case with input pattern of HLLL



## VDDQ

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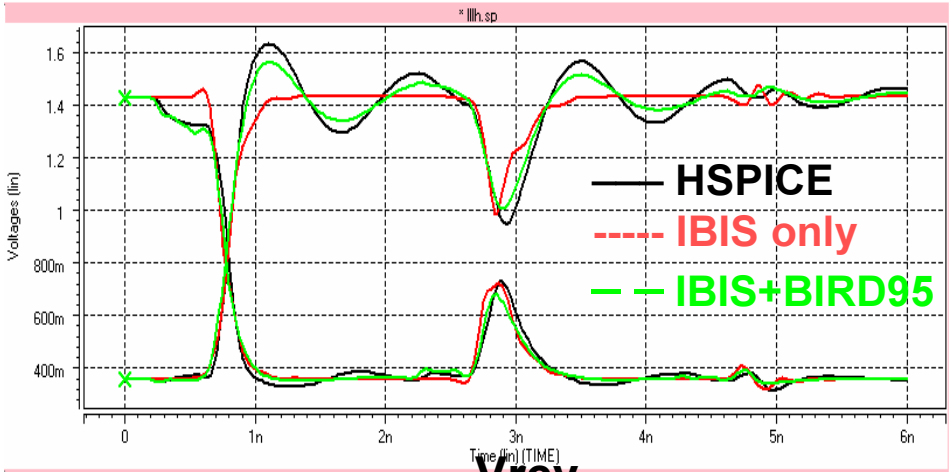
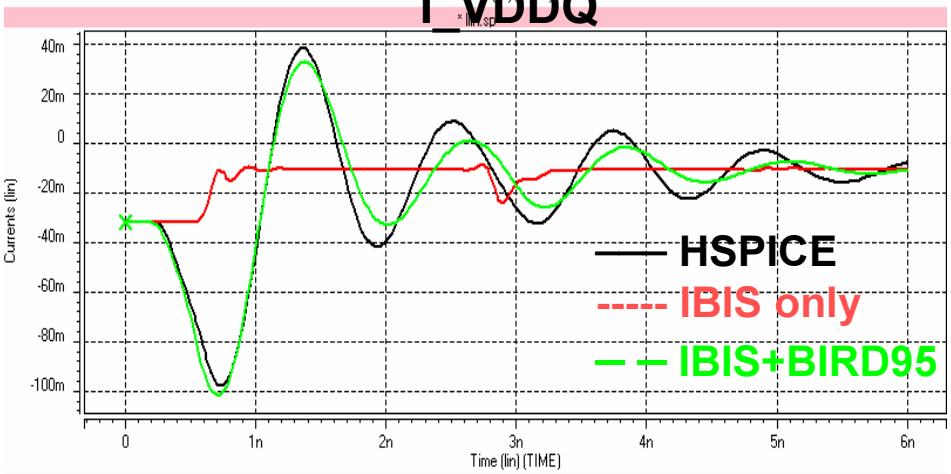
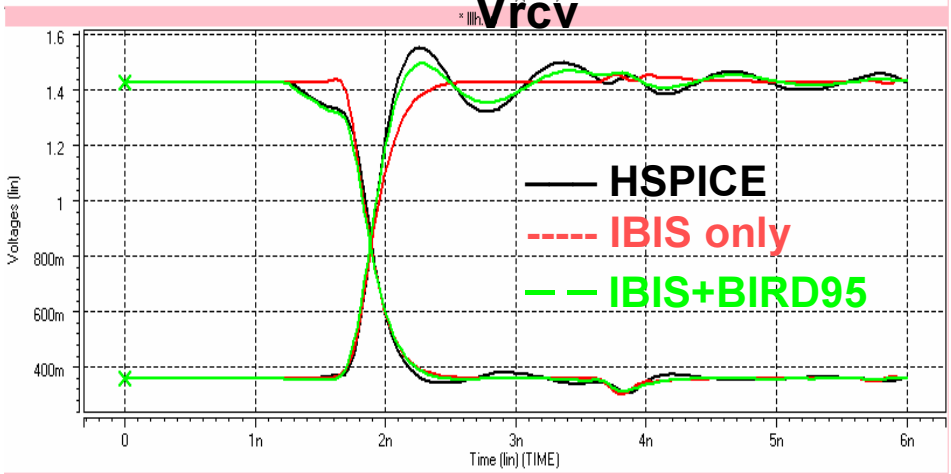



## I_VDDQ



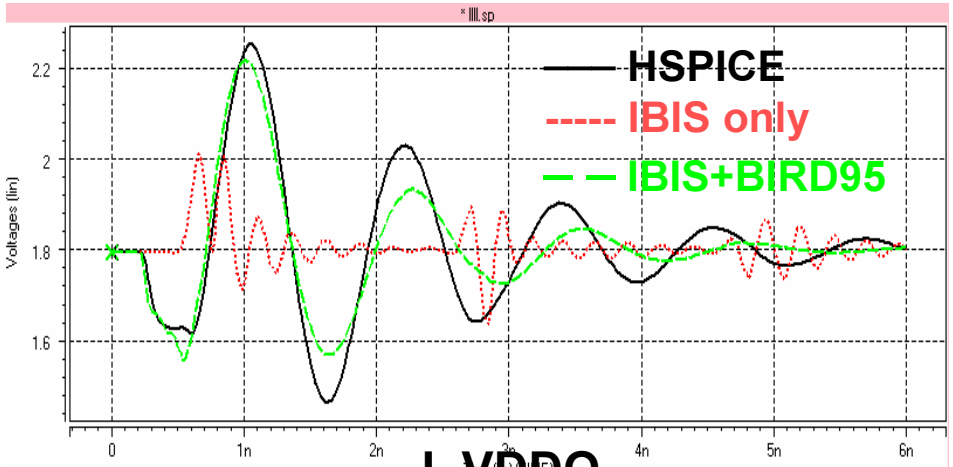

## Vrcv



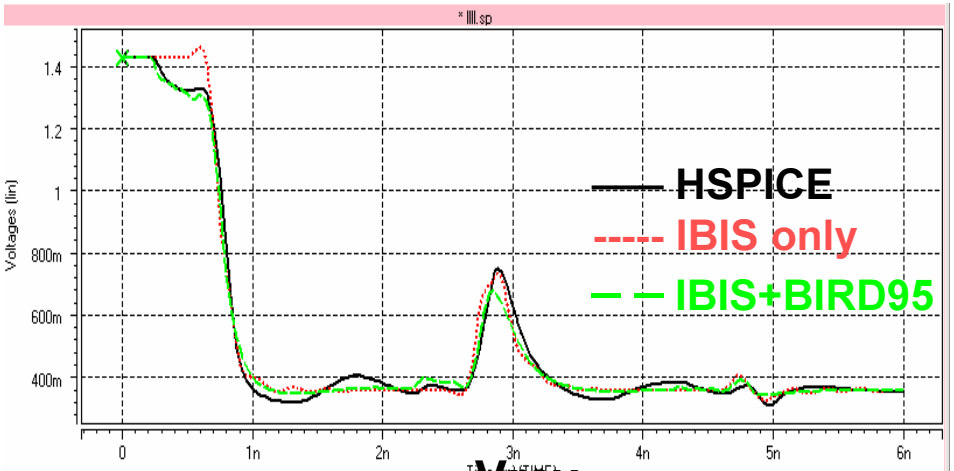
# Case with input pattern of LLLL



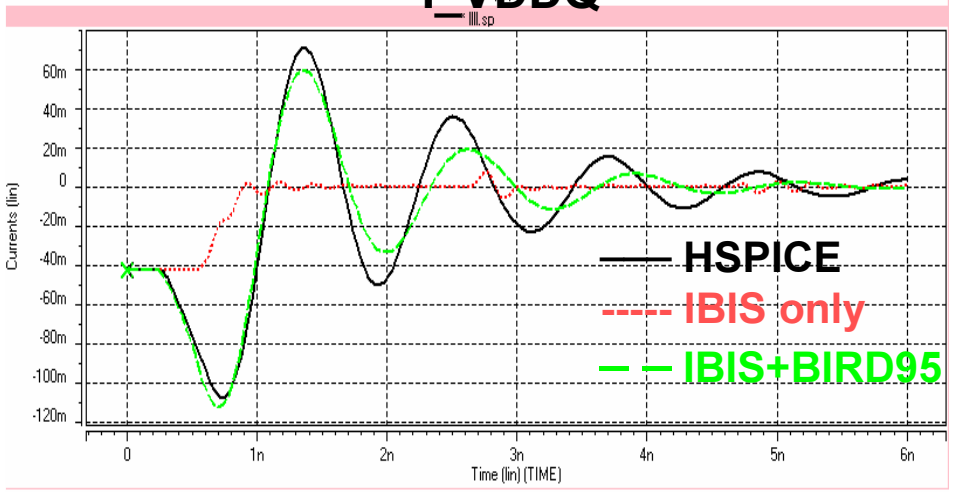
## VDDQ



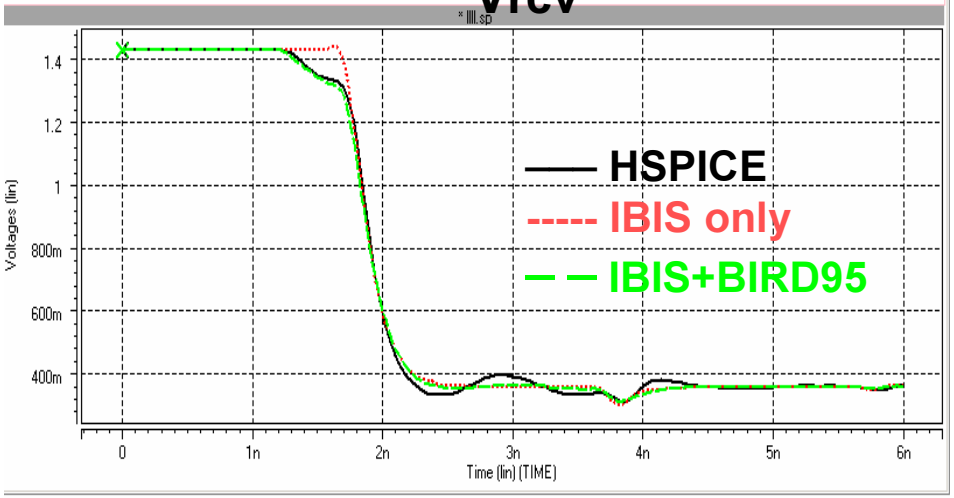

## Vpad




## I_VDDQ




## Vrcv



# Conclusions



- **Multi-buffer SSN simulation can be handled by using *BIRD95***
- **With *BIRD95*, the IBIS model matches the HSPICE model very well for all simulated cases**
- **No-ideal load can be handled well by *BIRD95***

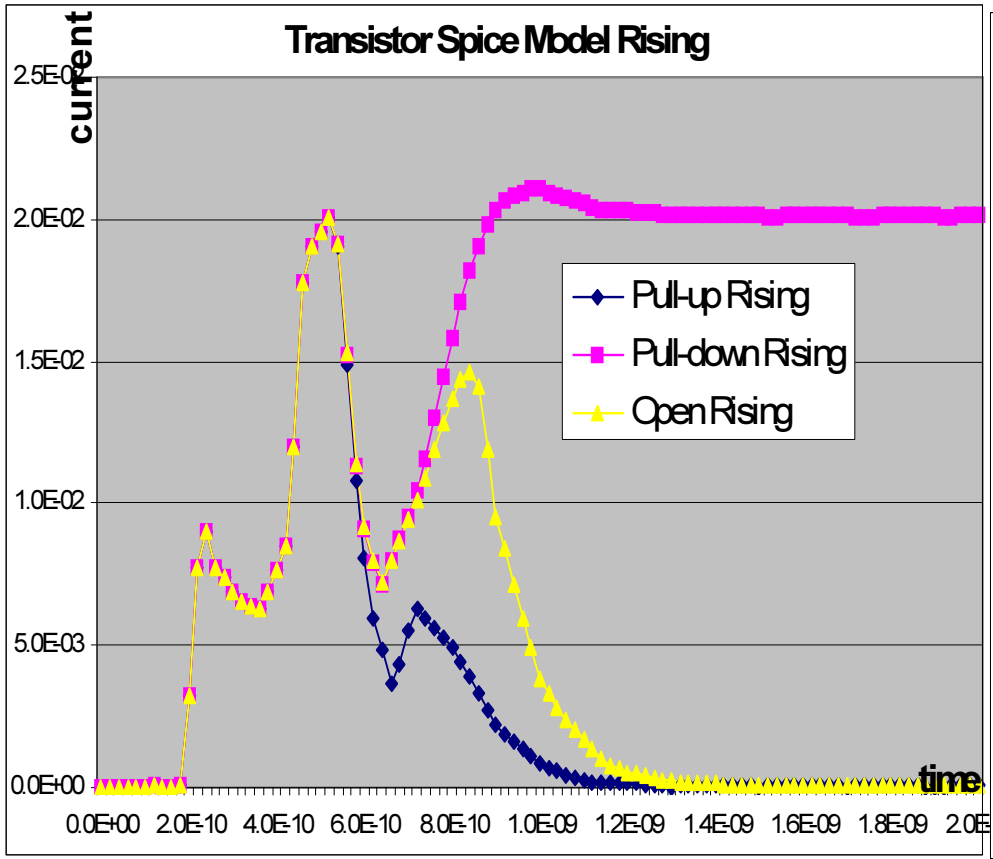
# Back up Slides

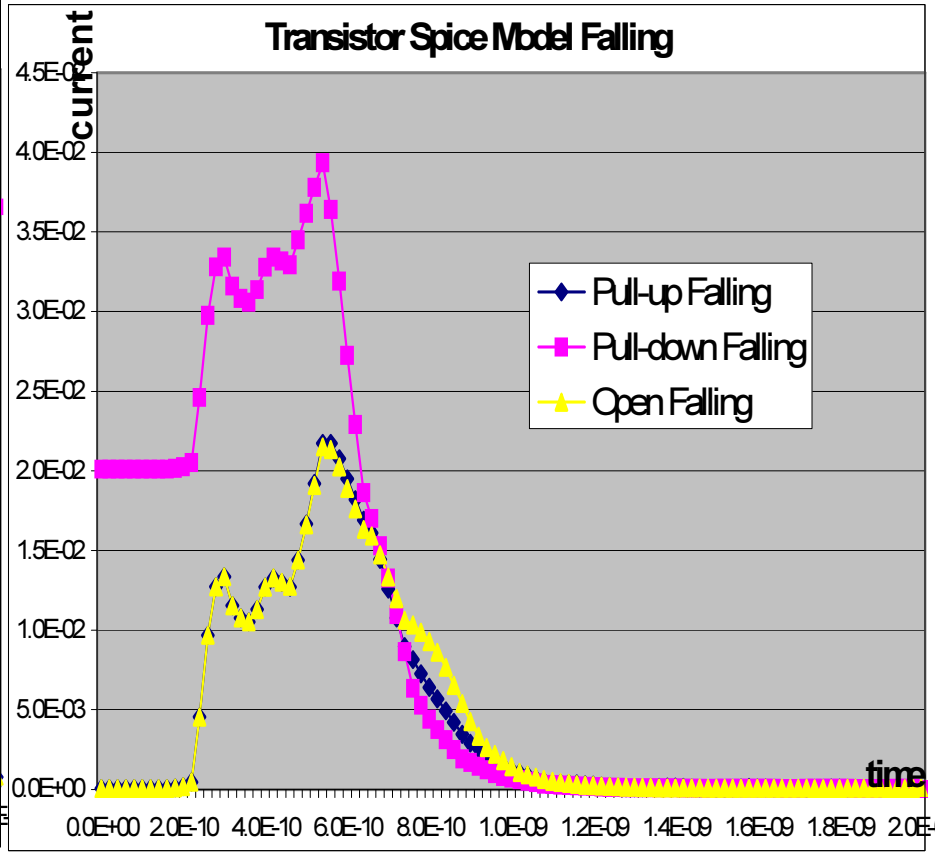


- IvsT, IvsT* and IvsT**
- What's impact of external load on IvsT, IvsT* and IvsT**

# IvsT

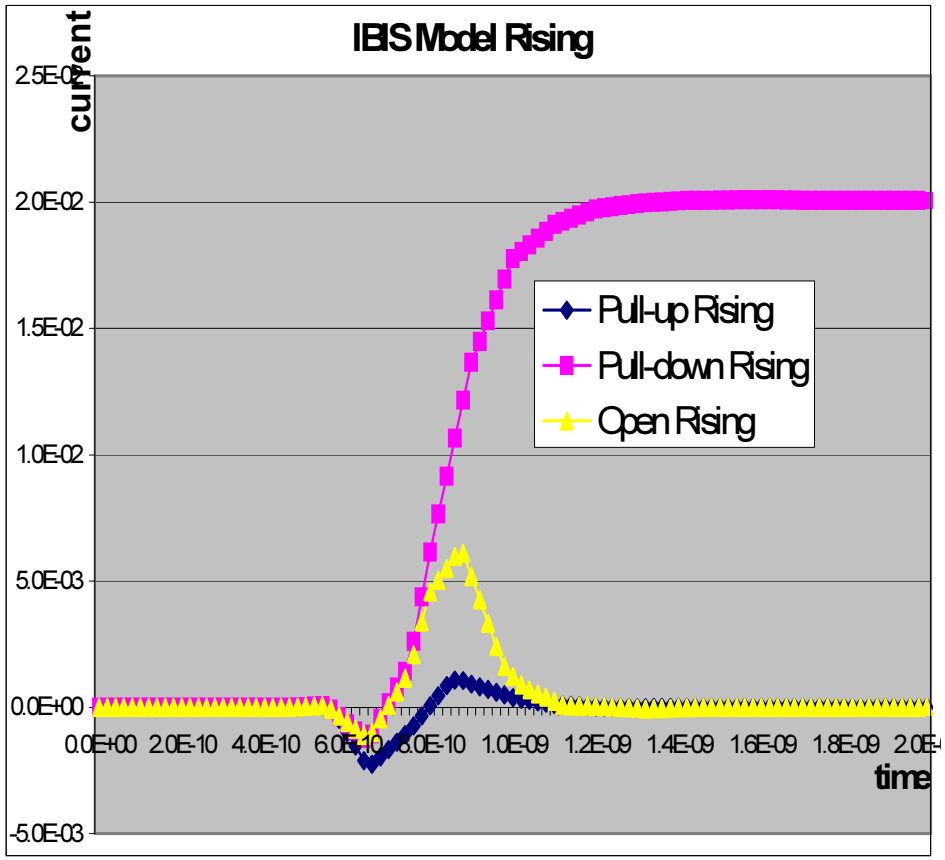


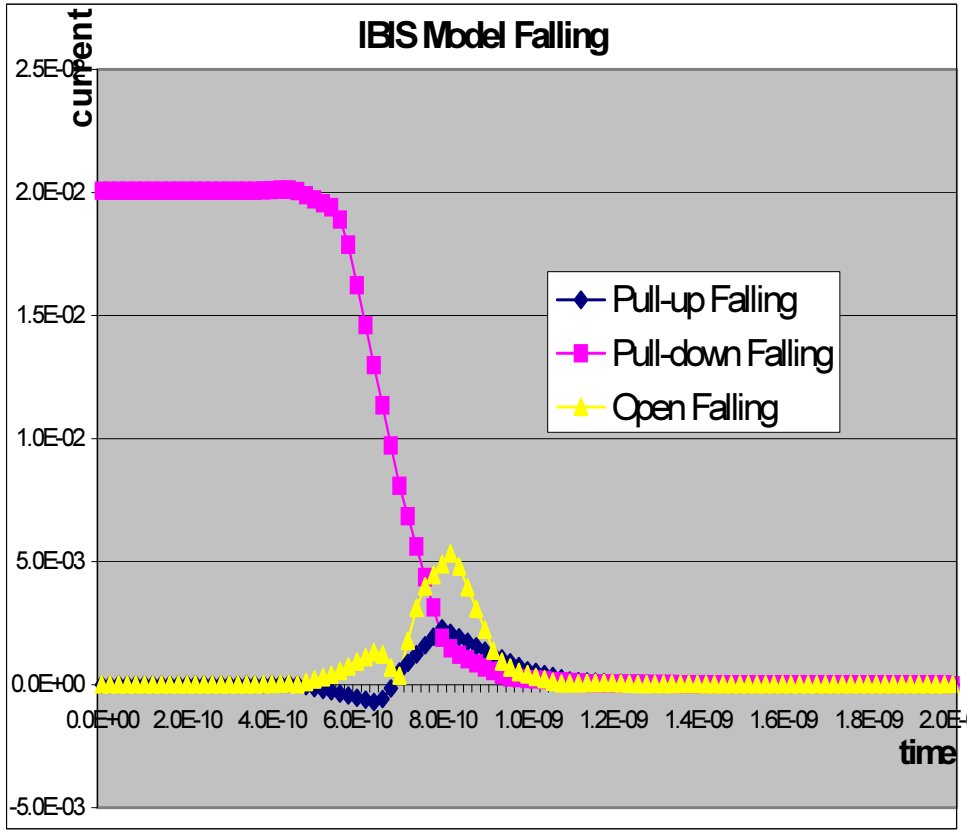


# IvsT**

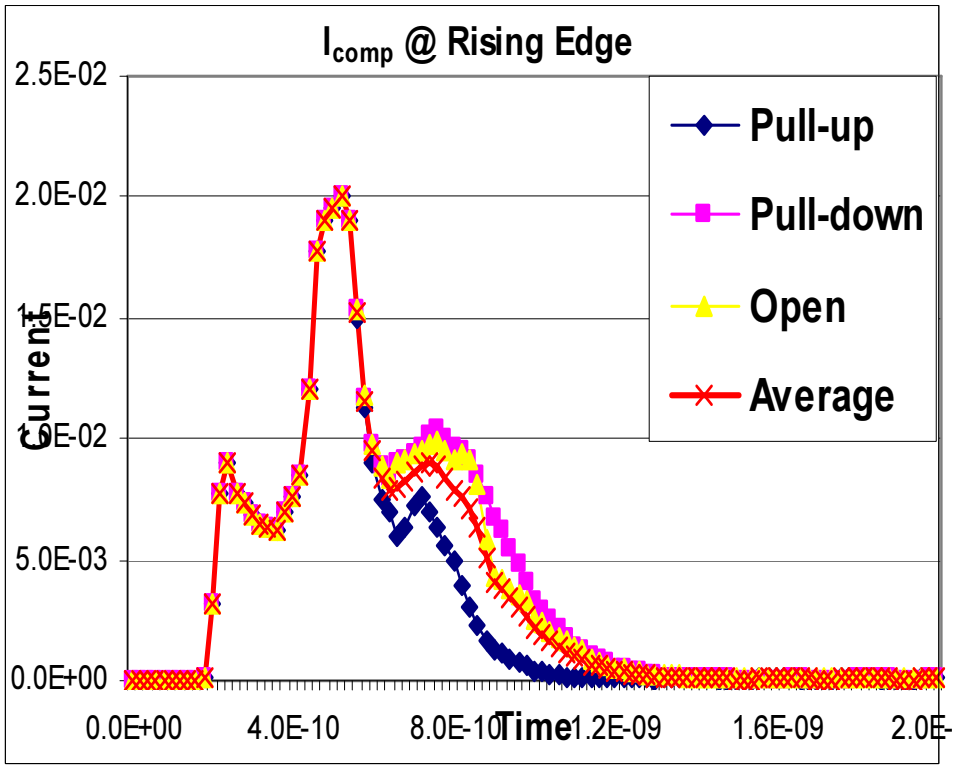


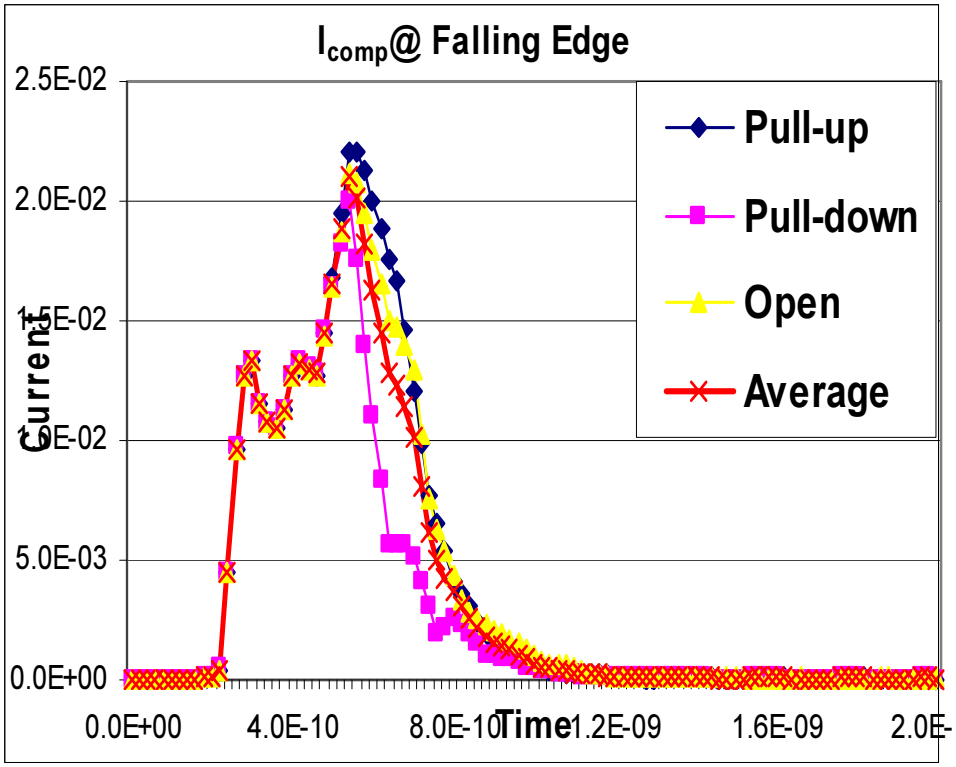


# IvsT*=IvsT-IvsT**





# Impact of external load on IvsT, IvsT* and IvsT**

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- Under ideal power supply condition, the external load has impact on IvsT, IvsT* and IvsT**.
- Since IvsT* is the difference between IvsT and IvsT**, ***BIRD95*** can compensate missed current components in existing IBIS simulators. (IvsT* and IvsT** can be different among different EDA tools)
- Under nonideal power supply condition, IvsT* can be adjust accordingly to model the first-order effects. ( RvsT, ZvsT, CvsT and similar proposal as BIRD98 can be used)
- Inaccurate loading dependent xbar current is the major reason behind the different IvsT* under different load condition. This issue can be solved by future BIRD. The new BIRD and ***BIRD95*** will not conflict since the new bird will only improve the accuracy in IvsT**.

# Questions and Answers

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