IBIS ST update

❑ 1. IBIS Development flow

- ➢ Automatic IBIS buffer production flow in place for big number of buffer in libraries.
  - reduction of V/I points to 100
  - reduction of V/t points to 100
  - comparison and adjusment of V/I and V/t end point on Rload
  - post-process to give reasonable value (cliping of reverse current)
  - post-process to correct non-motonicity for Pull-up and pull-down in clamp area
- ➢ IBIS buffer model compatible with ibis v2.1 and v3.2
- ➢ Standard IOs fully handled (LVCMOS, LVTTL, SSTL2, PCI, UDMA ...)
- ➢ Investigation on special IOs (LVDS, SATA, USB2?)

❑ 2. validation flow

- ➢ ST flow fully aligned on QualityIBIS flow (press release)
- ➢ Testcase put in place with customers (std buffer, UDMA, SSTL2)

❑ 3. ASIC IBIS model

- ➢ script is been developed to produce IBIS Asic model.
  no major requirement from customer on IBIS Asic model but only on IBIS buffer for the moment

IBIS ST highlight points

- 1. Syntax limitation
  - Difficulty to handle ST name convention with current IBIS syntax
    - file name in lower case ,
    - signal name limitation

- 2. Future requirement
  - How to handle PHY to PHY electrical validation (SATA,USB2)?
    - description of electrical model of buffer in differenet mode.
    - coherence between protocol and electrical buffer behavior
    - jitter description to track jitter propagation
    - What kind of models to insure customer validation environment (Verilog, VHDL, IBIS, cmodel ?, VHDL-AMS ?)

    - Is there any standard appear to fill this gap ?