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Buffer impedance modeling

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Outline

- Starting point - why
- Time Domain : *Capacitance vs. Voltage*
- Frequency Domain : *Capacitance & Impedance*
- NL impedance model
- Modified IBIS model
- Future work

Starting point - why

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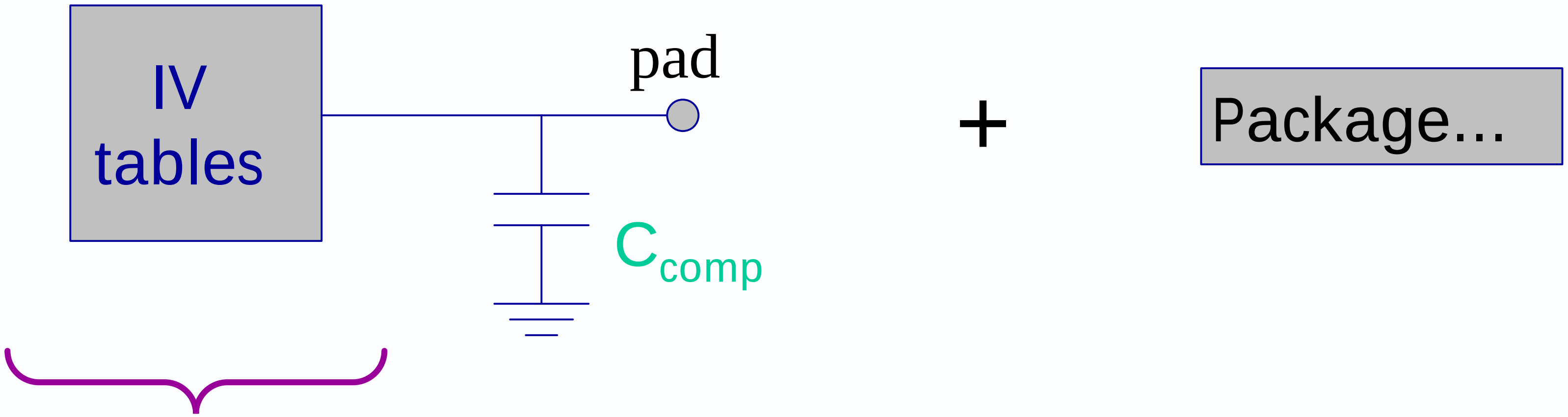
Mr. Muranyi's presentation in June 2001

(available on the IBIS website)

- Digital interconnects may be efficiently analyzed in *Frequency Domain*.

- Accurate analysis needs an accurate frequency model for drivers and receivers.

The IBIS model impedance



R(V)

$Z_{buffer,pad}$ is a shunt RC circuit, with « *R* » accounting for the whole non-linearity

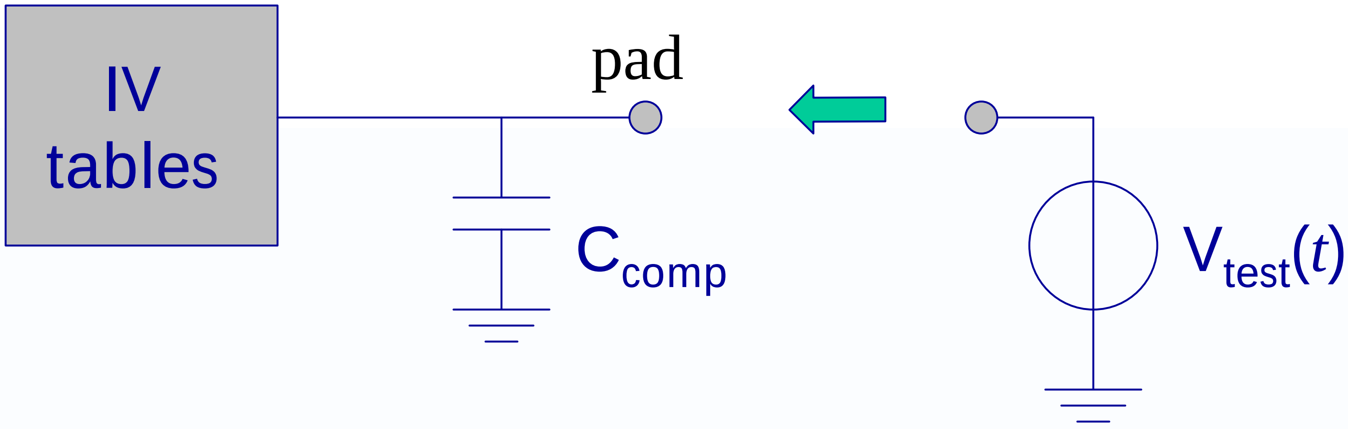
Time Domain

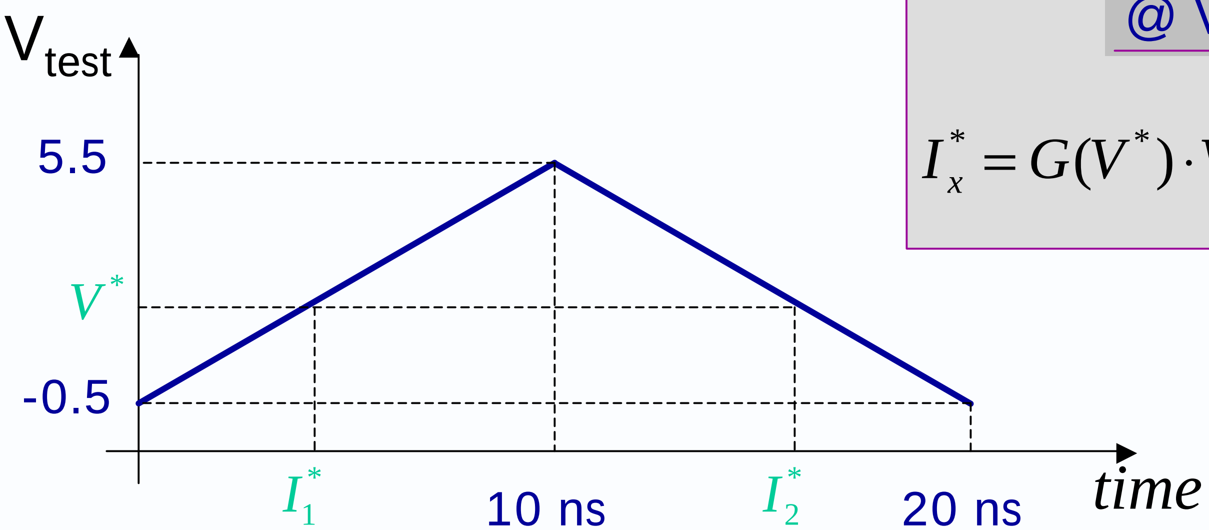
Buffer capacitance (C_{buff})

vs.

applied voltage (bias)

A "capacitance meter"





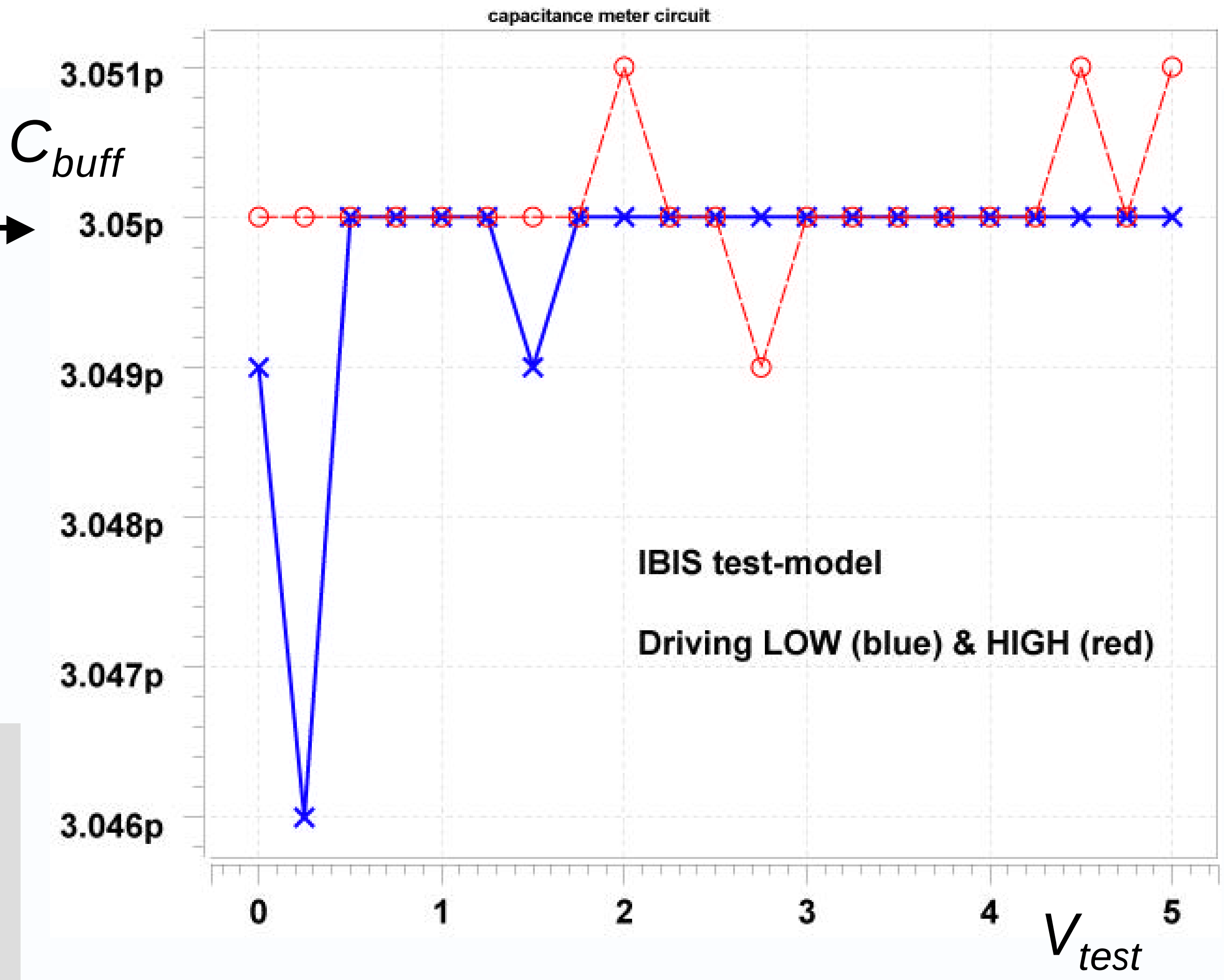
@ $V_{test} = V^*$

$$I_x^* = G(V^*)\cdot V^* + C_{buff}\cdot\frac{\Delta V}{\Delta t}$$

$$C_{buff} = \frac{I_1^* - I_2^*}{2}\cdot\frac{\Delta t}{\Delta V}$$

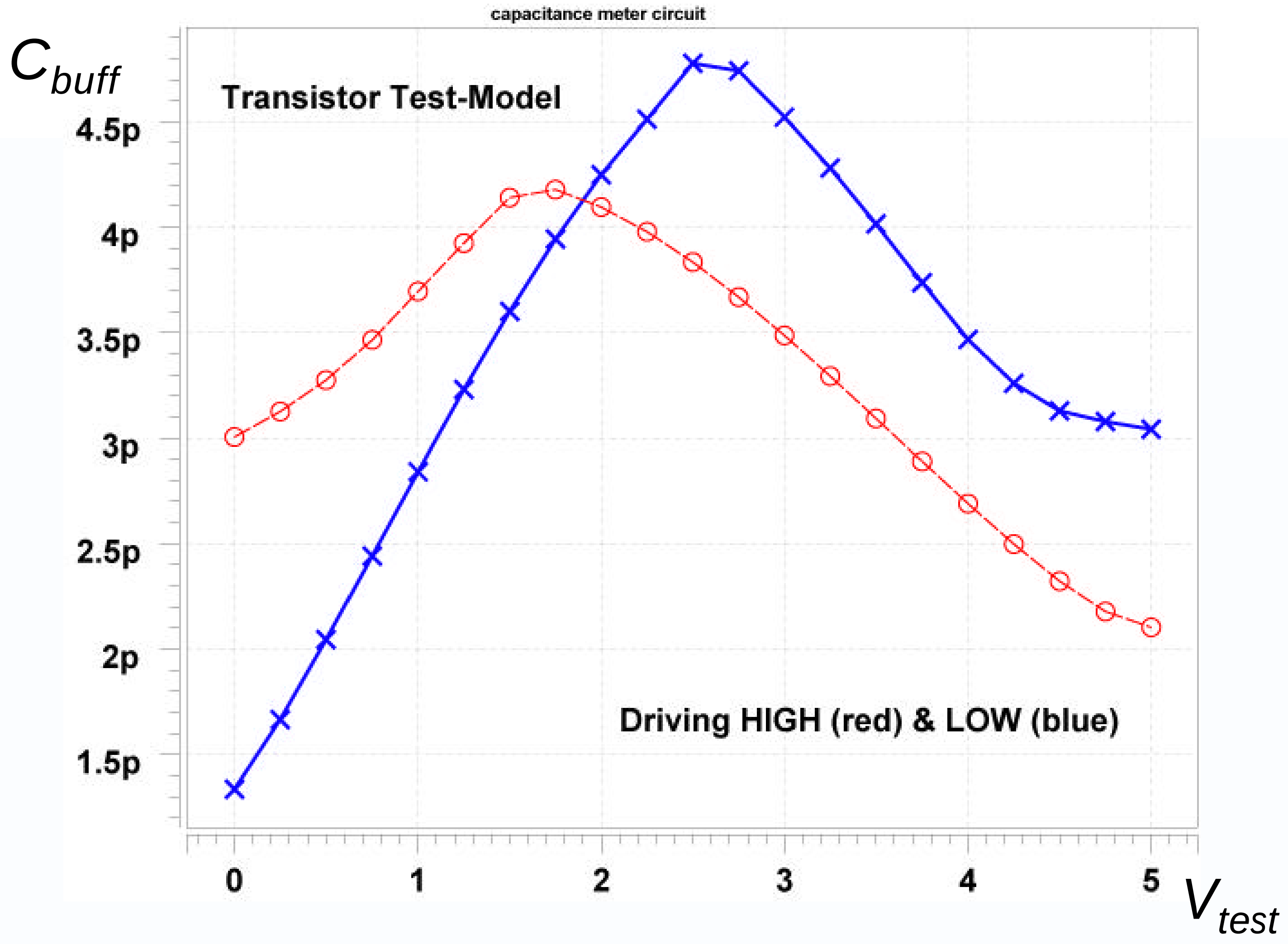
C_{buff} - IBIS model

C_{comp} = 3.05 pF



Numerical noise is due to the PWL approximation of the IV-tables

C_{buff} - Transistor model



N.B. : this transistor model is the same used to extract the data for the IBIS model in the previous slide. These two models are the ones used throughout the presentation.

Comments

- The IBIS output buffer shows a constant capacitance value vs. the applied voltage. This behaviour is consistent with the definition of the model.

- The transistor-level output buffer shows a capacitance that is strongly dependent on the applied voltage.

Frequency Domain

Z_{buffer} in Frequency Domain

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To have a better insight into the buffer impedance, let's look at it in the frequency domain.

As drivers and receivers are non-linear,
only *small-signal frequency analysis* is possible.

i.e., the buffer model is linearized around
the bias-level.

Z_{buffer} in Frequency Domain

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The output admittance of the IBIS model is :

$$Y_{out}(V,w) = \underbrace{G(V)}_{\text{IV-tables}} + \underbrace{jwC_{out}}_{C_{comp}}$$

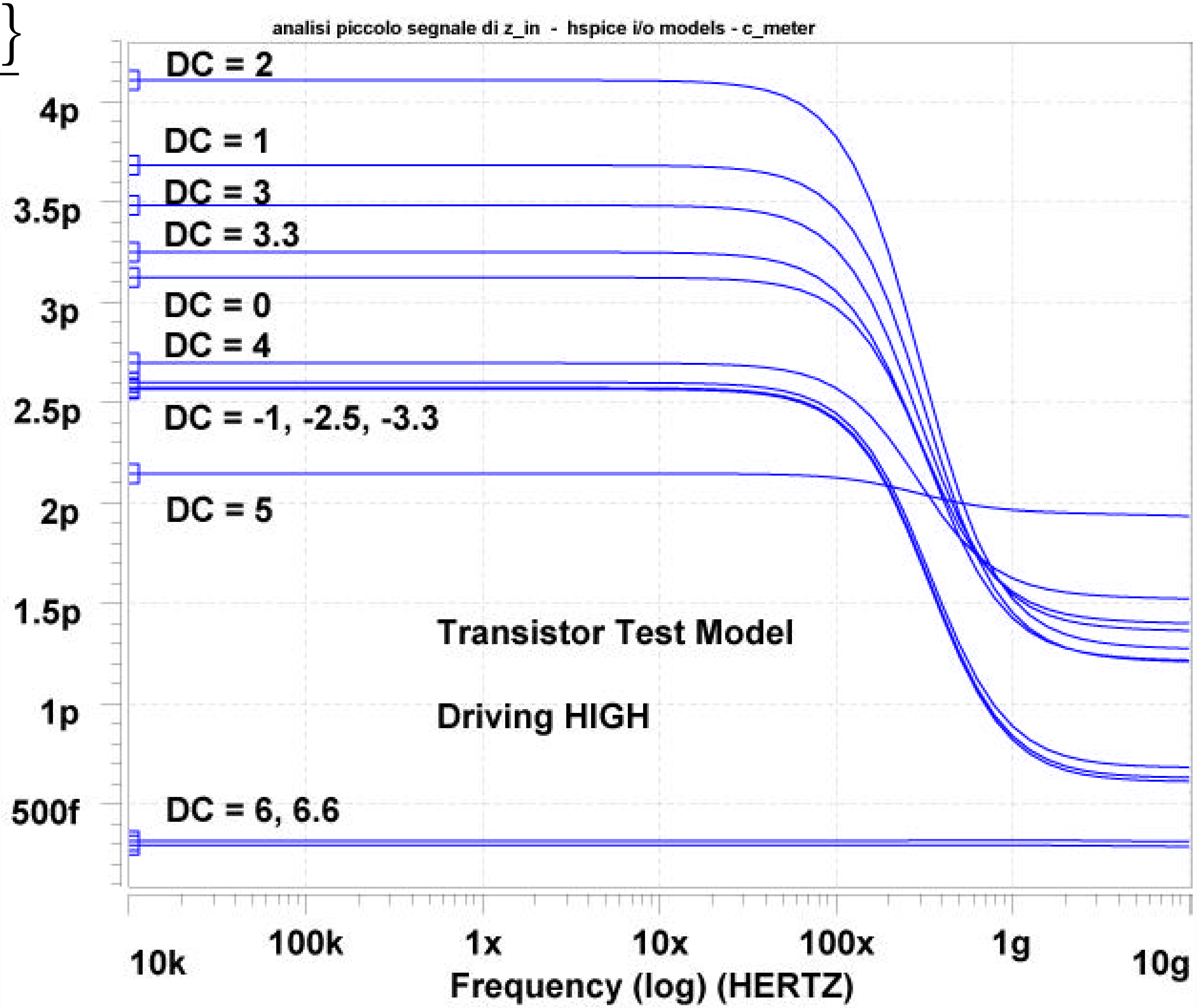
IV-tables C_{comp}

ergo :

$$C_{out} = \frac{\mathrm{Im}\{Y_{out}\}}{w}$$

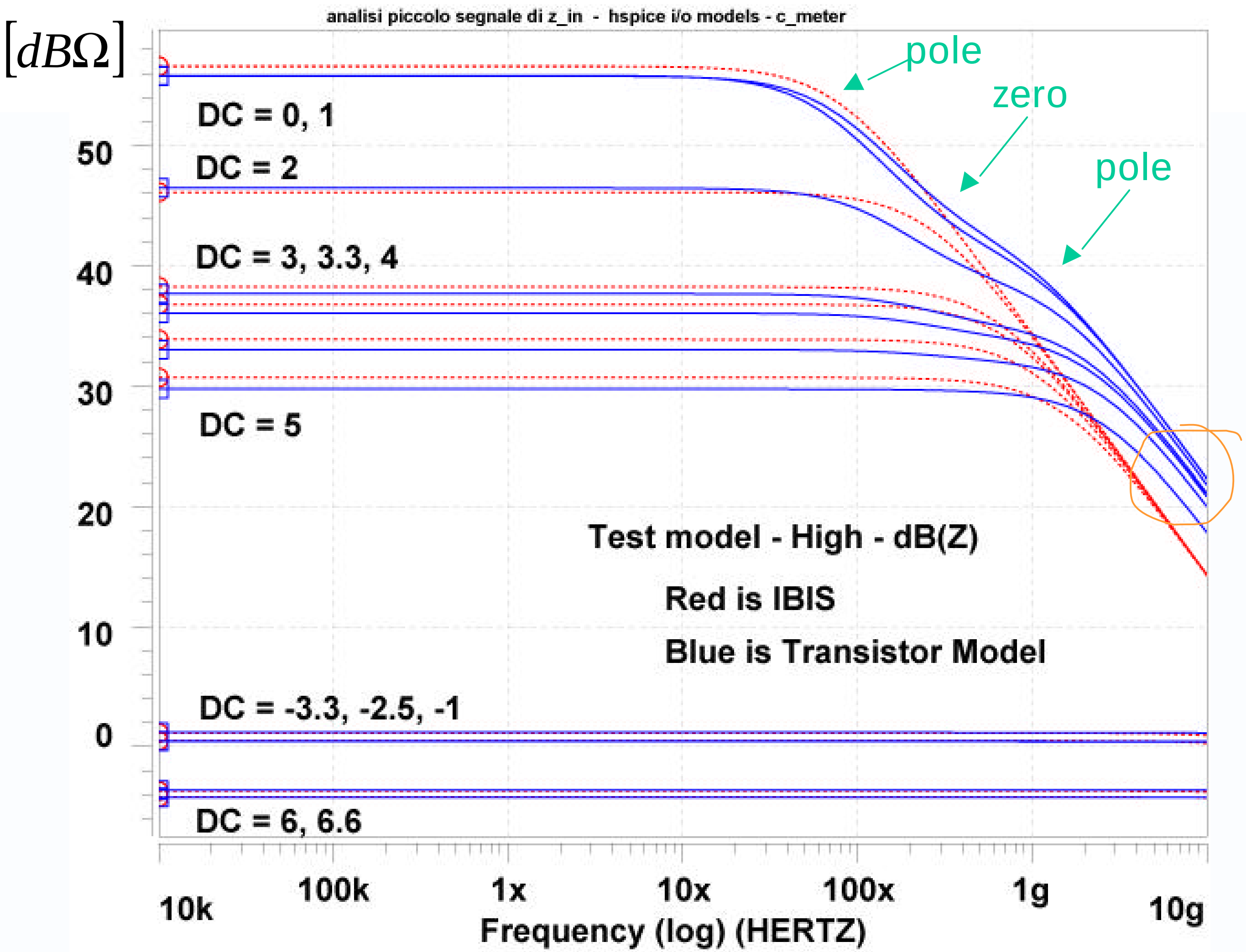
$C_{out}(f)$ - transistor model

$$\frac{\mathrm{Im}\{Y_{out}\}}{w}$$



$C_{out}(f)$ is not constant with frequency either

Z_{buffer} in dB - comparative



Red is IBIS

Blue is transistor model

HF capacitance varies with bias (for transistor model)

Z_{buffer} comparison: comments

The correlation between the impedances showed by the IBIS model and the transistor model gets poorer above 100 MHz.

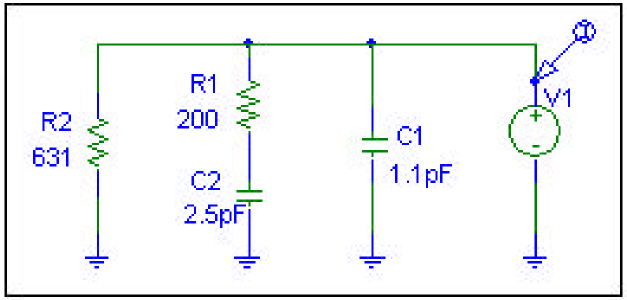
This may become relevant in high-speed designs.

Substituting

« C_{comp} »

in the IBIS model

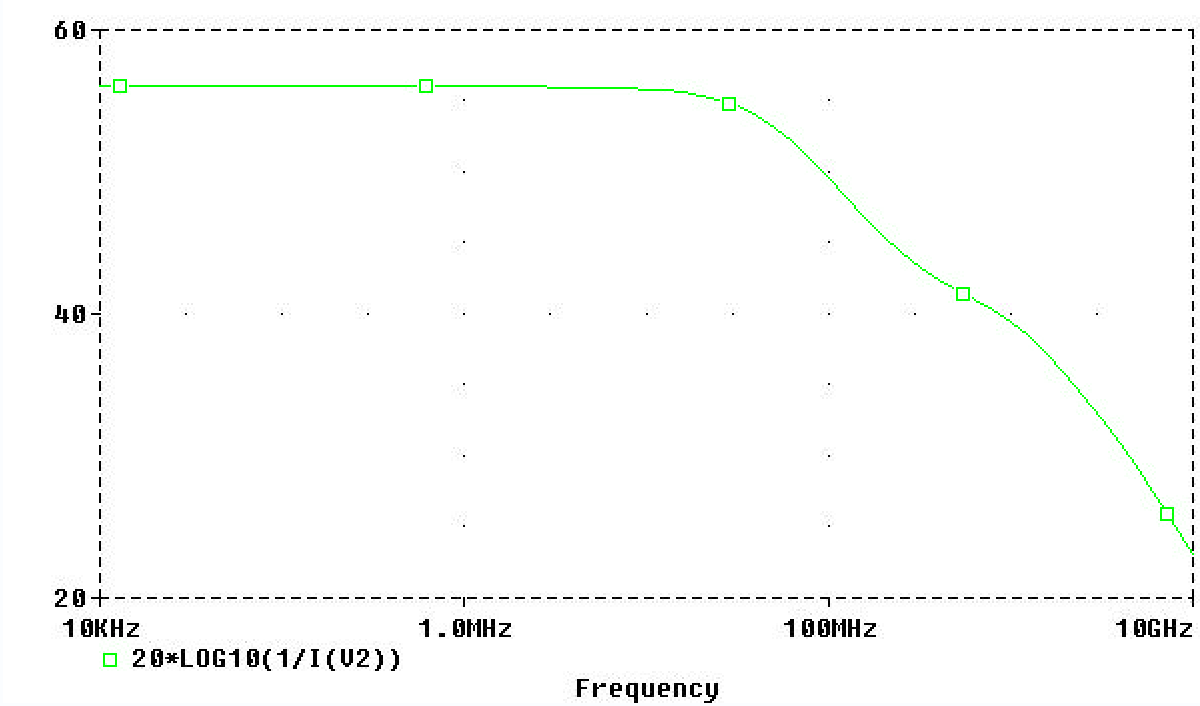
"Adding" a zero and a pole…



"small-signal" equivalent circuit

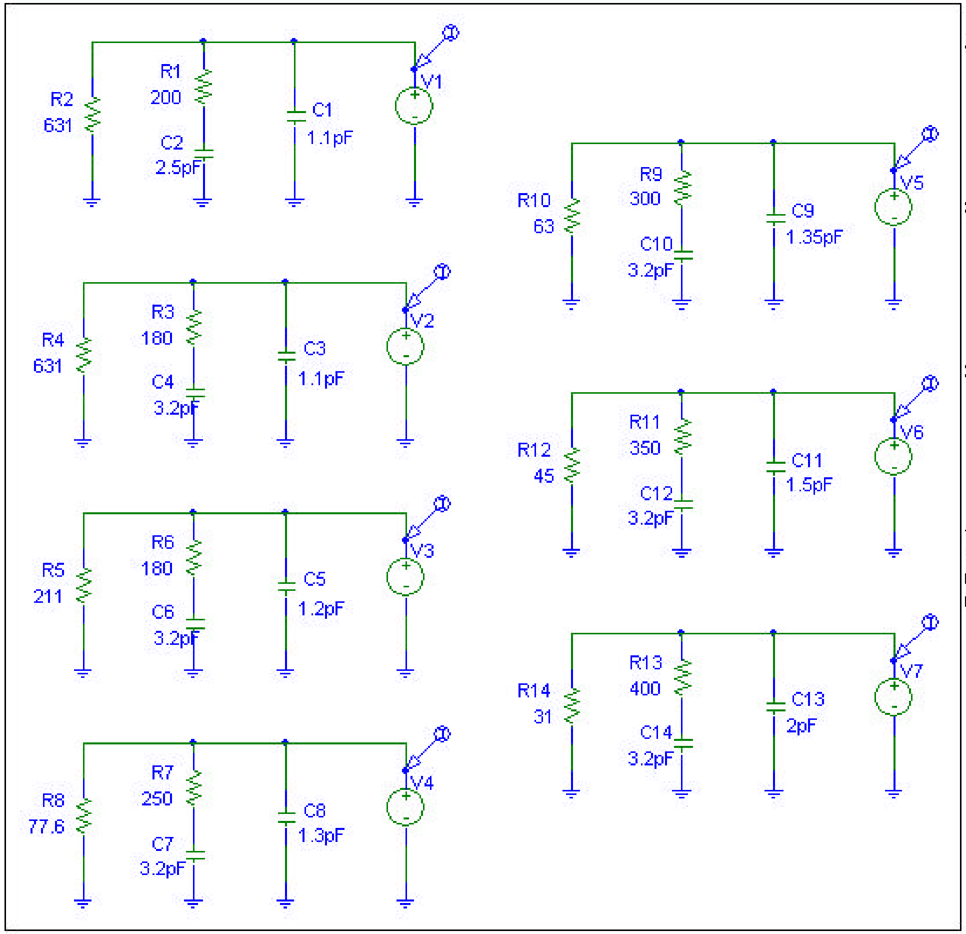
IV tables

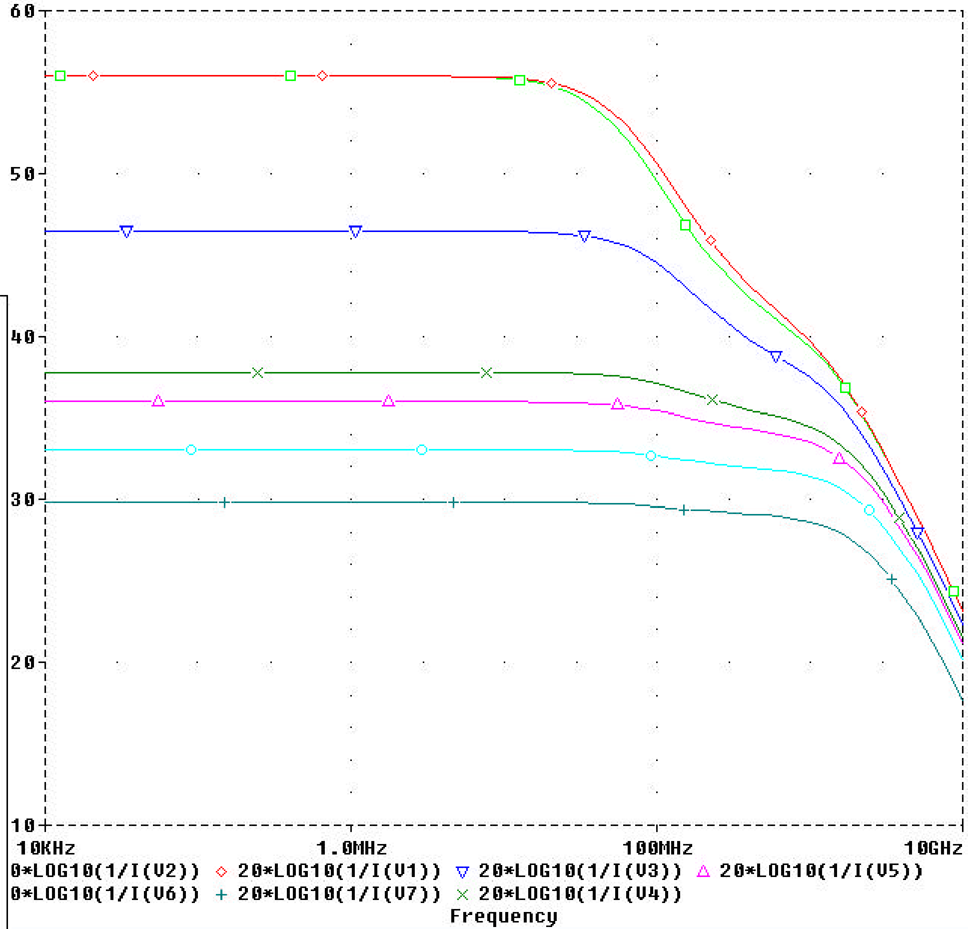
pseudo-C_{comp}



Playing with C1, R1 & C2...

... we can reconstitute the output impedance…

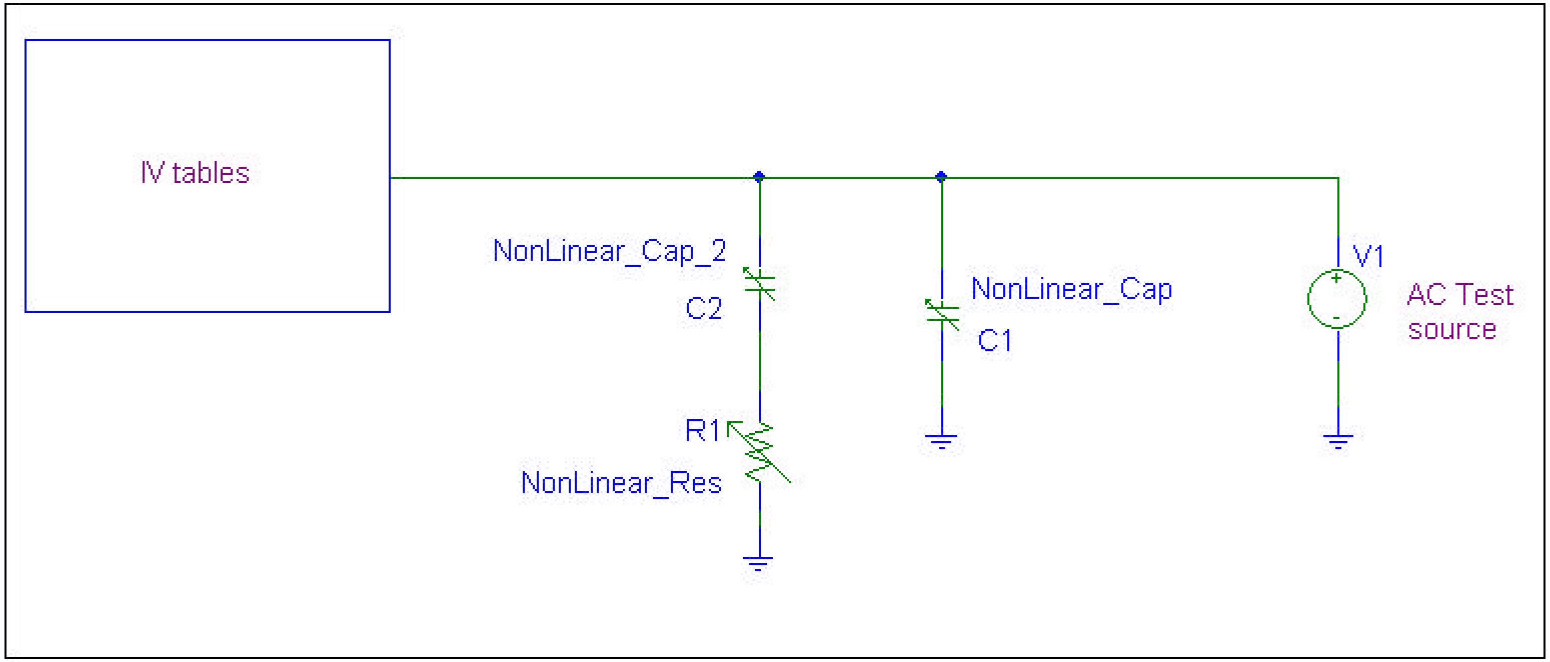




... of the transistor model at each bias level !

Spice implementation

Modifying an in-house IBIS simulator...



Spice implementation

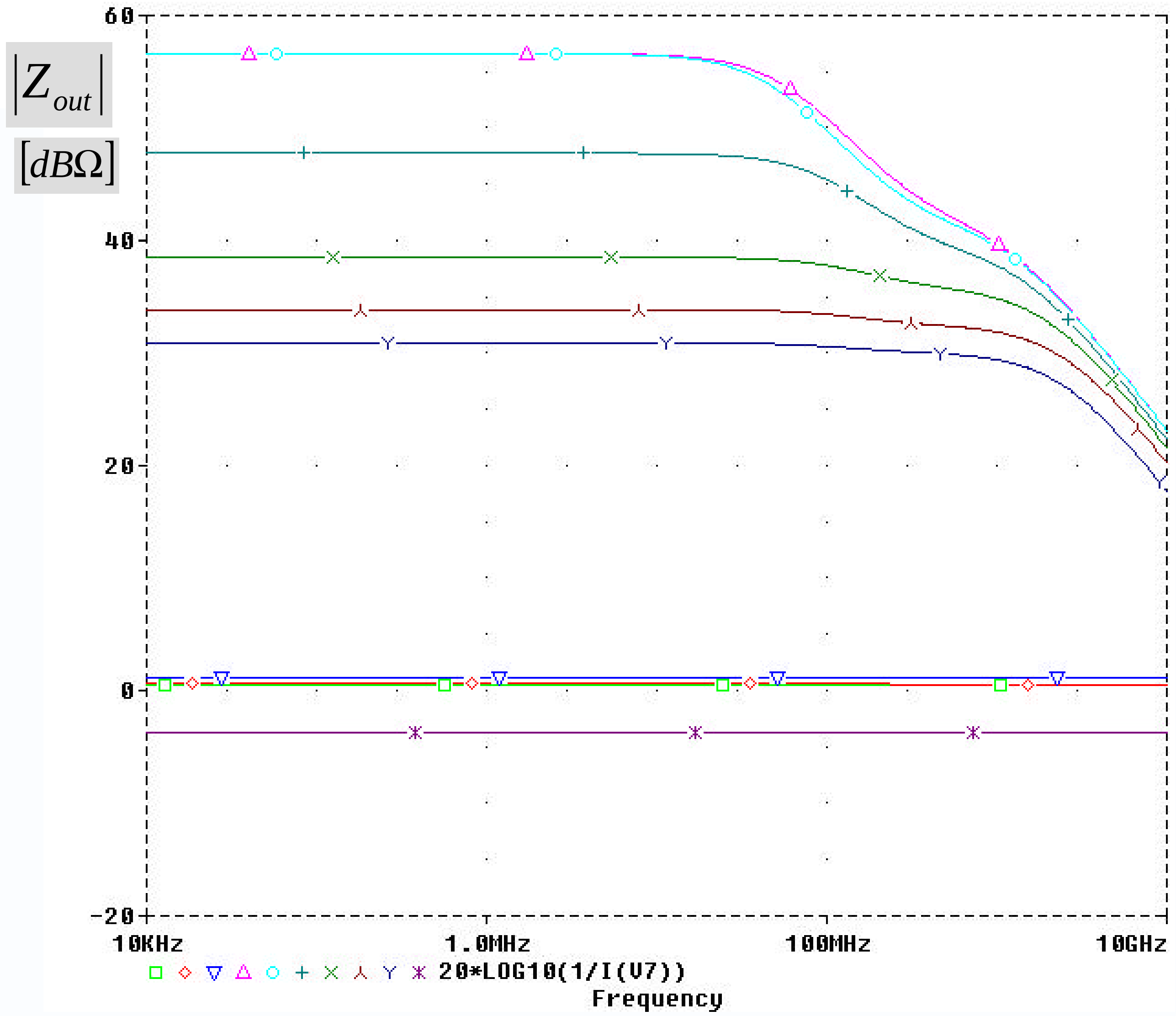
```
.subckt NonLinear_Cap 1 2
Ecopy 3 0 2 1 1.0
Vsense 0 6 0v
Cref 3 6 1e-06
Gout 1 2 VALUE = {I(Vsense)*1e06*TABLE(V(3),
**[Volt],[Farad]**
+  0 , 1.1pF,
+  1 , 1.1pF,
+  2 , 1.2pF,
+  3 , 1.3pF,
+ 3.3, 1.35pF,
+  4 , 1.5pF,
+  5 , 2pF
+ )}
.ends NonLinear_Cap
```

NL-cap

NL-resistance

```
.subckt NonLinear_Res 1 2
Gout 1 2 VALUE = {V(1,2)/TABLE(V(1,2),
**[Volt],[Ohm]**
+   0   , 200,
+   1   , 180,
+   2   , 180,
+   3   , 250,
+   4   , 300,
+   5   , 350,
+   6   , 400
+ )}
.ends NonLinear_Res
```

Spice implementation - result



A good agreement with the transistor model is achieved

Future work

- verify on other buffers and technologies (BJT,…) the ‘agreement’ with this topology

- quantify the impact in time domain

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