IBIS 4.0 – An Overview

Ralf Brüning
Michael Schäder

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Vattmannstr. 3, D-33100 Paderborn, Germany
Email: ralf.bruening@zuken.de
michael.schaeder@zuken.de

IBIS 4.0 – An Overview

- Ratified July 2002 by IBIS Open Forum.
- Incorporates changes and enhancements of 11 BIRDs:
  - Package model selection (BIRD64.4)
  - Golden Waveforms are added for single-ended and differential references (BIRD70.5).
  - Generalization of the [Series MOSFET] description (BIRD72.3).
  - Additional Fall_back Submodel_type (BIRD 73.4).
  - Subparameter additions to [Model Spec] (BIRD66, BIRD71).
  - Enhanced characterization of [Receiver Thresholds] (BIRD62.6).
  - Subparameter to split C_comp to up to four reference voltages (BIRD65.2 and BIRD76.1).
  - Clarification for [Rising/Falling Waveform] tables (BIRD68.1).
  - Increase the V-T table limit to 1000 points (BIRD67.1).

[Alternate Package Models]

[Alternate Package Models] can be used to select a package model from a list of package models.

```
[Alternate Package Models]
208p_plastic_PQFP_pkg-even_mode | What more can be said here?
208p_plastic_PQFP_pkg-odd_mode  | It's all in the name.
208p_ceramic_PQFP_pkg-even_mode | More comments here.
208p_ceramic_PQFP_pkg-odd_mode  | And some more here too.
[End Alternate Package Models]
```

(Example from IBIS 4.0 specification)

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Golden Waveform [Test Data]

[Test Data] The VT data provides a **golden waveform** showing how the IC should respond to a known load.

An IBIS file may contain any number of [Test Data] sections representing different driver and load combinations.

Golden Waveforms are reference waveforms derived from transistor-level simulations using known ideal test loads.

They are useful in verifying the accuracy of behavioral simulations against the transistor-level model from which the IBIS model parameters originated.

(Example from IBIS 4.0 specification)

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Generalization of [Series MOSFET]

The IBIS FET Bus Switch model assumes a series NMOS FET which has its gate tied to Vdd. We have come across two other topologies for the FET switches, specifically:

1. What appears to be a PMOS device with it's gate tied to ground
2. Parallel NMOS and PMOS devices with gates respectively tied to Vdd and ground.

The IBIS Golden Parser produces warnings and errors with models that describe this behaviour. (Excerpt from BIRD 72.3)

The IBIS 4.0 now supports a generalized [Series MOSFET] description that resolves both issues named in BIRD 72.3.

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Additional Submodel_type Fall_back

[Submodel] is used to define a submodel and its attributes.

Former submodels had a trigger for turning on functions (Bus_hold and corresponding active terminators and Dynamic_clamp functions).

Another mechanism to turn off submodels is needed for AVC type devices which have the overall driver strength reduced after the output passes through a voltage threshold value.

The new submodel operates similar to the Bus_hold submodel, but with opposite action. The trigger turns off a submodel (presumed on) when the output die voltage passes through a trigger threshold.

The total effective die capacitance including the submodel contributions are provided in the top-level model.

Changes and Additions to [Model Spec]

The following additional subparameters are added to the [Model Spec] keyword:

Parameter	Description
Cref	Timing specification capacitive load
Rref	Timing specification resistance load
Cref_rising/ Cref_falling	Timing spec. capacitive load for rising/falling edges
Rref_rising/ Rref_falling	Timing spec resistance load for rising/falling edges
Vref_rising/ Vref_falling	Timing spec test load voltage for rising/falling edges
Vmeas_rising/ Vmeas_*falling*	Meas. voltage for rising/falling edge timing measurements

[Receiver Thresholds] Single Ended

Required single ended receiver threshold parameters:

Parameter	Description
Vth	ideal input threshold voltage at which the output of a digital logic receiver changes state
Vinh_ac	voltage that a L-to-H going input wvfrm must reach to ensure that the receiver's output has changed state
Vinh_dc	voltage that an input wvfrm must remain above to ensure that a receiver's output will not change state
Vinl_ac	voltage that a H-to-L going input wvfrm must reach to ensure that the receiver's output has changed state
Vinl_dc	voltage that an input wvfrm must remain below to ensure that a rec. output will not change state
Tslew_ac	*absolute time difference between the points at which an input wvfrm crosses Vinl_ac and Vinh_ac*

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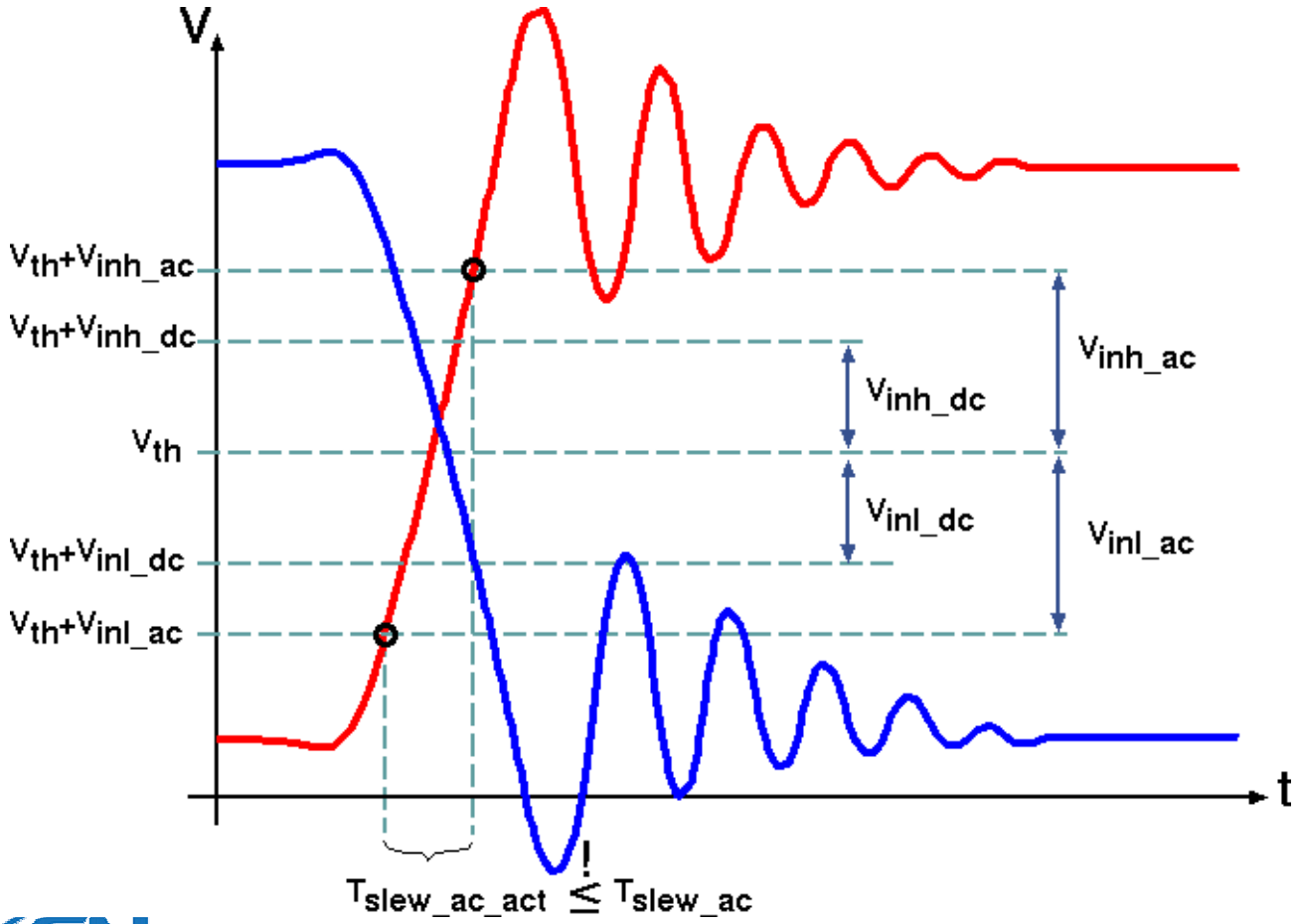
Vin[hl]_[ad]c is expressed as an offset from Vth.

[Receiver Thresholds] Single Ended

Required single ended receiver threshold parameters:
Vth, *Vinh_ac*, *Vinh_dc*, *Vinl_ac*, *Vinl_dc*, and *Tslew_ac*



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[Receiver Thresholds] Single Ended

Optional single ended receiver threshold parameters:

Parameter	Description
Vth_min	minimum input threshold voltage at 'typ' conditions
Vth_max	maximum input threshold voltage at 'typ' conditions
Threshold_sensitivity	specifies how Vth varies with respect to the supply voltage
Reference_supply	indicates which supply voltage Vth* tracks; legal arguments are *Power_clamp_ref, Gnd_clamp_ref, Pullup_ref, Pulldown_ref, Ext_ref*

[Receiver Thresholds] Single Ended

Threshold_sensitivity is defined as:

$$\text{Threshold\_sensitivity} = \frac{\text{change in input threshold voltage}}{\text{change in referenced supply voltage}}$$

Vth at minimum or maximum operating conditions:

$$\text{Vth(min/max)} = \text{Vth*} + \text{Threshold\_sens.} * \text{change\_in\_supply\_voltage}$$

with *Vth* = (Vth_min | Vth_max)*

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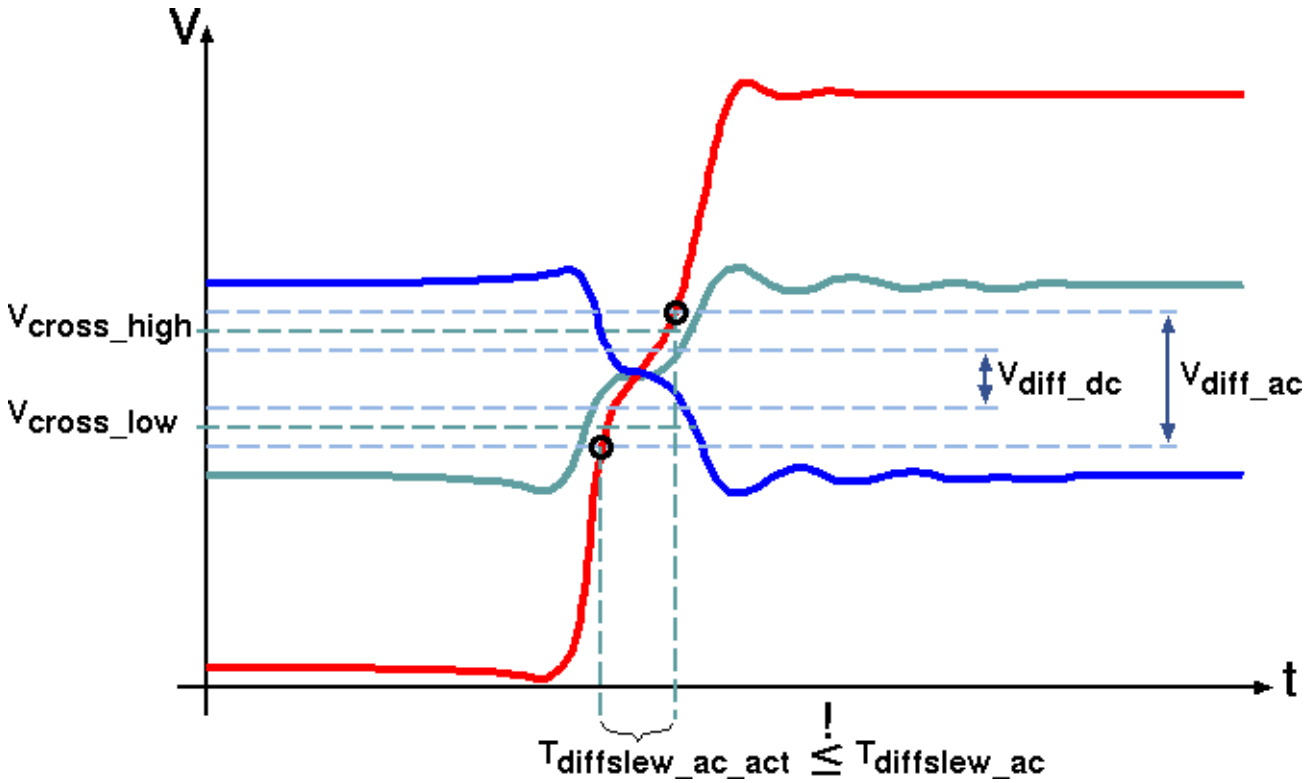
[Receiver Thresholds] Differential

The following parameters apply for differential receivers:

Parameter	Description
Vcross_low	least positive voltage at which a differential receivers' input signals may cross while switching
Vcross_high	most positive voltage at which a differential receivers' input signals may cross while switching
Vdiff_dc	minimum voltage difference that guarantees the receiver will not change state
Vdiff_ac	minimum voltage difference that guarantees the receiver will change state
Tdiffslew_ac	the absolute difference in time needed to transcend Vdiff_ac

[Receiver Thresholds] Differential

Required differential receiver threshold parameters: *Vcross_high, Vcross_low, Vdiff_dc, Vdiff_ac*, and *Tdiffslew_ac*



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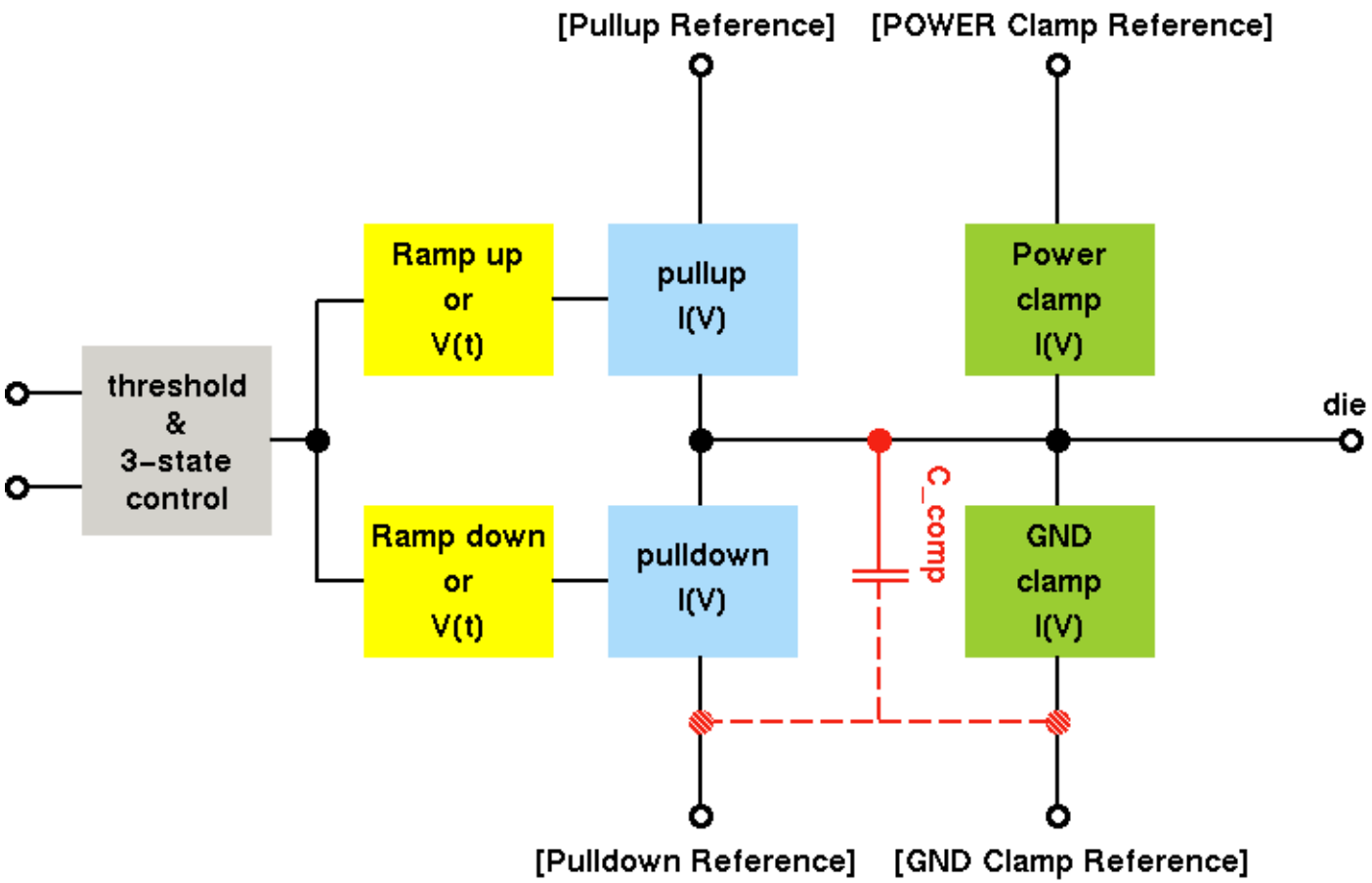
Splitting of C_comp in [Model] Statement

Former IBIS Model Structure:



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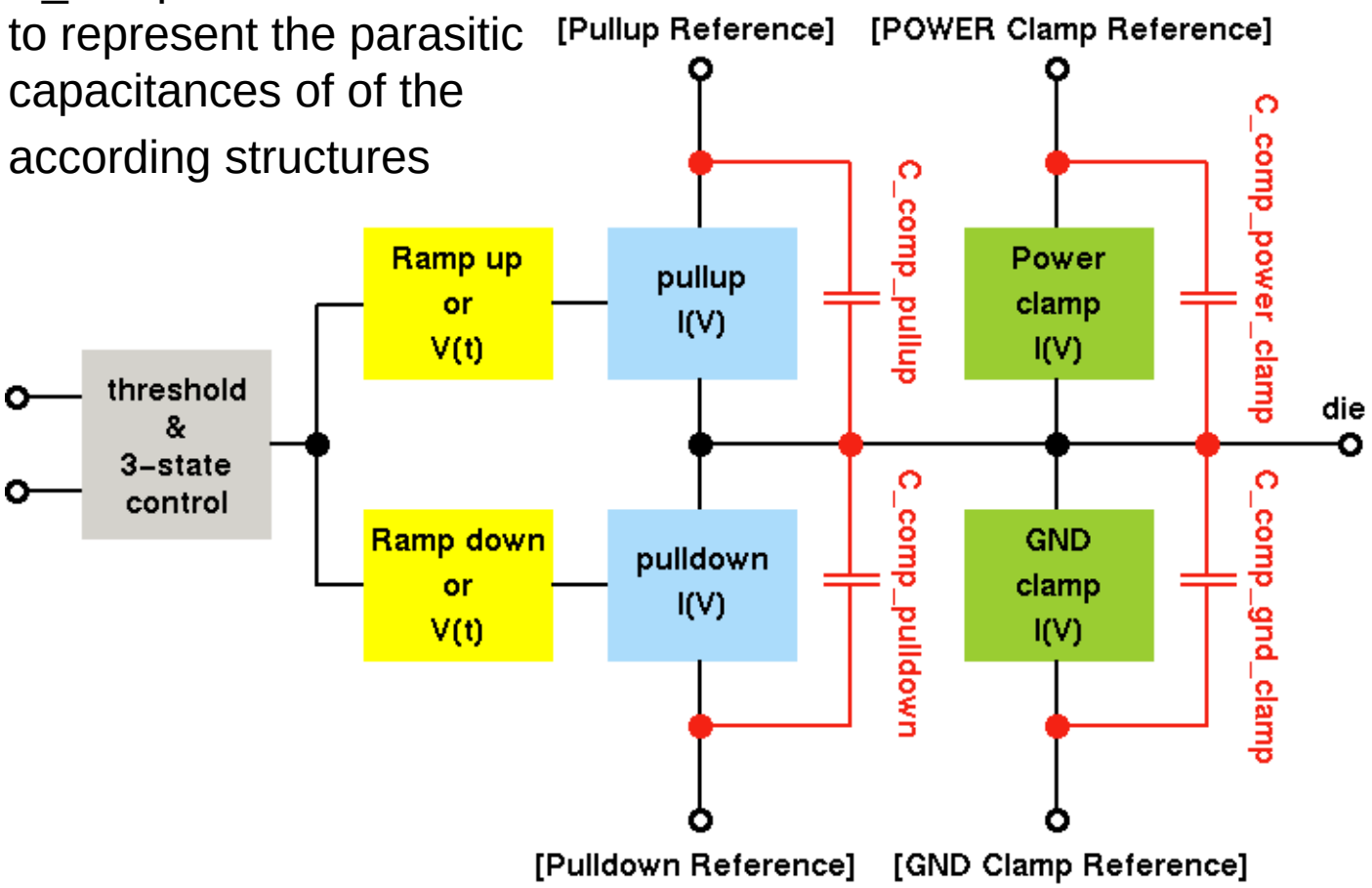
Splitting of C_comp in [Model] Statement

IBIS 4.0 Model Structure:

C_comp* are intended to represent the parasitic capacitances of of the according structures



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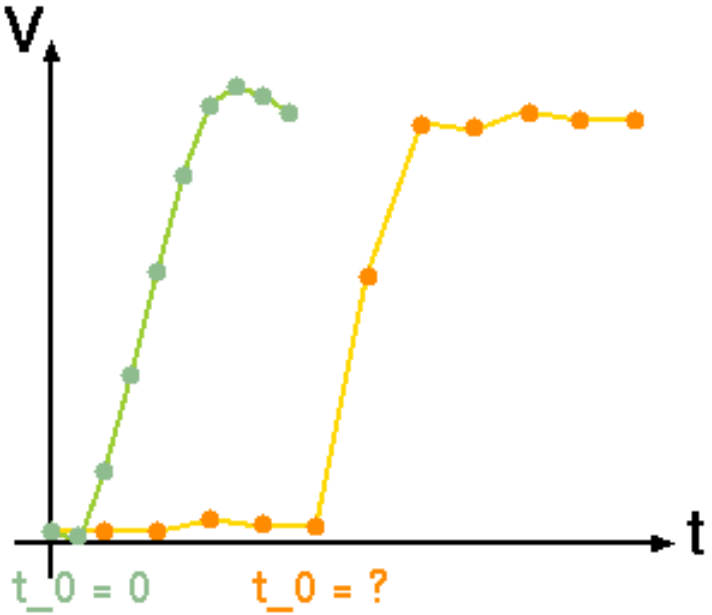
Clarification of [Rising/Falling Waveform]

Rising waveform data should be correlated with falling waveform data to help simulators provide accurate duty cycles for their output waveforms. (BIRD 68.1)



In addition,1000 points allowed in V-t table now (BIRD67.1)

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