Mπlog, Macromodeling via Parametric Identification of Logic Gates

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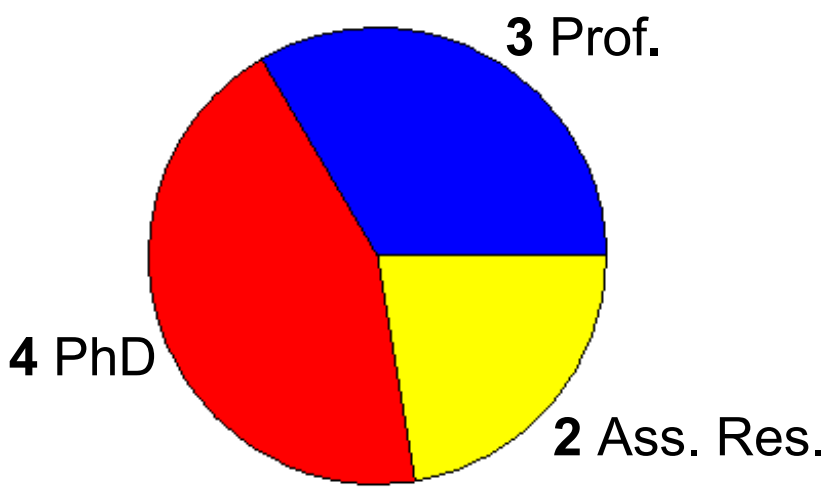


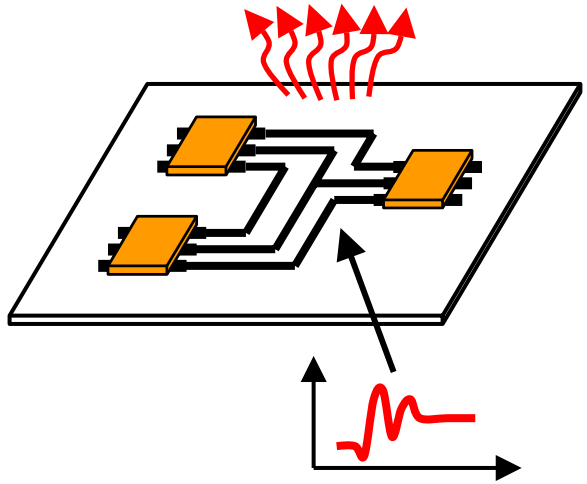
Research

Modeling of devices, interconnects and discontinuities in high-speed information and communication systems.

Collaborations:

- IBM (USA+GE)
- INTEL (USA)
- CST (GE)

Background



High Performance simulation requirements

- Very accurate timing
- Power-supply voltage variation effects
- Temperature effects

- Transistor-level models are not affordable (computation + structure disclosure)
- *Classic* IBIS models not always adequate

→ Complementary Approach

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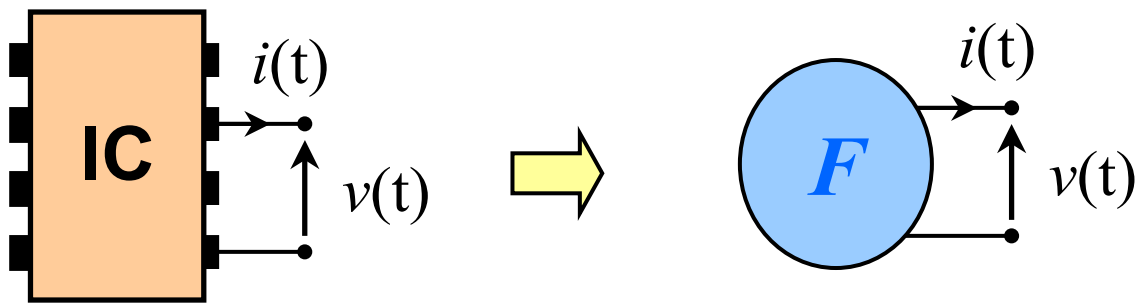
Mπlog (i)

Macromodeling via **P**arametric
Identification (π) of **LO**gic **G**ates

What is it ?

A **mathematical expression** reproducing the electrical behavior of the device



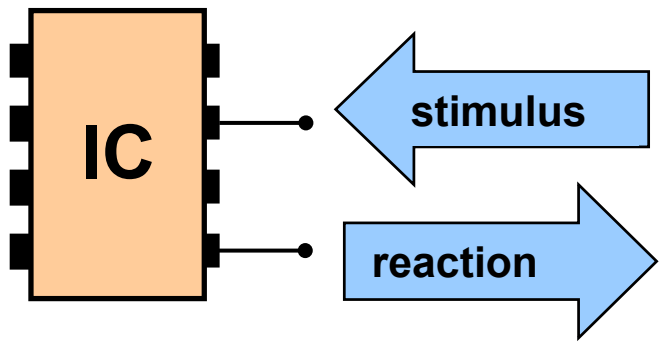
$$i = F(v,\ d/dt)$$

Nonlinear dynamic relationship

Mπlog (ii)

How does it work ?

- Real Device (or its physical model) is conveniently **stimulated**
- **Reaction** **(port transient responses)** is used to build the model



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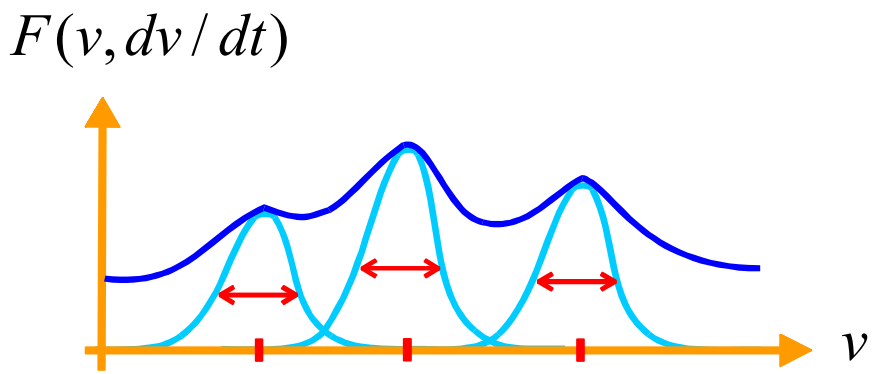
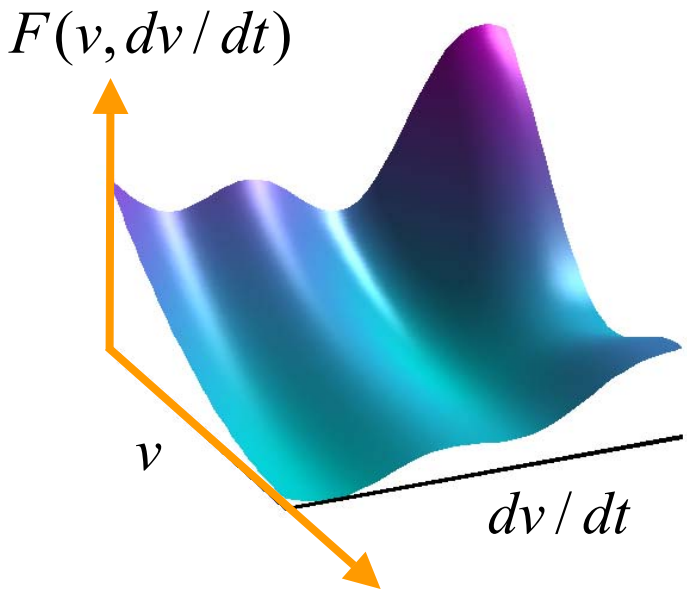
Mπ*log*: what is the output ?

Model structure: F is a Σ nonlinear Gaussian **R**adial **B**asis **F**unctions **(RBF)**

e.g., $$i = -a_1 \exp\{- v^2/a_2\} + a_3 \exp\{-(dv/dt)^2\}$$



unknown parameters: **amplitude, position, spreading**

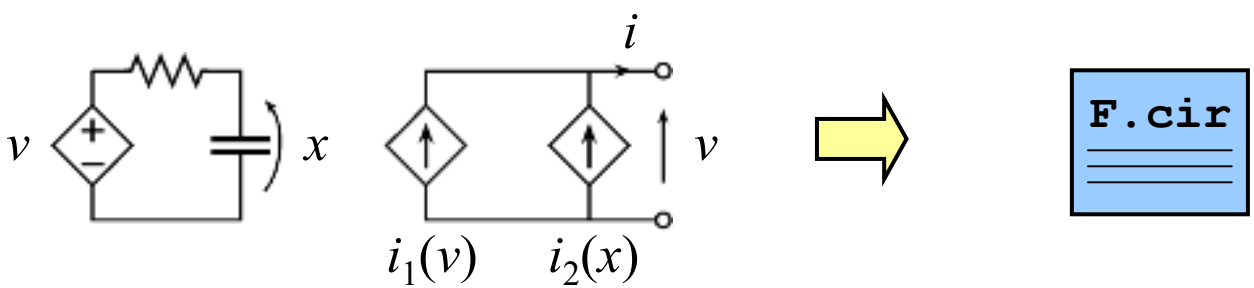


Mπlog: implementation

$$i = -a_1 \exp\{- v^2/a_2\} + a_3 \exp\{-(dv/dt)^2\}$$

(a) DIRECT EQUATION DESCRIPTION/IMPLEMENTATION

(b) CIRCUIT INTERPRETATION & SPICE IMPLEMENTATION



(Compatible with IBIS MULTI-LINGUAL Model Support, BIRD #75.8)

Mπ*log* applications

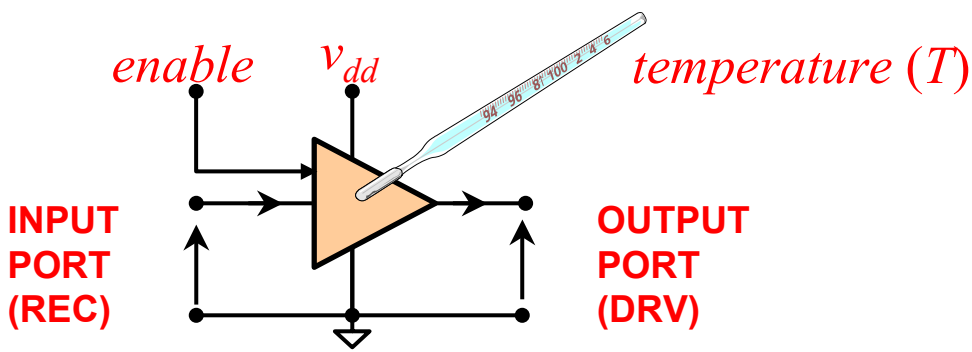
- **Basic macromodels** of Input and Output ports

  [I.S.Stievano, F.G.Canavero, I.A.Maio, "Parametric Macromodels of Digital I/O Ports," IEEE Trans. on Advanced Packaging, Vol. 25, No. 2, pp. 255-264, May 2002]

- Inclusion of slowly-varying **device parameters** (eg, **temperature**)
- Inclusion of the **power-supply voltage** variation
- models of the **power supply port**
- models of **tristate drivers**

  [I.S.Stievano, F.G.Canavero, I.A.Maio, "Mπ*log*," Proc. Of the 4th Annual IBM CAS Conference, Austin, TX, Feb. 21, 2003]

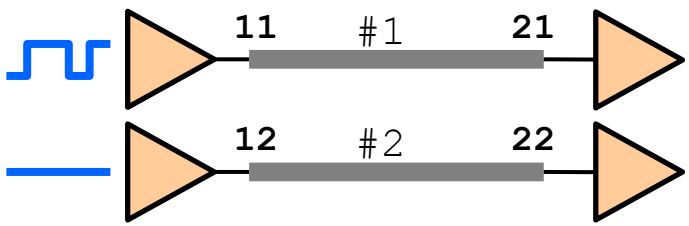
Following examples are based on a high-speed IBM CMOS transceiver ($V_{dd} = 1.8$ V)



Example #1: basic devices

High-speed interconnection system with (*Z-Series*) IBM I/O ports

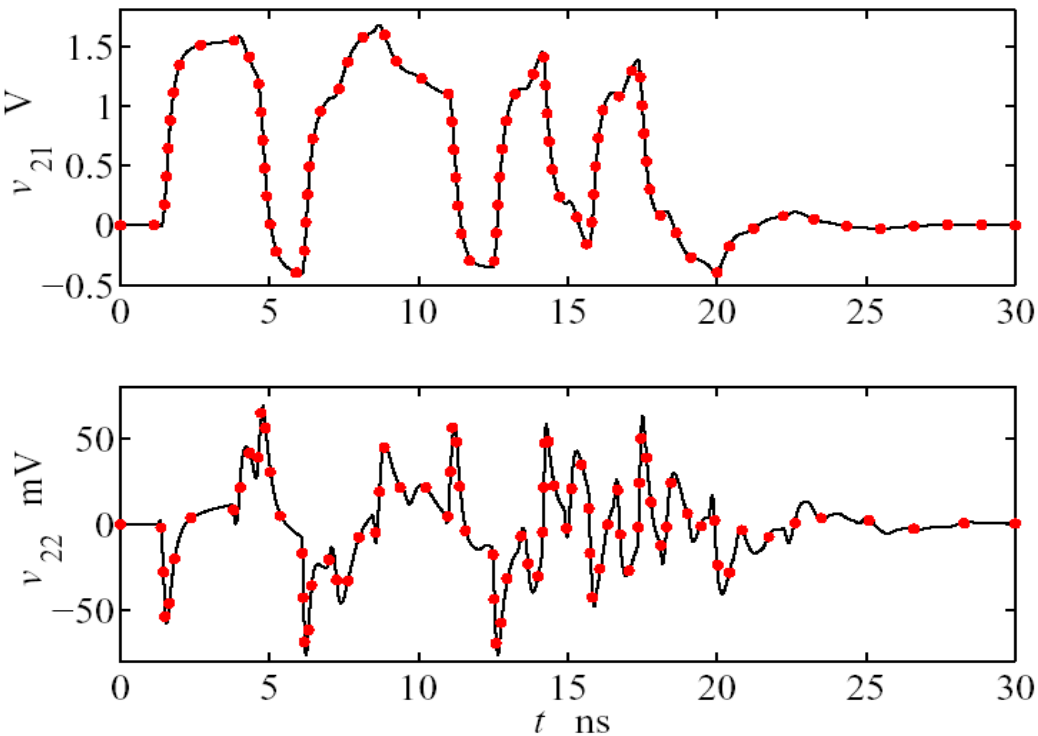
Setup



Models

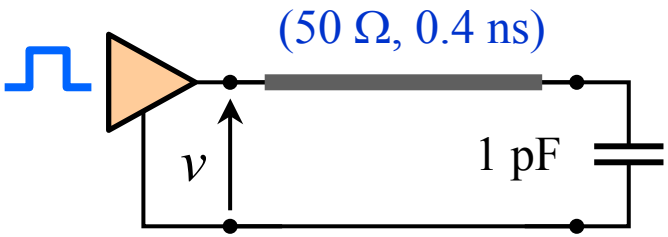
- **Reference (transistor-level)**
- **Macromodels (Mπ*log*)**

CPU TIME (PowerSPICE)	
Transistor-level	6 min
Mπ*log* model	5 s

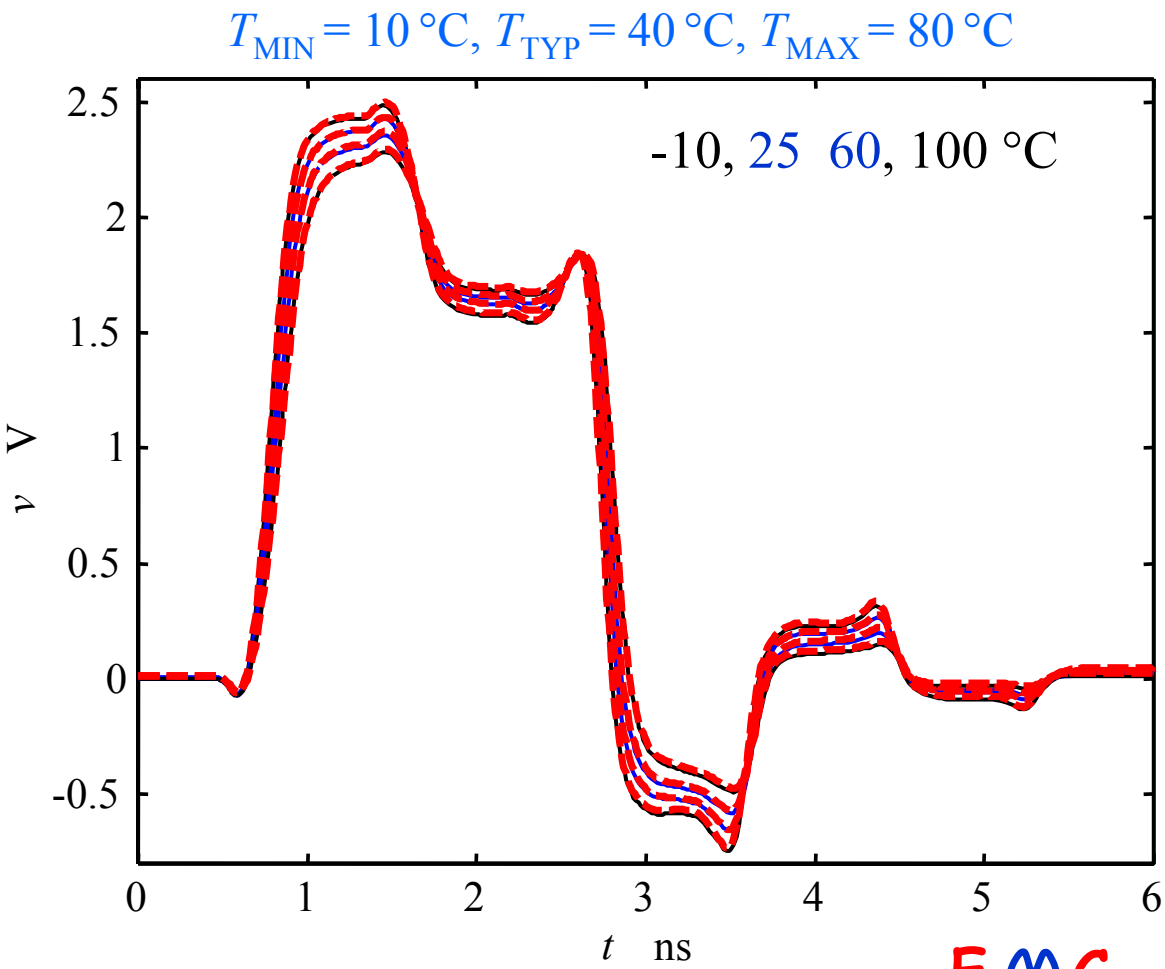


Example #2: temperature effects

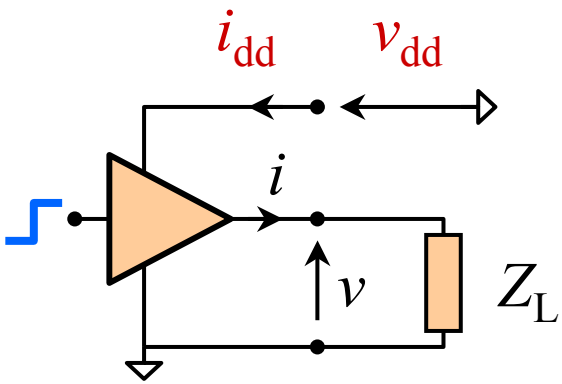
- **Test Case**



accuracy confirmed for realistic loads and a wide range of T values



Integration of signal and power supply port behavior



$$i = F(\Theta, v, v_{dd})$$
$$i_{dd} = F_{dd}(\Theta, v, v_{dd})$$

Macromodels obtained for v_{dd} values within the range $V_{dd} \pm 15\ \%$

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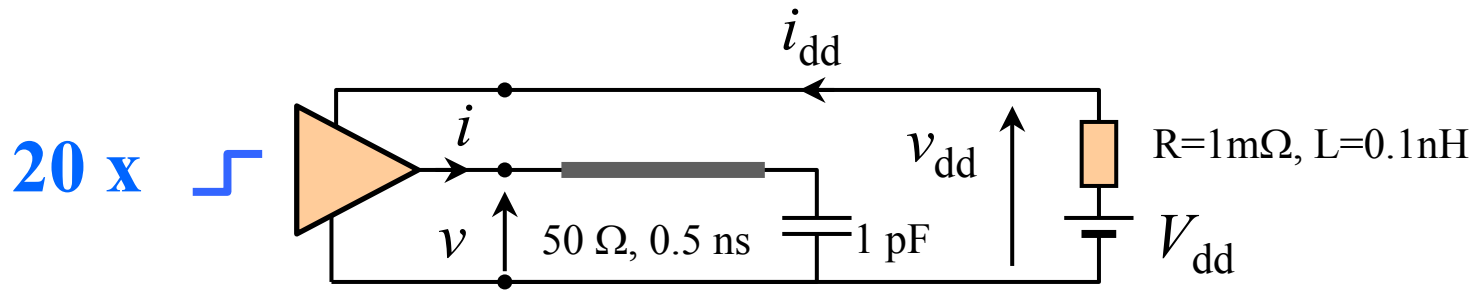
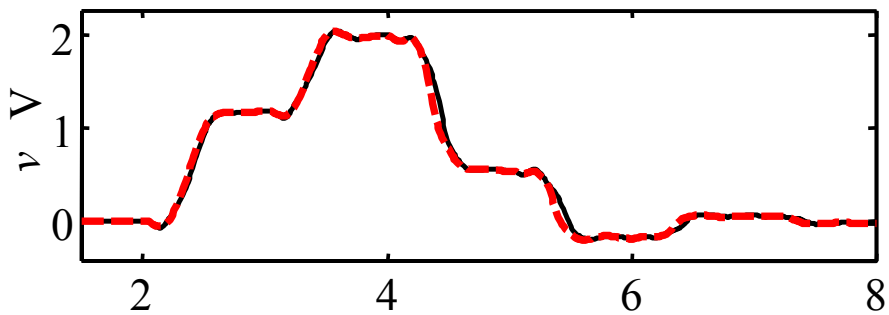
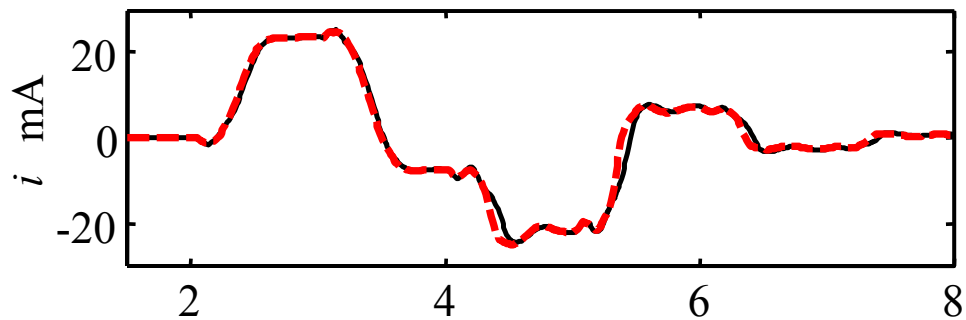
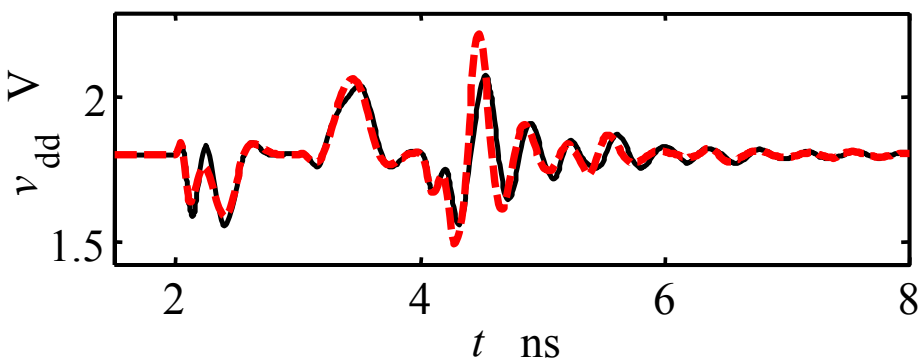
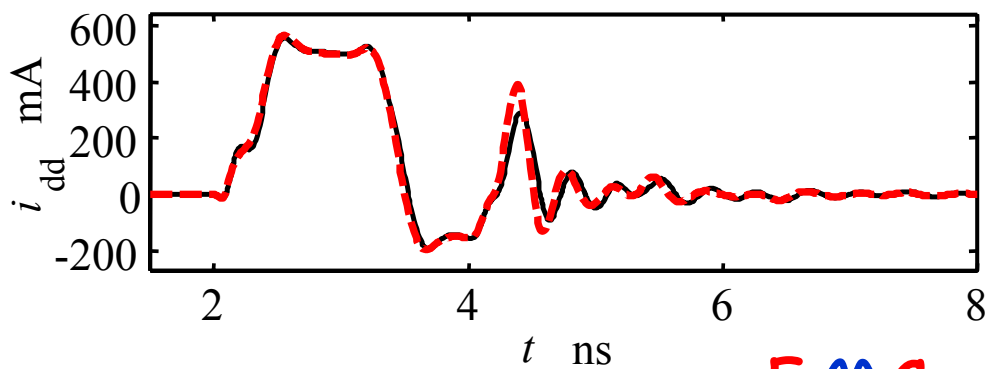
Example #3: SSN analysis





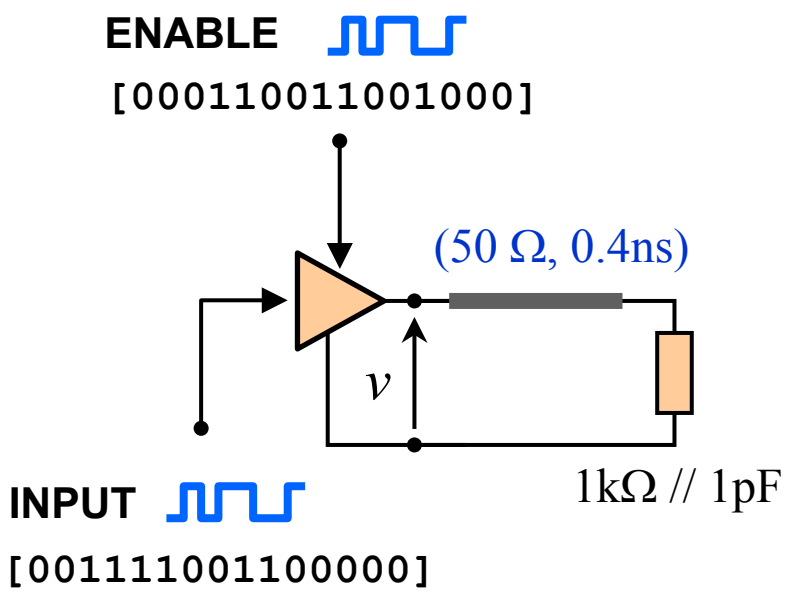


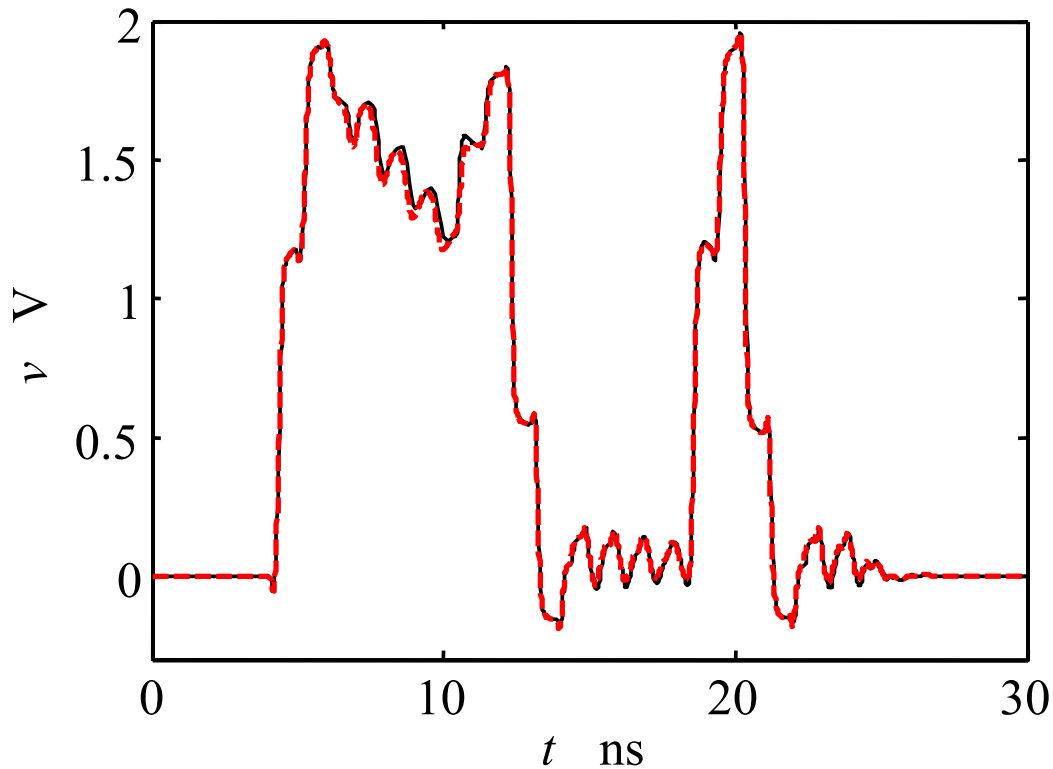




Example #4: tristate driver

- **Test Case**





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Conclusions

Mπ*log* approach

- **Macromodels for I/O Buffers and Power Supply Ports of Digital ICs**
- **Advantages**
  - **PROTECTION OF IP**
  - **HIGH ACCURACY** (timing errors **~10 ps @ 400 MHz**)
  - **LOW COMPLEXITY** (a few Gaussian functions)
  - **HIGH EFFICIENCY** (**20÷100** time **faster** than transistor-level models)

IBIS Compatibility via Multi-lingual description

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