# Some Remarks on Electrical Board Descriptions

**Michael Schäder**

**European IBIS Summit**
**Munich 2003**


**Vattmannstr. 3, D-33100 Paderborn, Germany**
**Email: michael.schaeder@zuken.de**

# Electrical Board Description (EBD)

*A board level component is the generic term to be used to describe a printed circuit board (PCB) or substrate which can contain components or even other boards, and which can connect to another board through a set of user visible pins. The electrical connectivity of such a board level component is referred to as an Electrical Board Description.*

Excerpt from IBIS 4.0 spec.

Typical examples of use are:

- SIMM, DIMM Modules,
- MCMs,
- Processor Modules, and also
- Packages

ZUKEN BE FIRST™

# EBD Limitations

- Transmission line parameters have to be derived with respect to well defined reference plane(s).
- No coupling between paths.
- Thus, no correct modelling of differential signalling.
- Insufficient connector modelling.

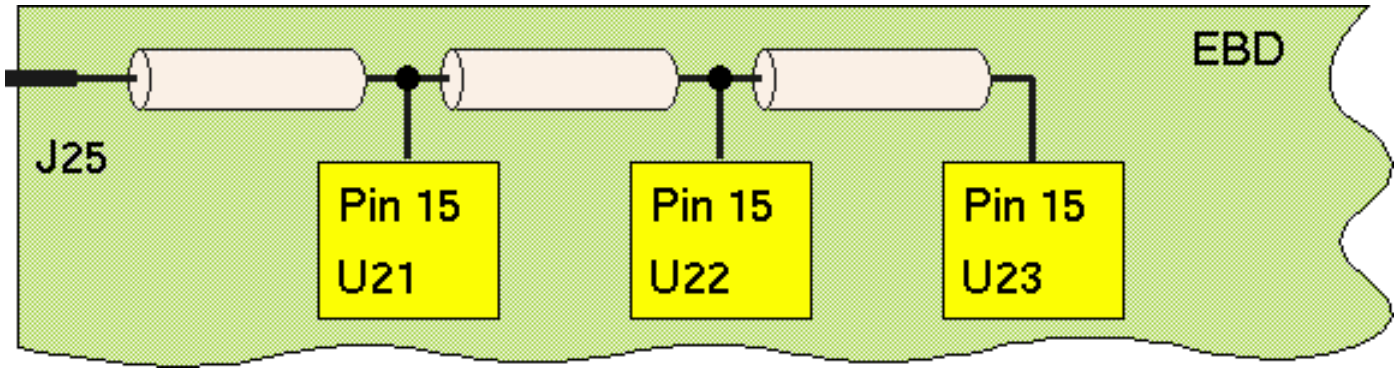
# Structure of an EBD Description

```
[Begin Board Description] zmini
[Manufacturer] Zuken
[Number Of Pins]  1
[Pin List] signal_name
1           D0
[Path Description] net1
Pin 1
Len = 0.1 L = 7.5n C = 3.0p /
Node U1.1
[Reference Designator Map]
U1          zsimple.ibs    zsimple
[End Board Description]
[End]
```

ZUKEN
BE FIRST™

# EBD Path Example 1 (SIMM Module)

```
[Path Description] CAS_2
Pin J25
Len = 0.5 L=8.35n C=3.34p R=0.01 /
Node u21.15
Len = 0.5 L=8.35n C=3.34p R=0.01 /
Node u22.15
Len = 0.5 L=8.35n C=3.34p R=0.01 /
Node u23.15
```

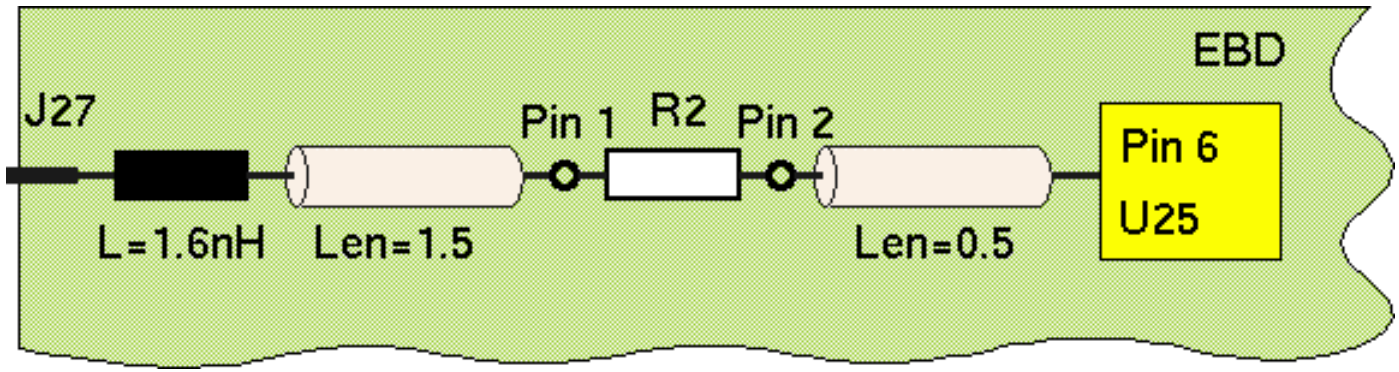



Example from IBIS 4.0 specification

ZUKEN BE FIRST™

# EBD Path Example 2 (Discrete Series El.)

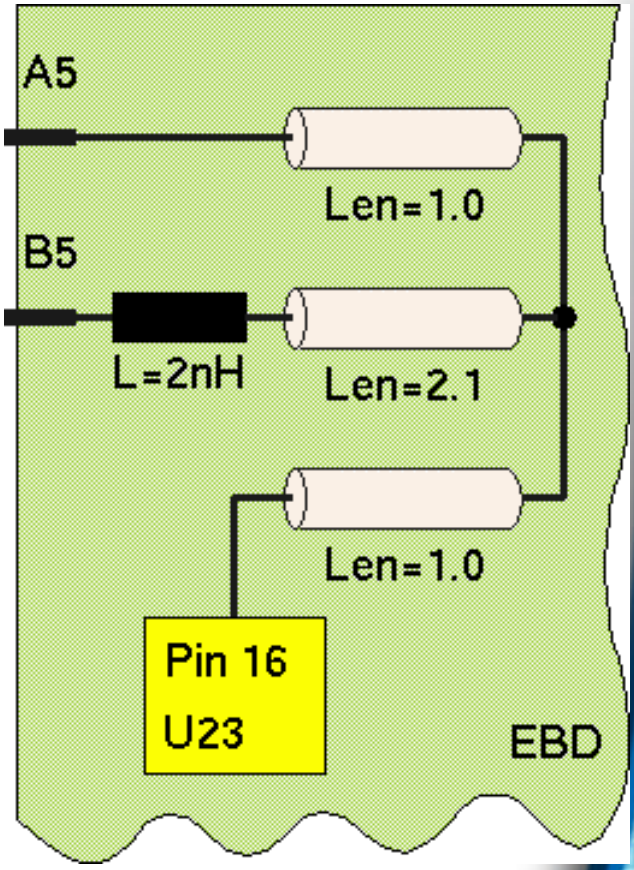
```
[Path Description] sig1
Pin J27
Len = 0  L=1.6n /
Len = 1.5 L=6.0n C=2.0p /
Node R2.1
Node R2.2
Len = 0.5 L=6.0n C=2.0p /
Node U25.6
```




Example from IBIS 4.0 specification

# EBD Path Example 3 (Fork/Endfork)

```
[Path Description] PassThru1
Pin B5
Len = 0    L=2.0n /
Len = 2.1 L=6.0n C=2.0p /
 Fork
 Len = 1.0 L = 1.0n C= 2.0p /
 Node u23.16
 Endfork
Len = 1.0 L = 6.0n C=2.0p /
Pin A5
```

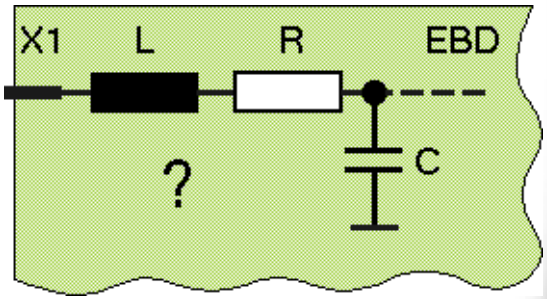



Example from IBIS 4.0 specification

# Common Problems in EBDs

- Unresolved external references.
- Missing boundary pins.
- Double listed boundary pins.
- Incomplete path descriptions.
- Connector modelled as part of path description.
- Ambiguous order of R,L,C, if described in one path segment:

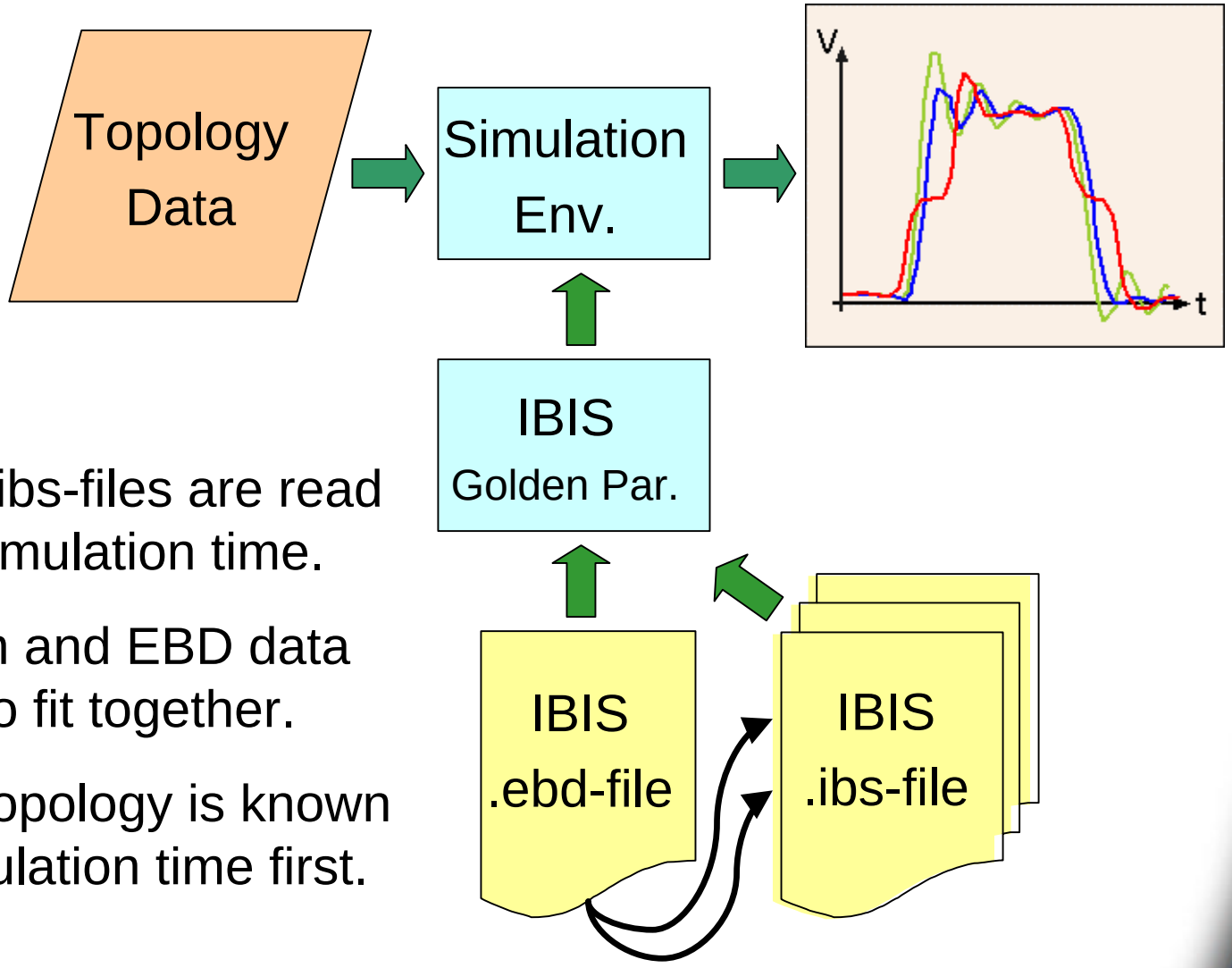
```
Len = 0 L=5n C=4p R=0.01
```




- Path descriptions are not optimised.
- Confusion about arbitrary unit length.

ZUKEN
BE FIRST™

# Apply EBDs in Simulation (Directly)




- .ebd-/.ibs-files are read in at simulation time.
- Design and EBD data have to fit together.
- Final topology is known at simulation time first.

ZUKEN
BE FIRST™

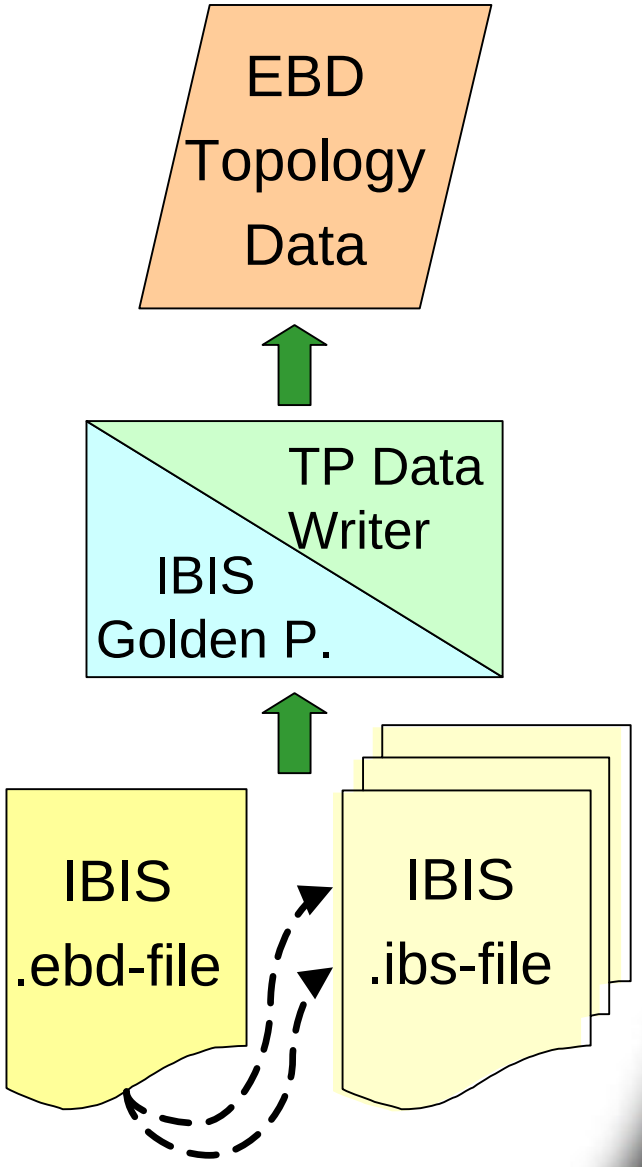
# Another way getting EBDs into Simulation

- Convert EBD into the simulation environment's specific topology format.
- Combine PCB component(s) pins with the EBD's boundary pins (logically).
- Consider EBD paths in electrical net extraction.
- Perform simulation as usual.

ZUKEN
BE FIRST™

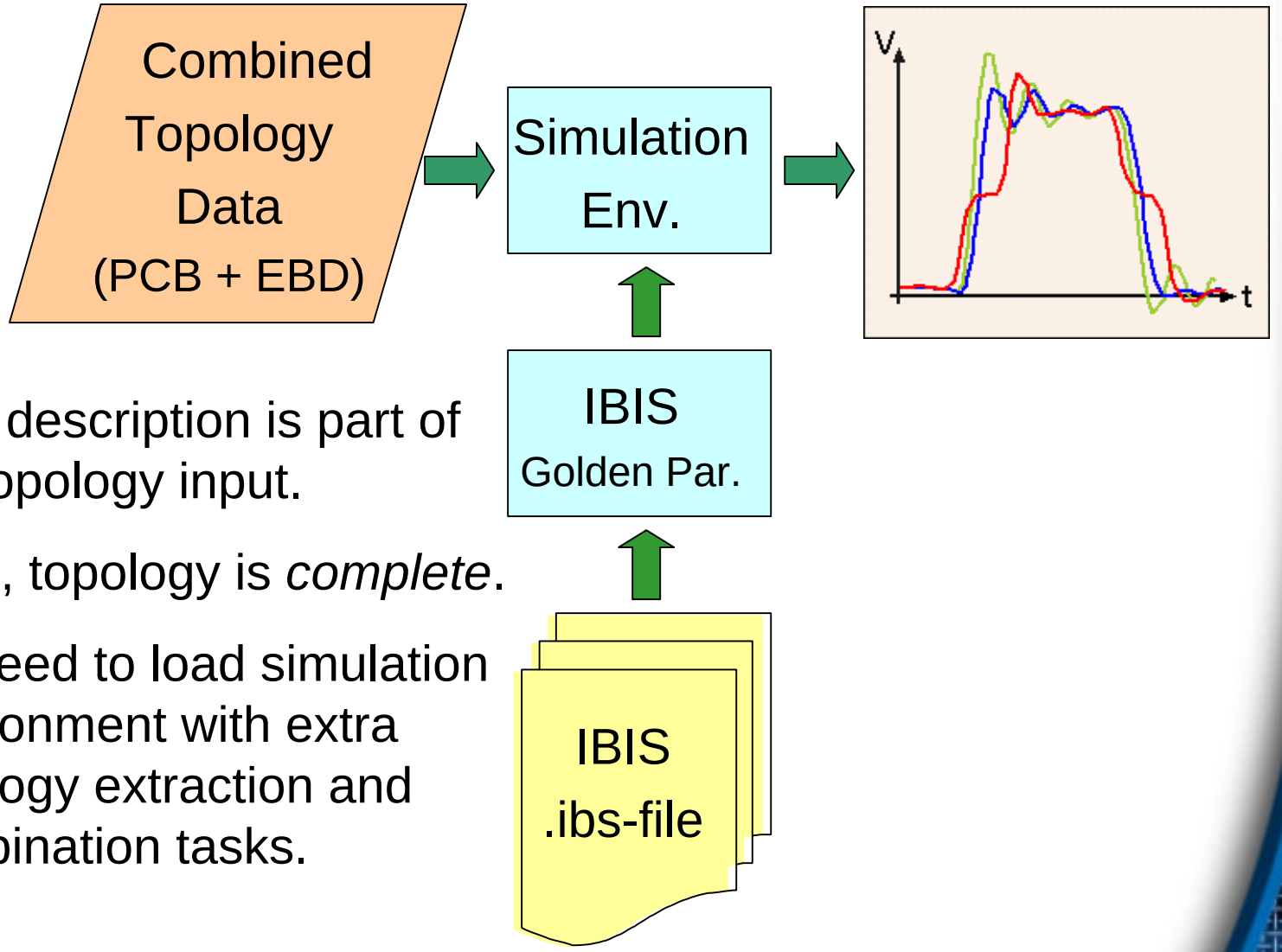
# Conversion of EBDs

- Can improve quality of final topology description.
- Enables logical combination of PCB with EBD data.
- Allows connector models to be used (PCB ✍✍ EBD).




ZUKEN
BE FIRST™

# Simulate Combined PCB/EBD Topology




- EBD description is part of the topology input.
- Thus, topology is *complete*.
- No need to load simulation environment with extra topology extraction and combination tasks.

ZUKEN
BE FIRST™