Quality of IBIS Models
IBIS for LVDS

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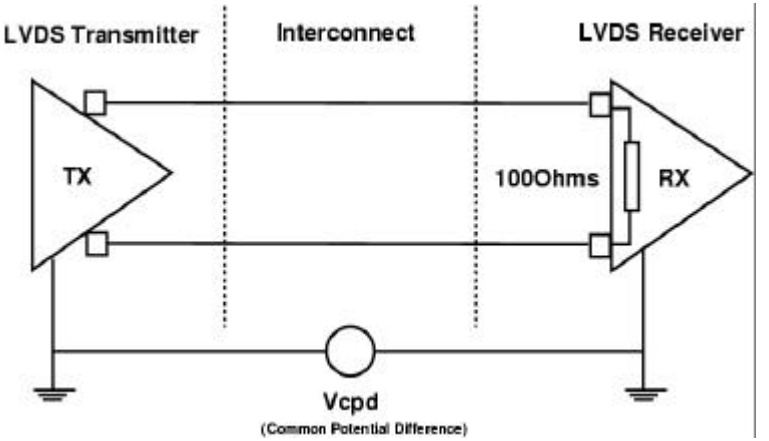
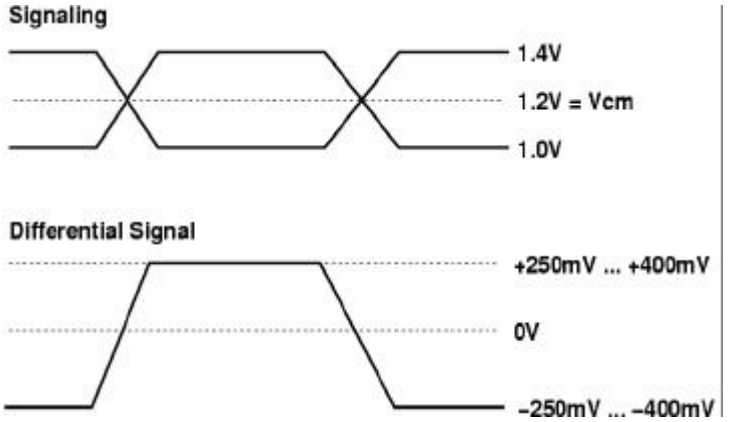
Infineon Technologies AG

LVDS Definition

LVDS Low Voltage Differential Signaling
Point to Point 500 MBit/sec



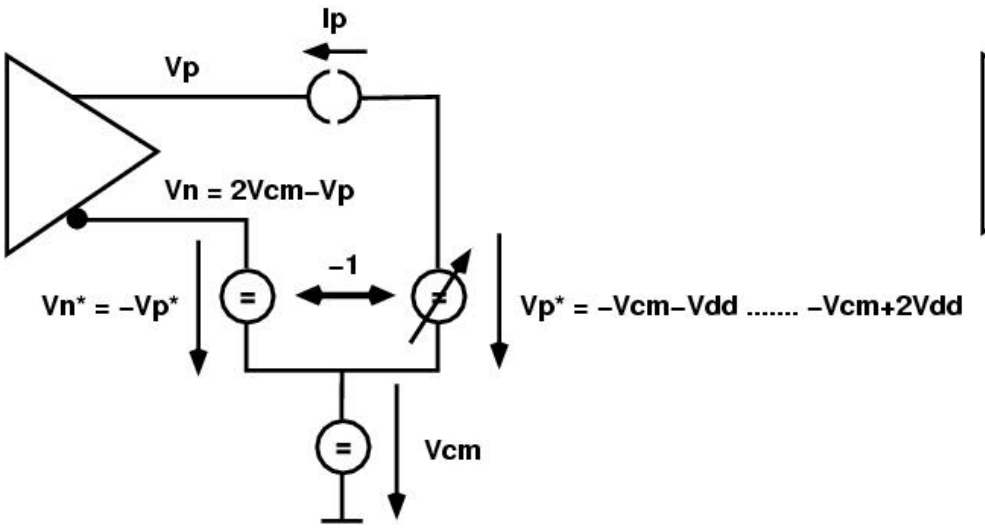


Standard TIA/EIA-644
IEEE Std 1596.3

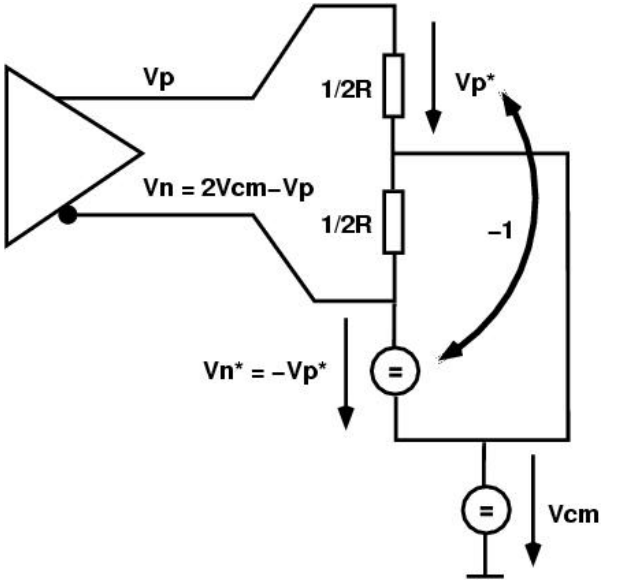
Modeling Methodology

Problem: **In IBIS for each differential output pin a own buffer model is necessary, but this models are not independent !!**

VI - Characteristics

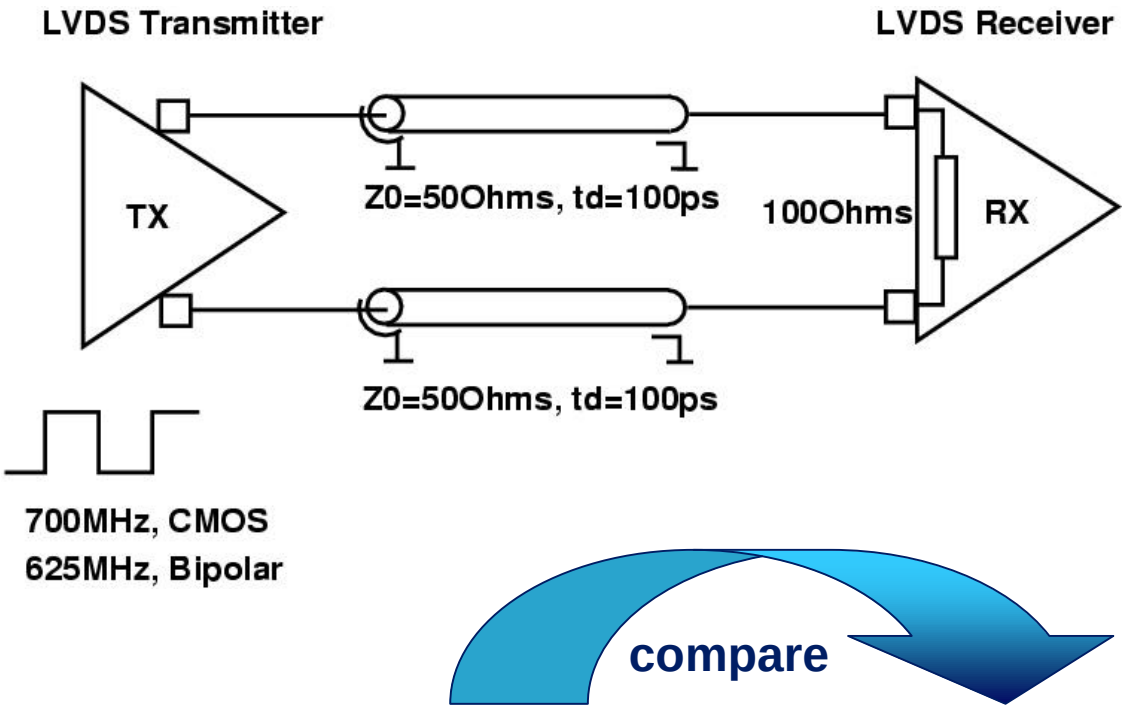


Vt - Waveforms



Introduced by	**A. Tambone**	**(Semiconductor Business News 2000)**
Proven by	**H. Hegazy, et. al.**	**(IBIS Summit Date 2001)**
	D. J. Burns, et. al.	**(IBIS Summit DAC 2002)**

Testsystem



Testcases:

700MHz, CMOS

625MHz, Bipolar

SPICE Referenz:

TITAN (Infineon) for 700MHz, CMOS using layout extracted netlist.

SPECTRE (Cadence) for 625MHz, Bipolar using schematic netlist.

IBIS Simulation:

HSPICE (Avant!)

Interconnectix, ICX IS (Mentor)

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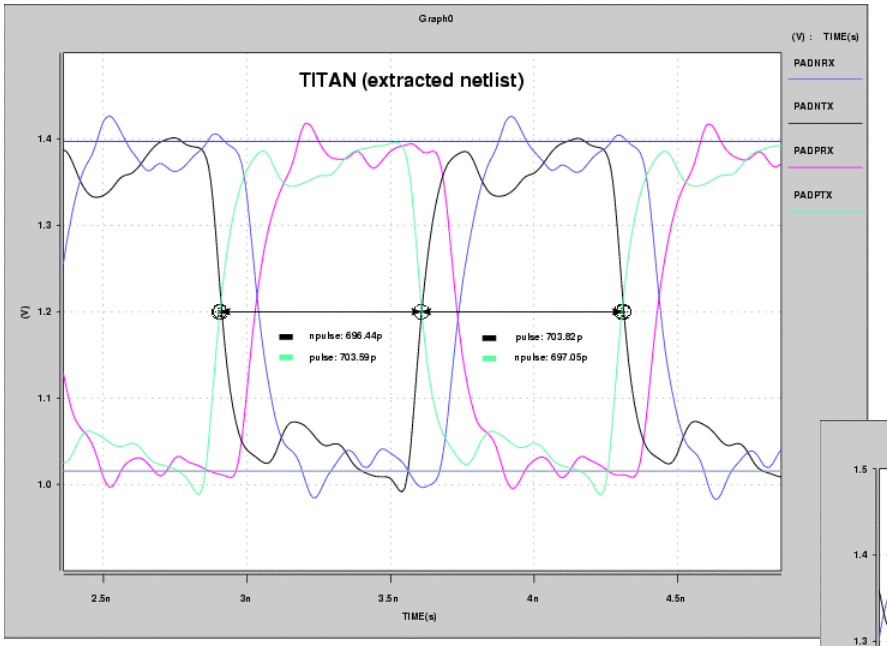
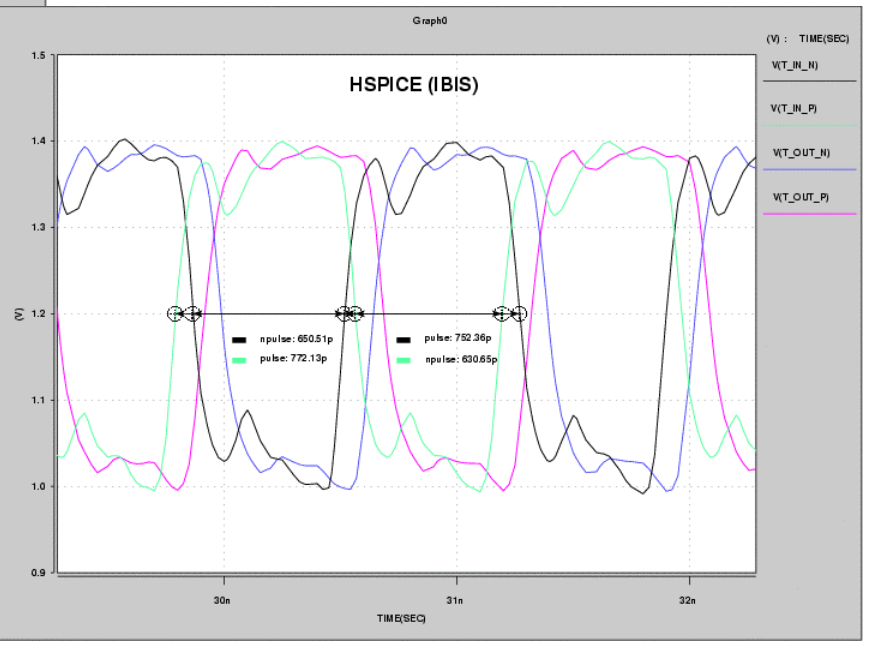
Results 700MHz, CMOS



SPICE (TITAN)
Transmitter Output & Receiver Input

IBIS (HSPICE)
Transmitter Output & Receiver Input



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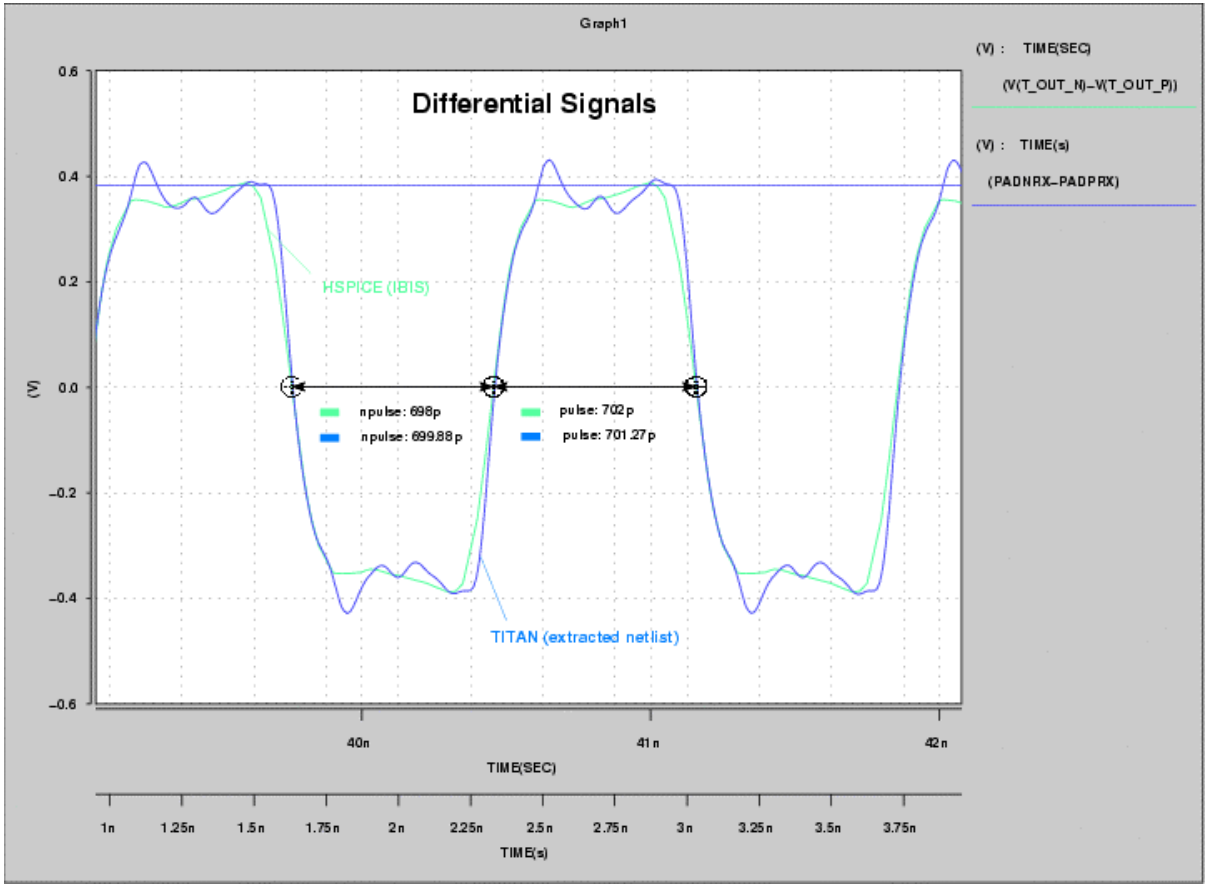
Results 700MHz, CMOS



Differential Signal at Receiver Input

SPICE (TITAN) & IBIS (HSPICE)

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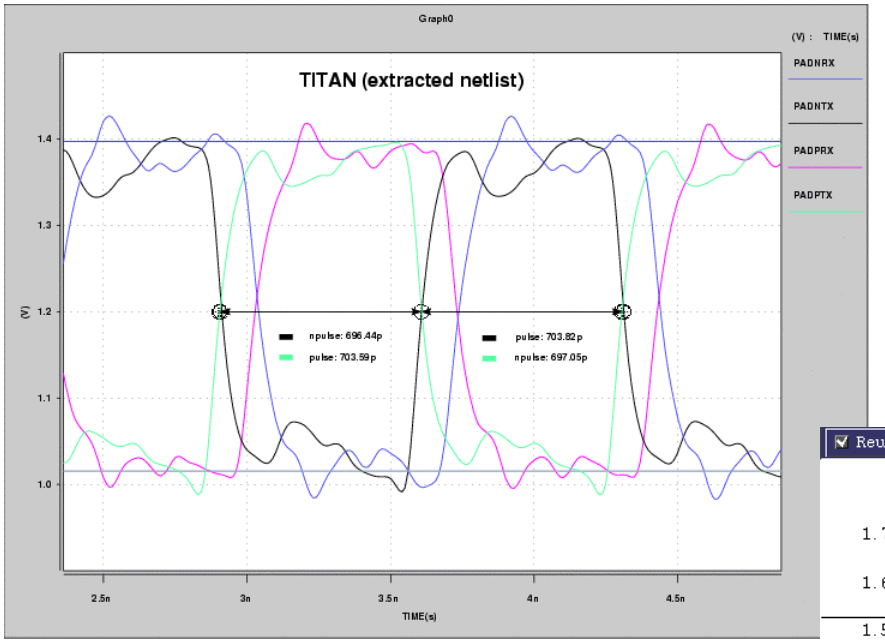
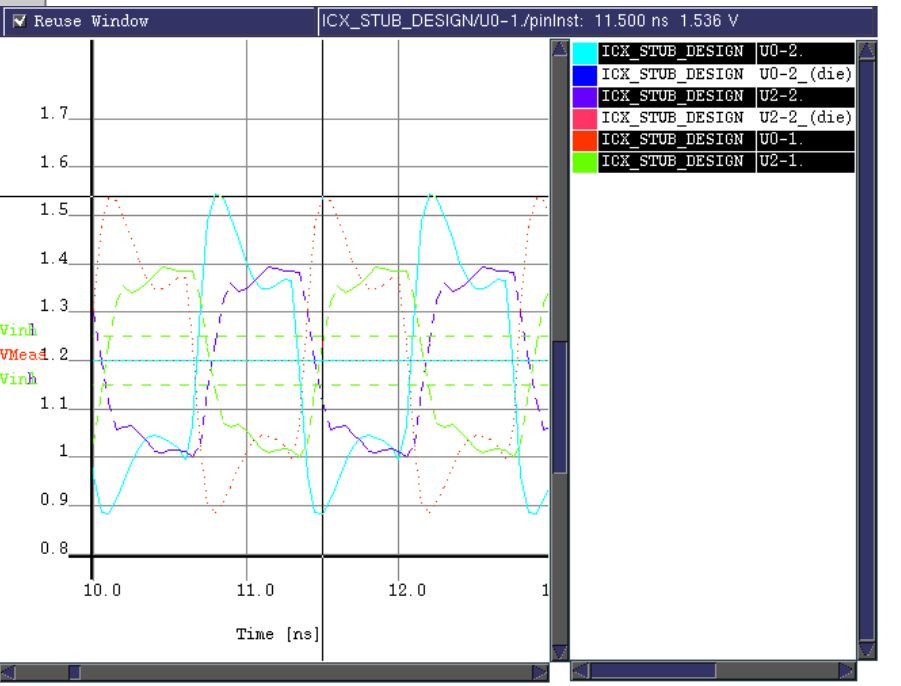
Infineon

Results 700MHz, CMOS



SPICE (TITAN)
Transmitter Output & Receiver Input

IBIS (Interconnectix, ICX IS)
Transmitter Output & Receiver Input



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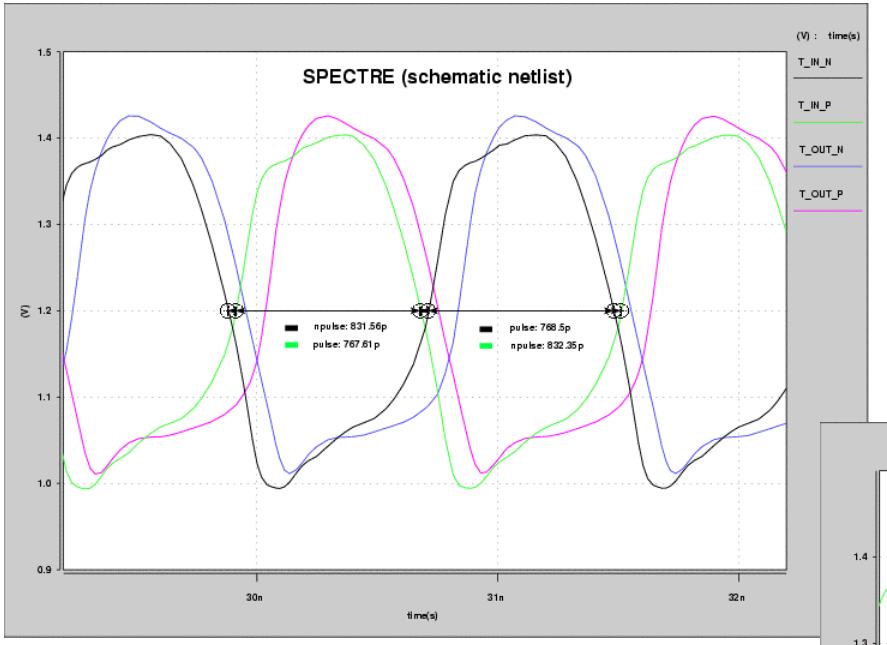
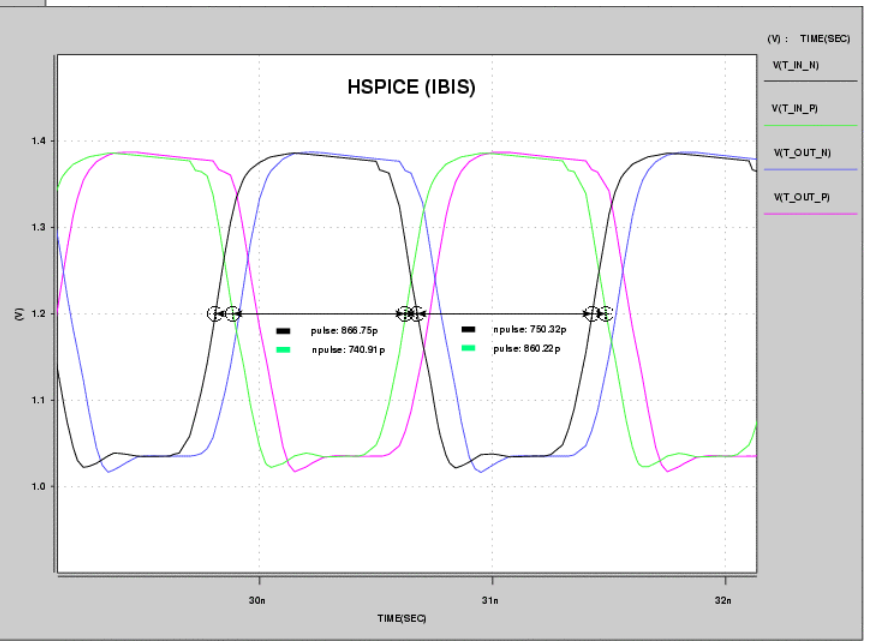
Results 625MHz, Bipolar



SPICE (SPECTRE)
Transmitter Output & Receiver Input

IBIS (HSPICE)
Transmitter Output & Receiver Input



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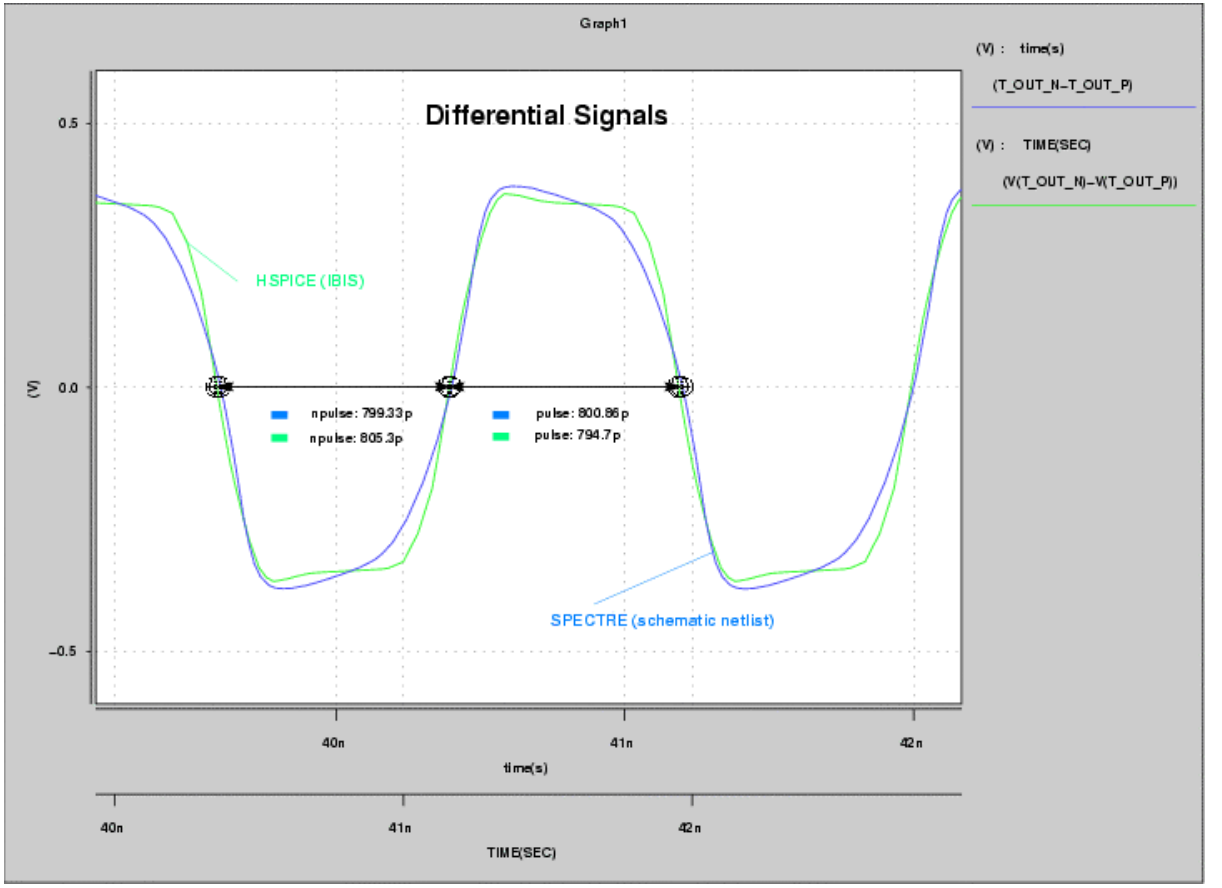
Results 625MHz, Bipolar



Differential Signal at Receiver Input

SPICE (SPECTRE) & IBIS (HSPICE)

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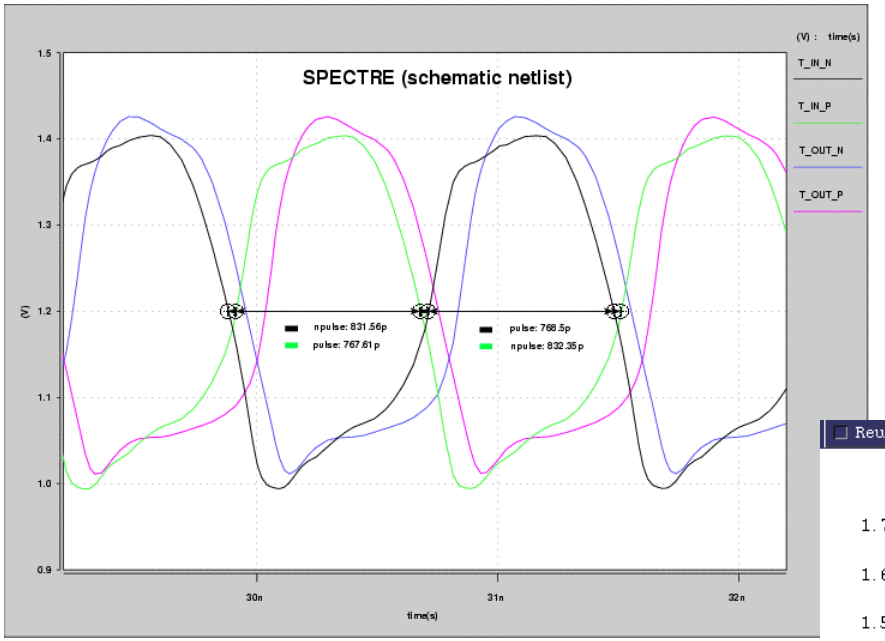
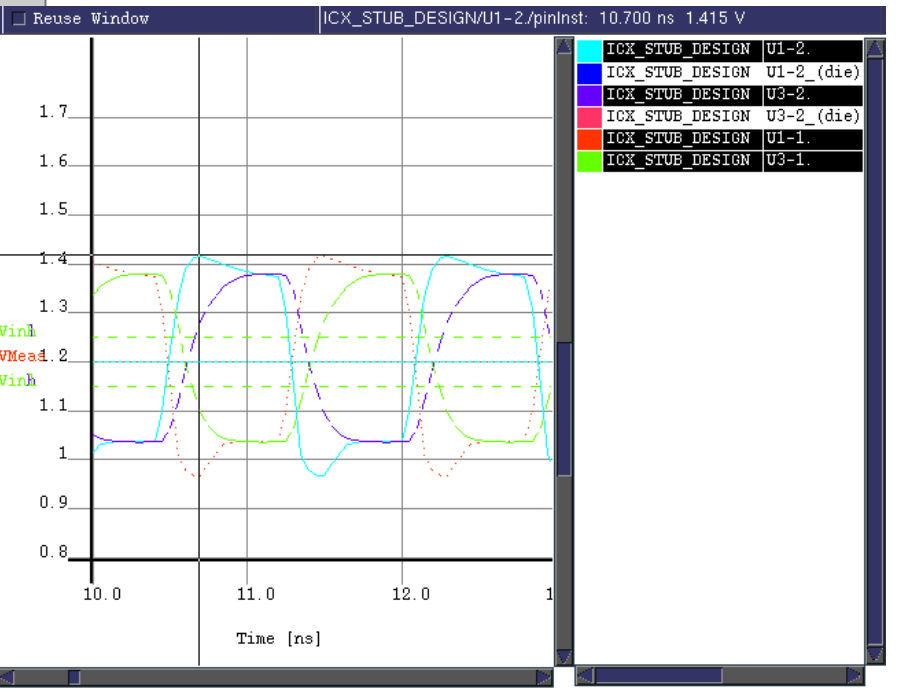
Results 625MHz, Bipolar



SPICE (SPECTRE)
Transmitter Output & Receiver Input

IBIS (Interconnectix, ICX IS)
Transmitter Output & Receiver Input



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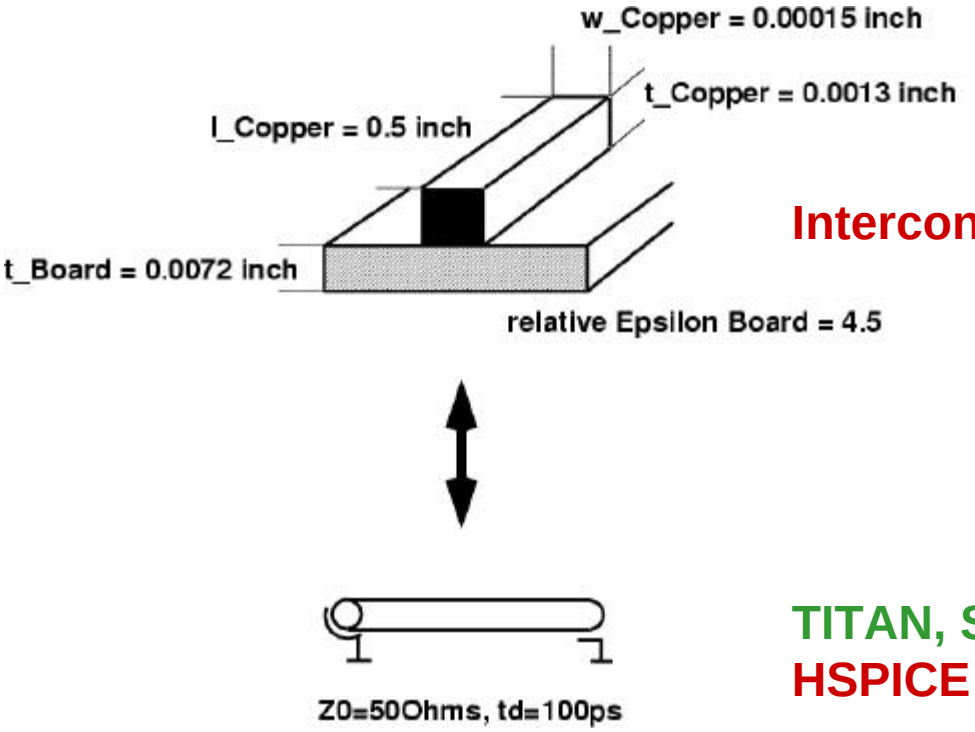
Transmission Line Modeling

Microstrip Approach proposed by Brain C. Wadell

Transmission Line Design Handbook

Artech House
Norwood
MA, 1991
pp 94 .. 95



Interconnectix, ICX IS

TITAN, SPECTRE, HSPICE

Results Summary

- Differences in pulsewidth symmetry and dc-shift of waveform crossings

- HSPICE: Tendency to shorten the low level pulse.
  ICX IS: Interchange of signal behaviour at transmitter output and receiver input compared to SPICE.
  Option > Remove Initial Delay from V-t-curves < must be turned on!

- Overclocking
  HSPICE: t_rise + t_fall < 2T_Signal
  (e.g. T_Signal = 1.6ns for 625MHz, Bipolar testcase)
  ICX IS: not verified!

Without assistance of tool vendors improvement of IBIS model quality is very difficult !!

Model Vendors Dilemma

- The different simulation results are all similar, but the differences are large enough, that a potential modeling weakness cannot be excluded.

  What is wrong: the IBIS modeling or the IBIS simulations ?

- The Golden Parser only supports syntax checking and plausibility checks (e.g. vi-characteristics, vt-waveforms compliance check), but no verification of the electrical behaviour.

How to assure the quality of IBIS models ?

Possible Solutions

What can be done ?

- Ignore the problem
- Golden Simulator
- Focus on key customer
- Qualification service for IBIS models
- Free access to IBIS tool sweet
- Cooperation with dedicated tool vendor