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An Initial Case Study for BIRD95: Enhancing IBIS for SSO Power Integrity Simulation

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SIGRITY, INC.

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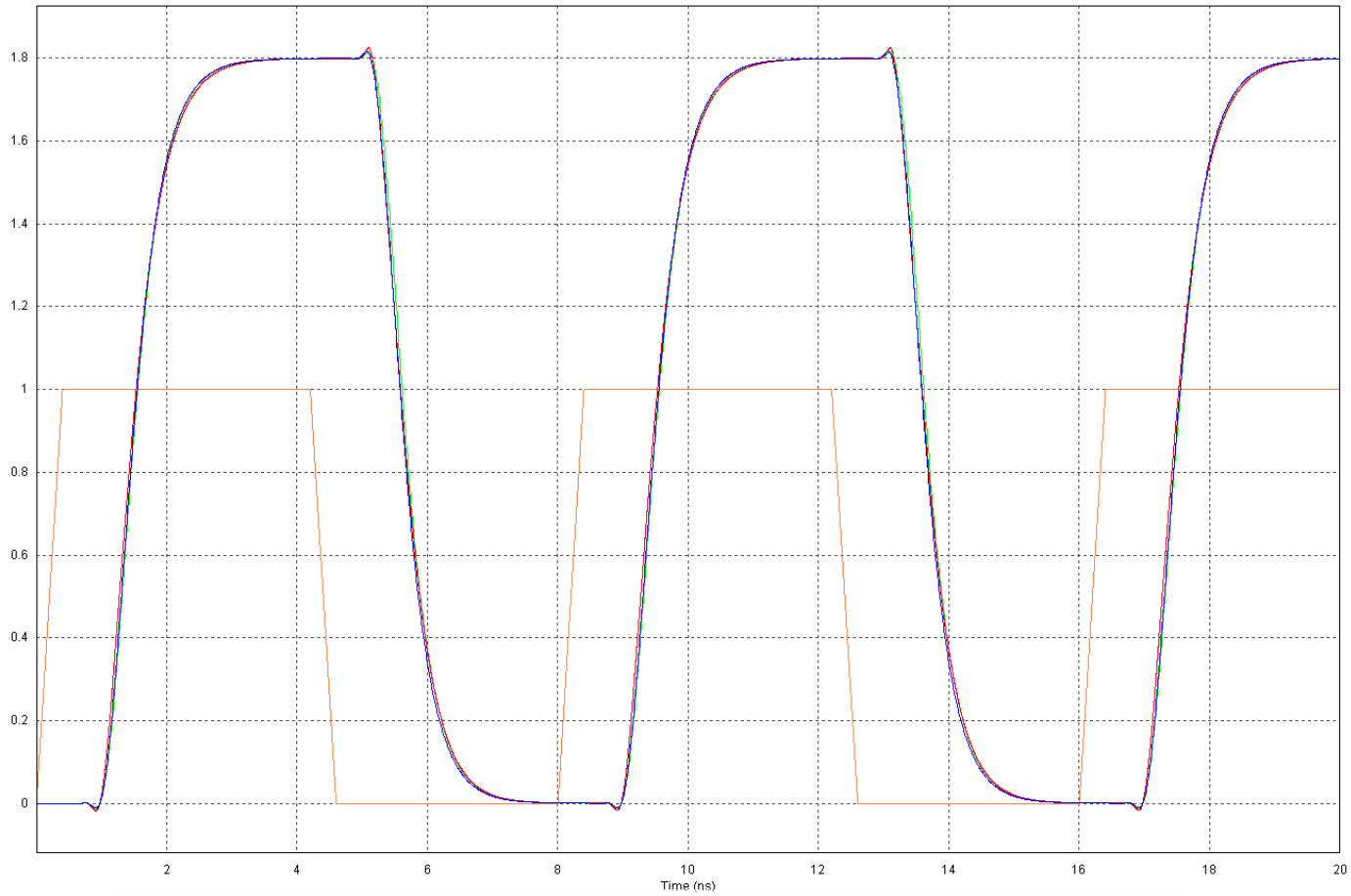
- Present-day IBIS vs SPICE correlation
  - Limitations of IBIS based SSO simulations
- Currents that IBIS can calculate
  - Comparison of IBIS currents with transistor currents
- BIRD95: Add parasitic currents to the IBIS model
  - Parasitic current extraction methodology
  - Preliminary results and observations
- Suggestions for improvement
- Summary

Correlation of IBIS and SPICE output voltages

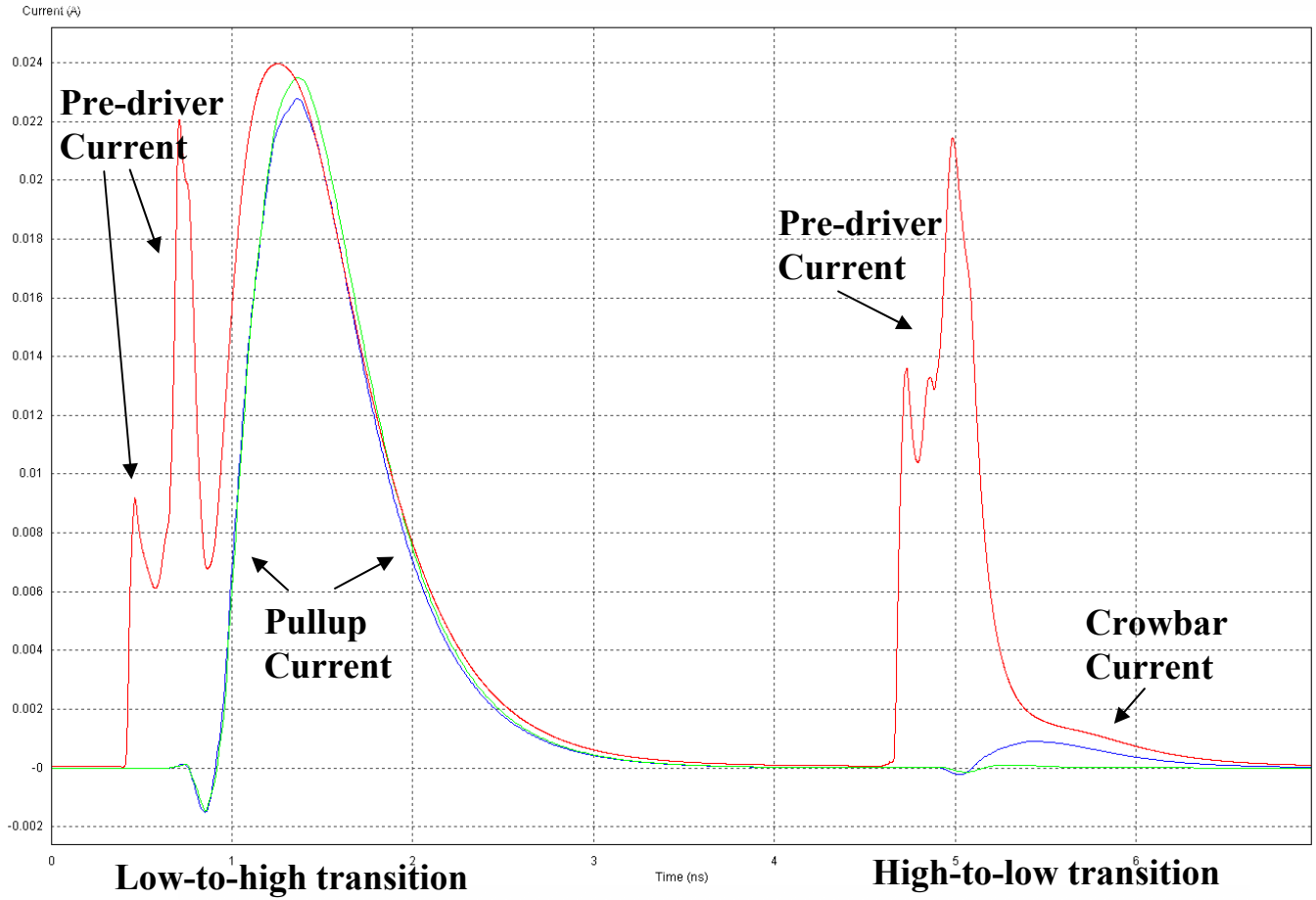
I/O voltage at the die; 10 pF load; no package information; ideal PDS



HSPICE transistor – Red HSPICE IBIS – Green Speed2000 IBIS – Blue

Comparison of IBIS and SPICE total VDDQ current

Total VDDQ driver current; 10 pF loading; ideal PDS



HSPICE transistor – Red HSPICE IBIS – Green Speed2000 IBIS – Blue

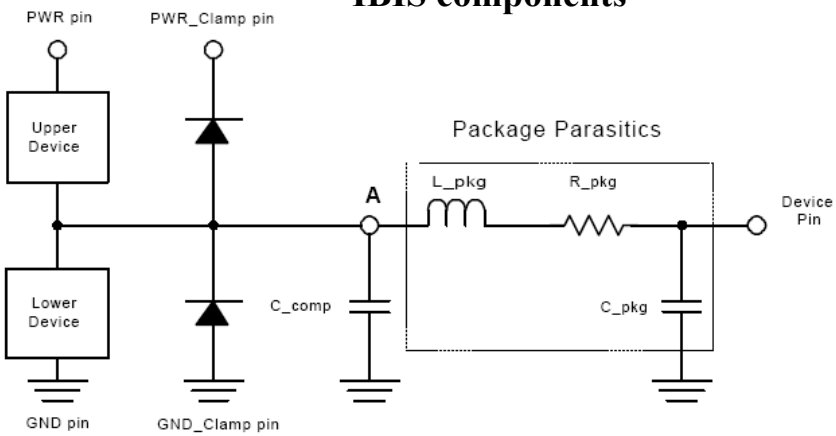
The total VDDQ current for the transistor-level model is significantly different from its pullup component. There is a large amount of pre-driver current due to crowbar effects and gate capacitance charging.

Pre-driver current occurs significantly earlier than the pullup current. The pre-driver current is rapidly decreasing as the pullup is turning on.

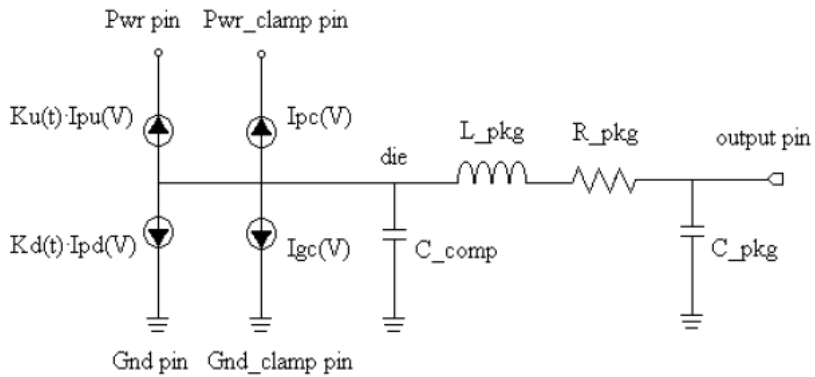
The pre-driver current peaks almost as high as the pullup current. Note that the dI/dt of the pre-driver is much larger than that of the pullup current.

Currents that IBIS can calculate

IBIS components



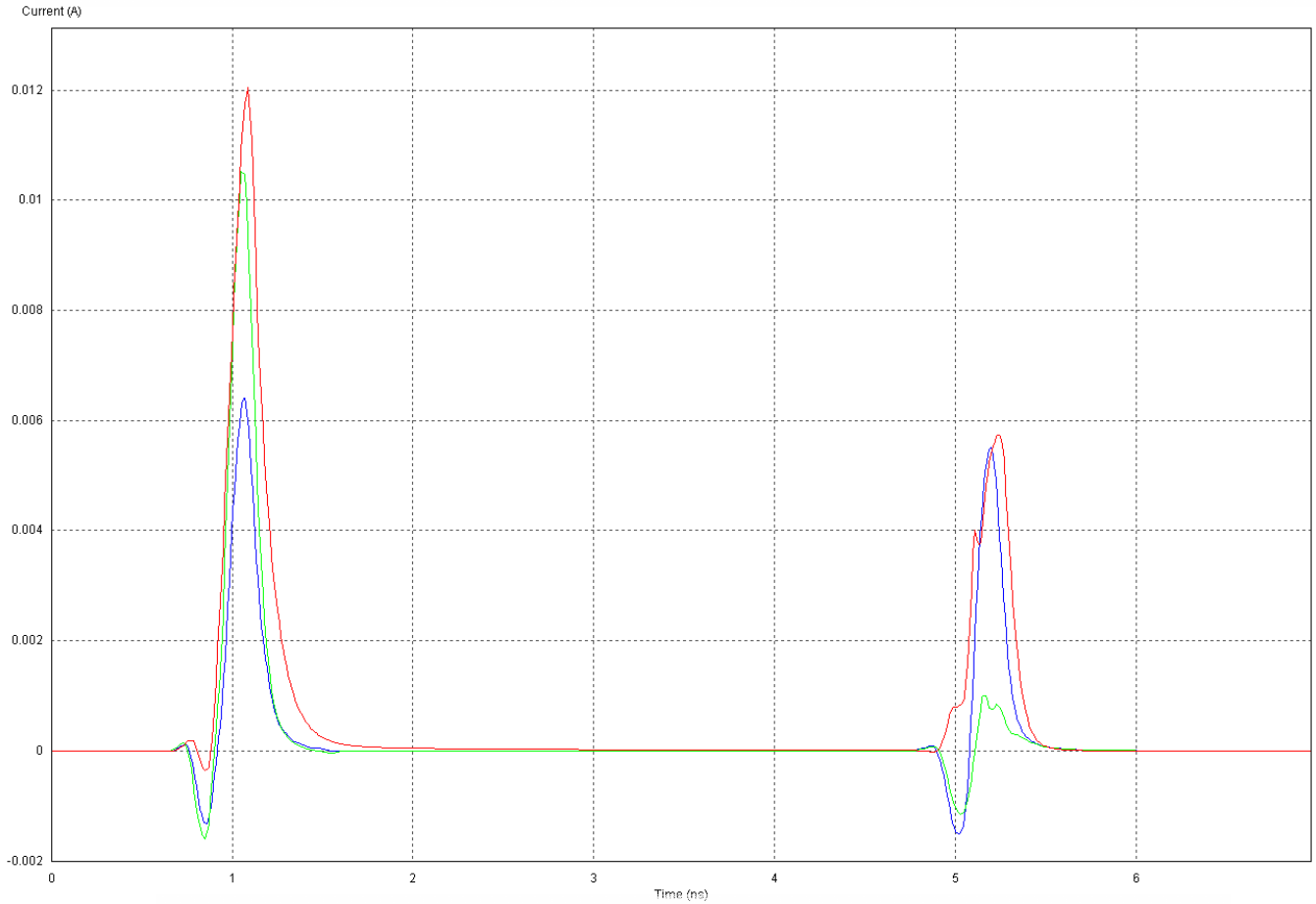
Analog Model of an IBIS output



- **The pullup and pulldown components are modeled as voltage controlled current sources**
- **The instantaneous value for each voltage controlled current source is derived from the I/V tables and is scaled based on the information in the V(t) tables**
- **The voltage controlled current sources are simultaneously active to model crowbar**
- **Crowbar current can be approximated fairly well if all four V(t) tables are present in the IBIS file**

Comparison of final drive stage crowbar current

Current through the driver's upper device; open circuit loading; ideal PDS



HSPICE transistor – Red HSPICE IBIS – Green Speed2000 IBIS – Blue

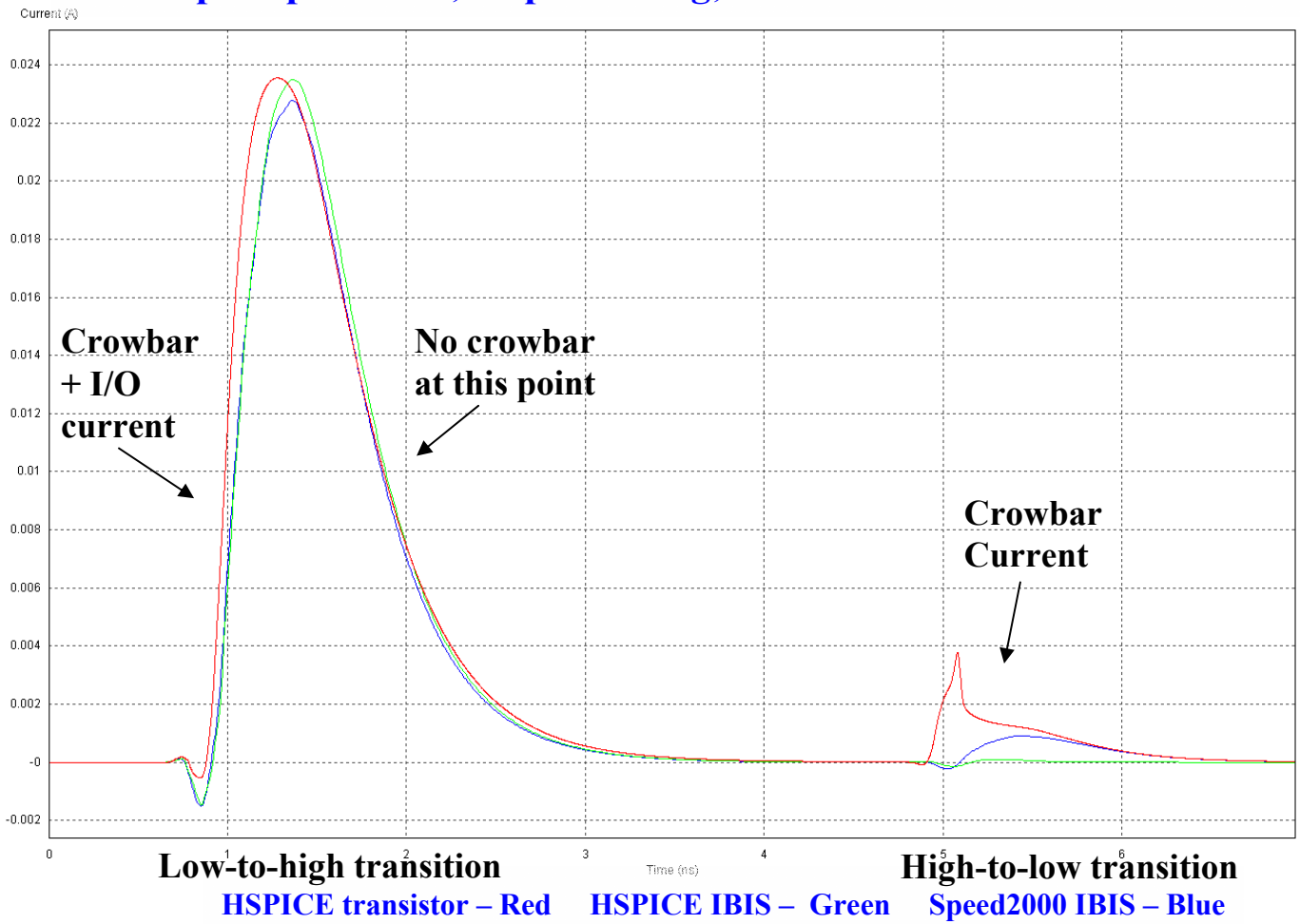
The IBIS algorithms in HSPICE and Speed2000 include the crowbar current. The overlap of the pullup and pulldown current sources is inherent in the model and cannot be excluded.

HSPICE currents show the best correlation for the low-high transition at 1ns.

Speed2000 currents show the best correlation for the high-low transition at 5ns.

Comparison of driver pullup current

Driver pullup current; 10 pF loading; ideal PDS



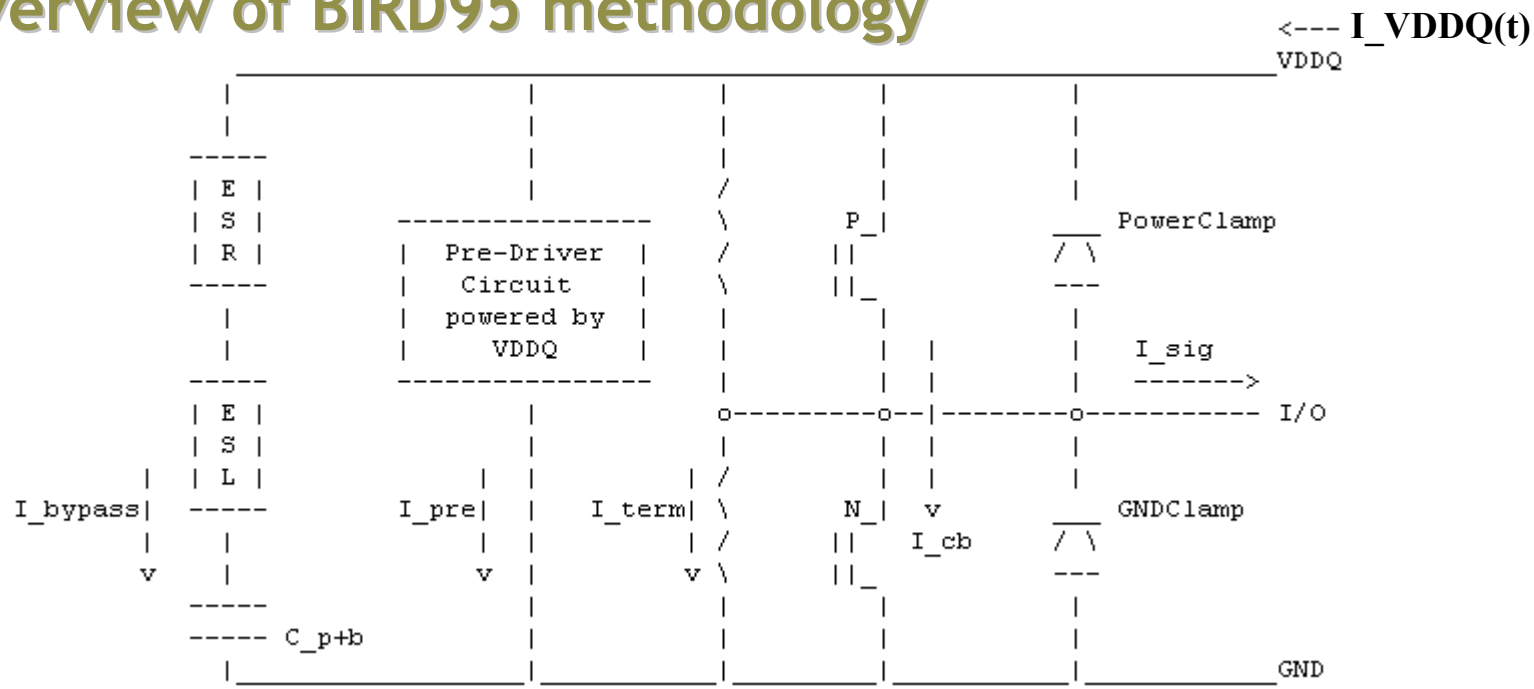
The magnitude of the rising-edge pullup current is dominated by the I/O current that charges the load capacitor. Both IBIS algorithms show good correlation to the SPICE model for the rising edge pullup current.

The crowbar current is easily identified for the high-low transition at 5ns. Speed2000 catches the trailing edge of the crowbar current.

Objective of BIRD95:

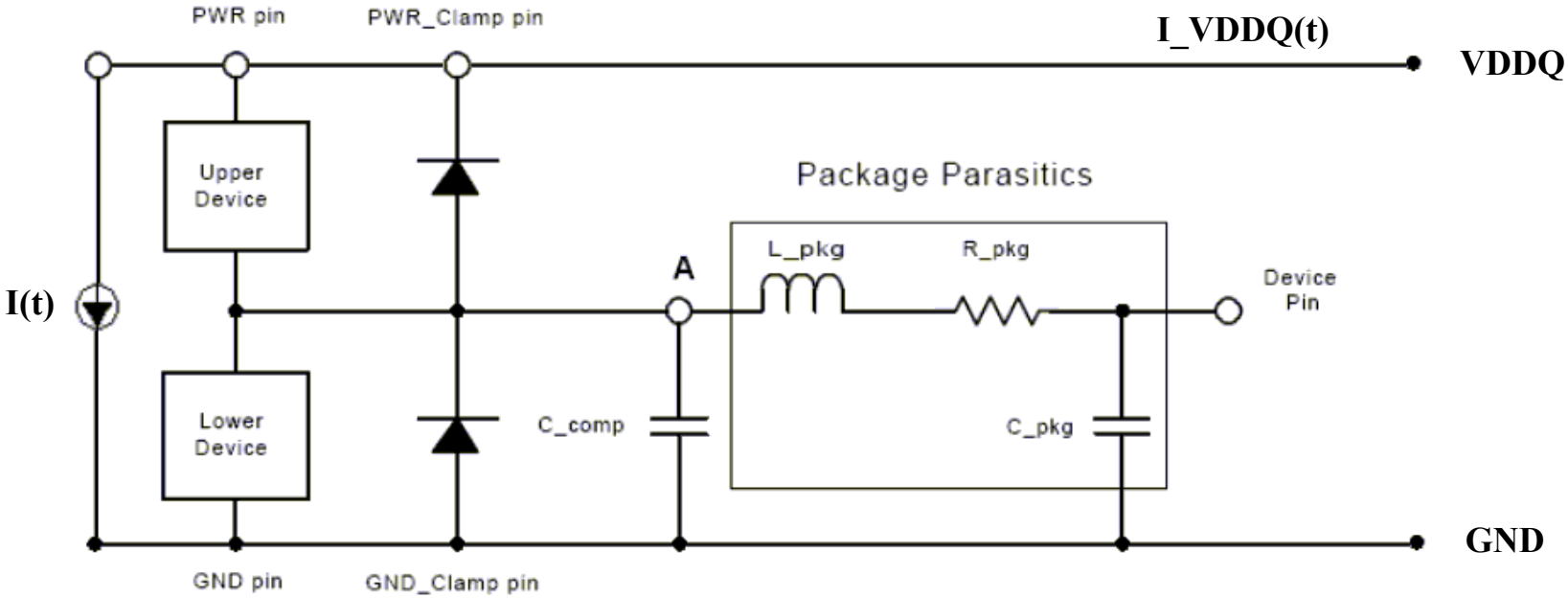
Improve IBIS models to facilitate accurate SSO and other Power Integrity Simulations

Overview of BIRD95 methodology



- Total VDDQ current will be measured for the transistor level model
- Current versus time tables will be added to the IBIS file
- The IBIS simulator will use the I_VDDQ(t) tables to include the parasitic currents from the pre-driver, I/O termination, crowbar, etc.
- Note that if an ideal VDDQ supply is used, I_bypass(t) = 0 for all t.

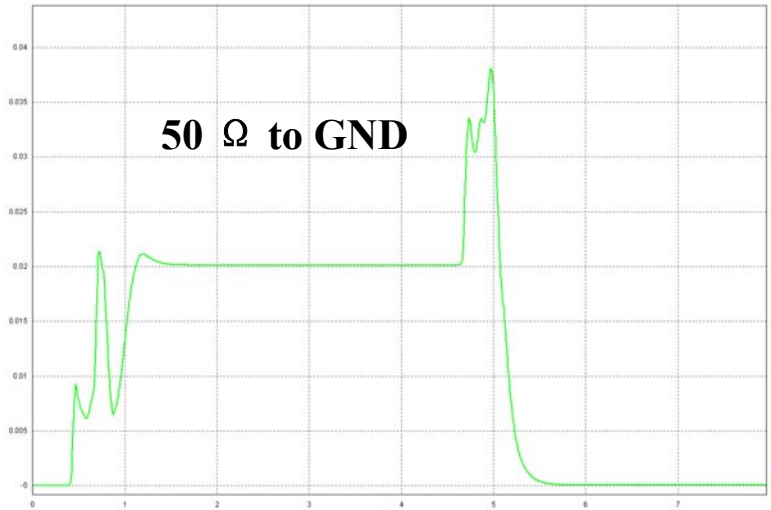
Overview of BIRD95 methodology

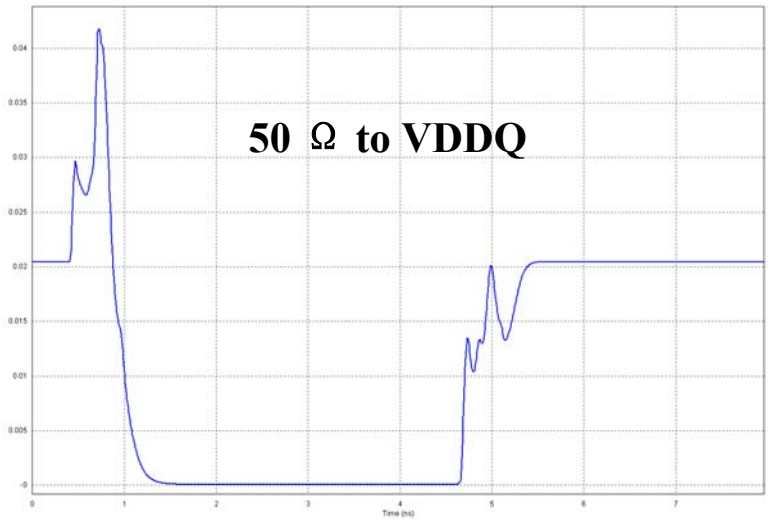


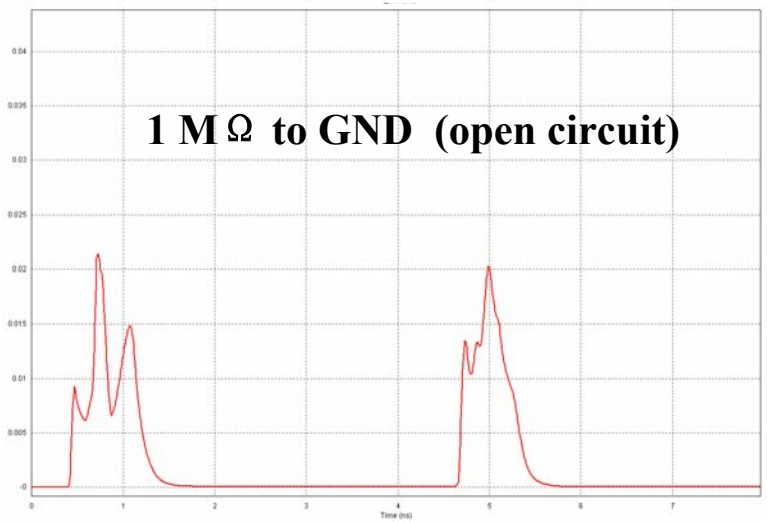
- **This IBIS simulator will include the parasitic currents by calculating the difference between the IBIS VDDQ current and I_VDDQ(t)**
- **A current source is added in parallel with the IBIS device such that**

  I(t) = I_VDDQ(t) – IBIS VDDQ current(t)

BIRD95 recommends three parasitic current extractions



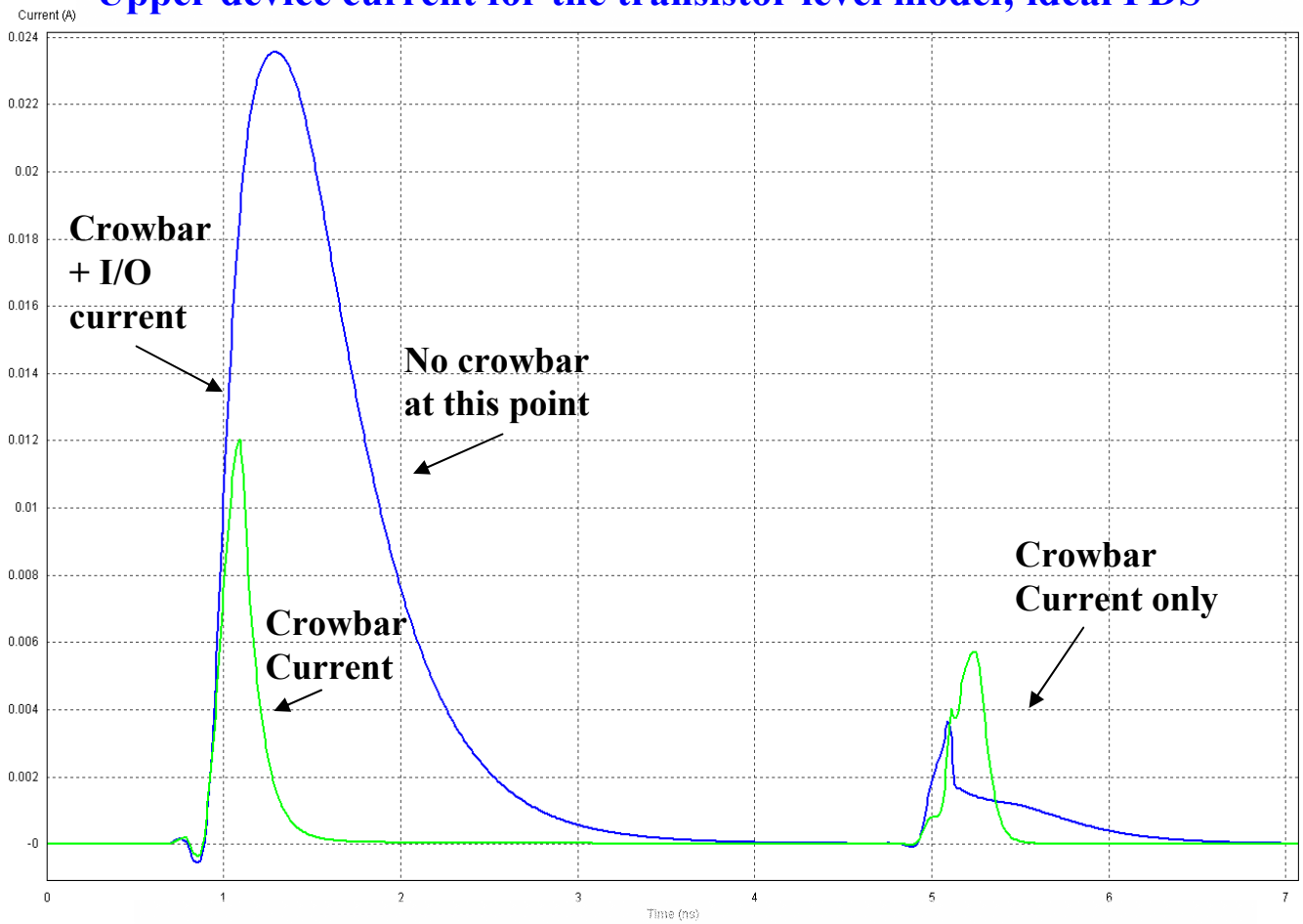




- BIRD95's I_VDDQ consists of all pre-driver, final stage I/O, termination, crowbar, and other parasitic currents.
- As expected, these waveforms vary significantly due to the final stage I/O currents.
- The two spikes that precede each transition are due to the pre-driver current.
- Unfortunately, there is no clear separation between the final stage crowbar and I/O current contributions. Is this a problem? If so, why?

Comparison of crowbar currents

Upper device current for the transistor level model; ideal PDS



10 pF load – Blue 1 MΩ (open circuit) – Green

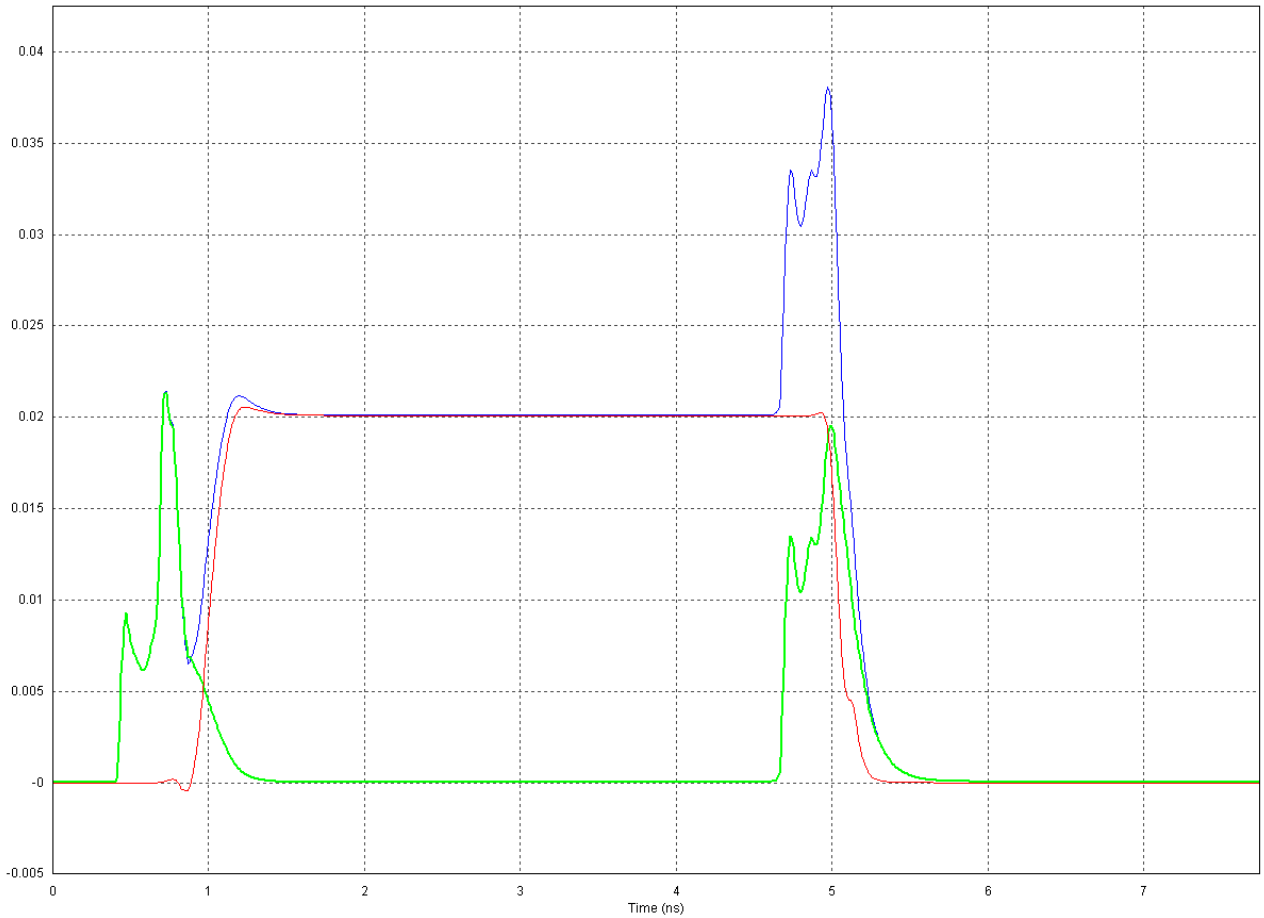
This slide compares the final stage's crowbar current at the high-to-low transition at 5ns. All loads are fully charged to VDDQ before the transition begins, thus the upper device current is the crowbar current.

The crowbar current of the final drive stage is dependent on the I/O loading condition. Therefore, the problem remains that IBIS simulators will have to extrapolate the crowbar current for arbitrary loading conditions that are not provided in the IBIS file.

At this point, it is unclear how this will be implemented from an algorithmic point of view, as the present-day scheme must be improved to incorporate the new data.

Pre-driver Current Extraction

Extraction with 50 Ohms to GND loading; ideal PDS



Total VDDQ current – Blue Pullup current – Red Pre-driver current – Green

This paper will examine the results for a 10 pF I/O loading condition, as it is different from the BIRD95 extractions.

To eliminate any double counting of crowbar current, only the pre-driver current was added to the IBIS current.

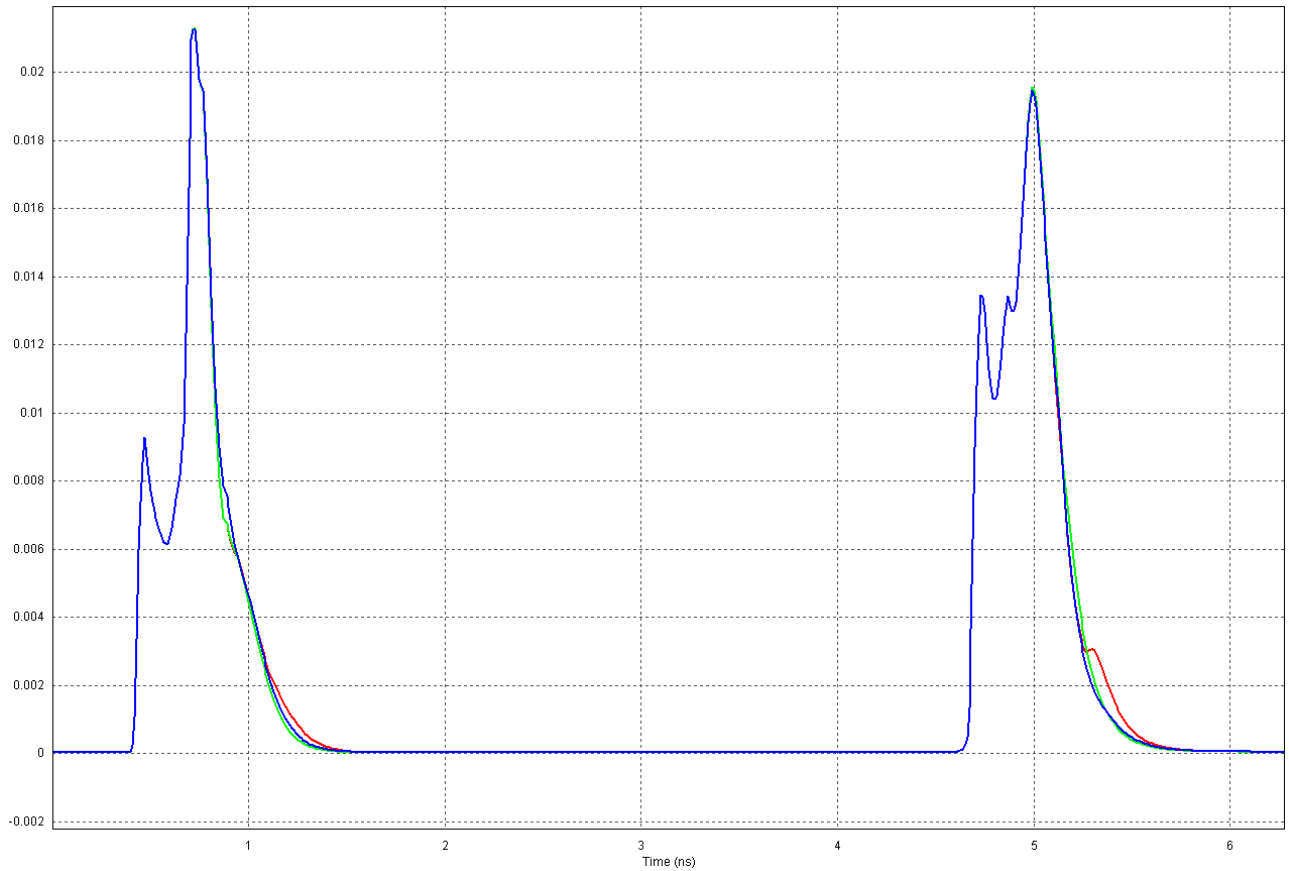
Pre-driver current =
Total VDDQ current –
final drive stage current

These currents were obtained through HSPICE transistor level simulations.

Again, note that any crowbar current in the final drive stage will be calculated by the IBIS simulator.

Pre-driver Current Comparison

All BIRD95 recommended loading conditions; ideal PDS



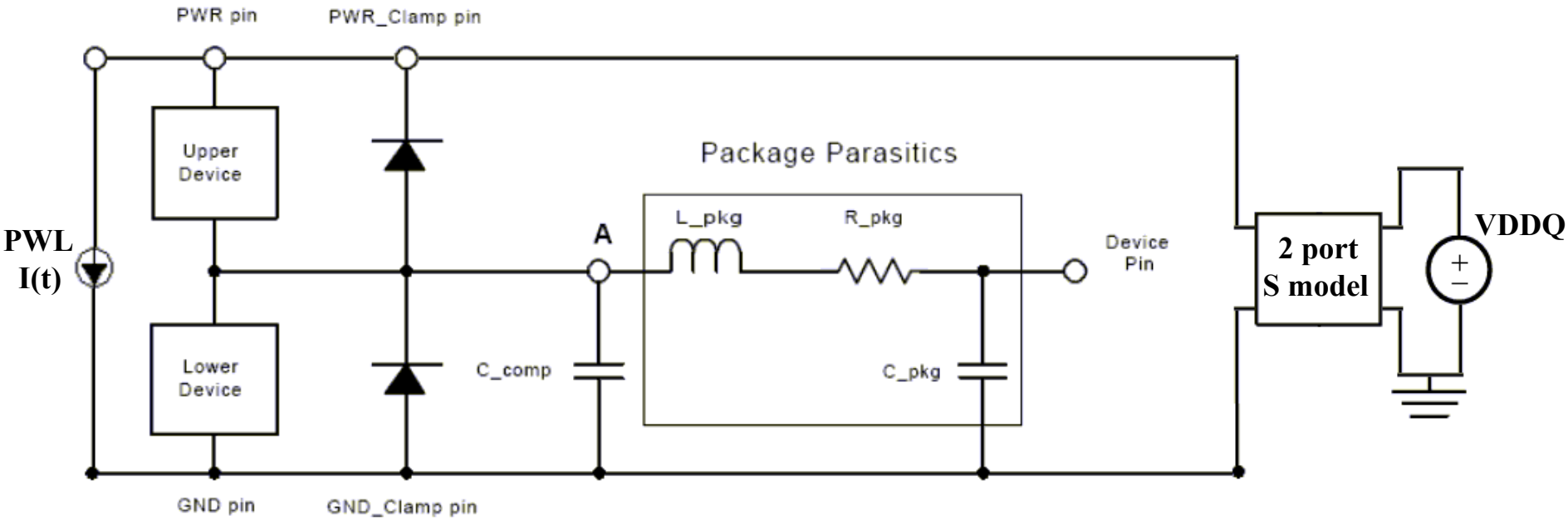
50 Ω to GND – Green 50 Ω to VDDQ – Blue 1 MΩ to GND – Red

For this buffer model, the pre-driver currents were extremely similar for all loading conditions. This is reasonable for pre-driver circuitry that only drives the gates of the final drive stage – their loading is independent of the I/O load.

As the currents were very similar, it appears that scaling is rather unnecessary for this case. Therefore, the 50 Ω to GND pre-driver current was used in the rest of this paper's analysis.

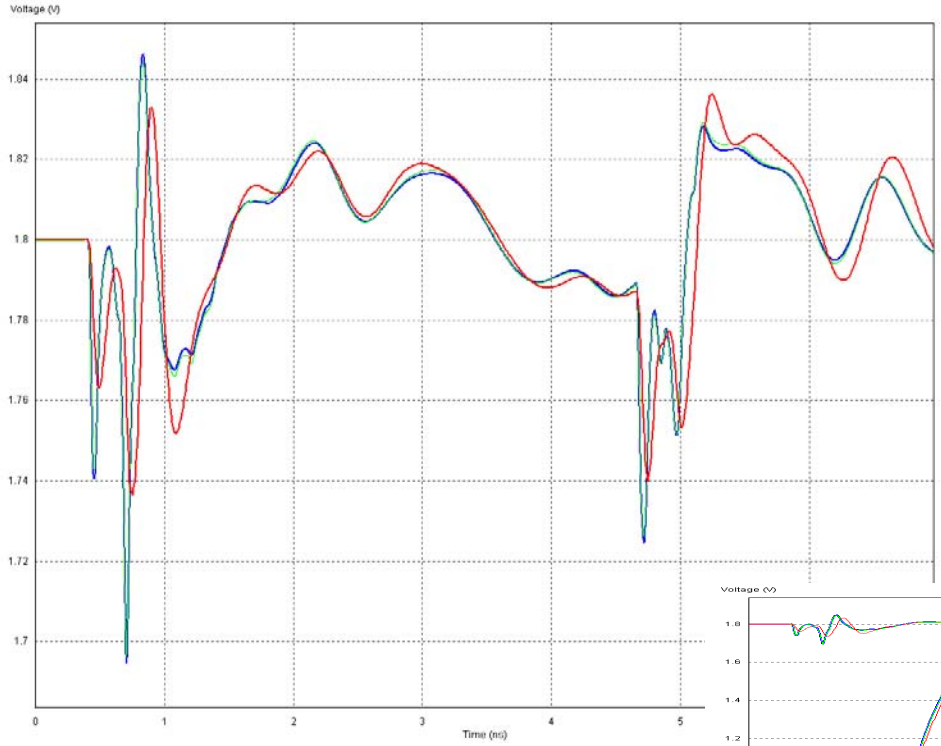
The BIRD95 recommendations align with the V(t) extraction methodology, which minimizes the difficulty in parasitic current extraction.

Improved IBIS model with Pre-driver Current



- The pre-driver current is added in parallel with the pullup/pulldown
- A PWL current source was used to implement the extracted pre-driver current. It was aligned in time with the stimulus pulse.
- A realistic PDS was modeled by a 2-port S parameter element

Voltage waveforms for the new methodology

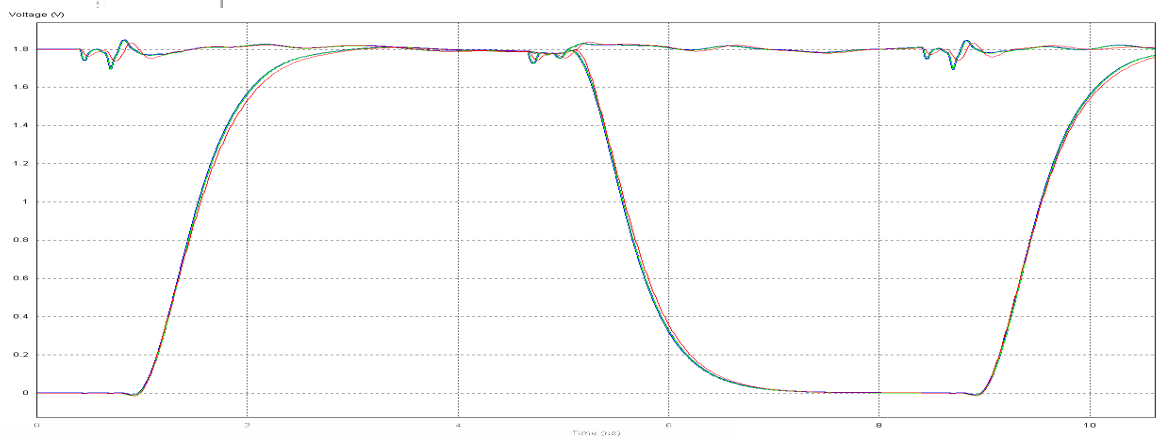


The new IBIS methodology is now able to model the pre-driver and final drive stage currents. Correlation with the SPICE results is significantly improved over the IBIS-only results.

Waveforms from both IBIS simulations were very similar. No artifacts were observed.

Note that the IBIS waveforms overestimate the peak-peak SSO magnitude and occur slightly before the SPICE peaks. The cause can be found by examination of the current waveforms.

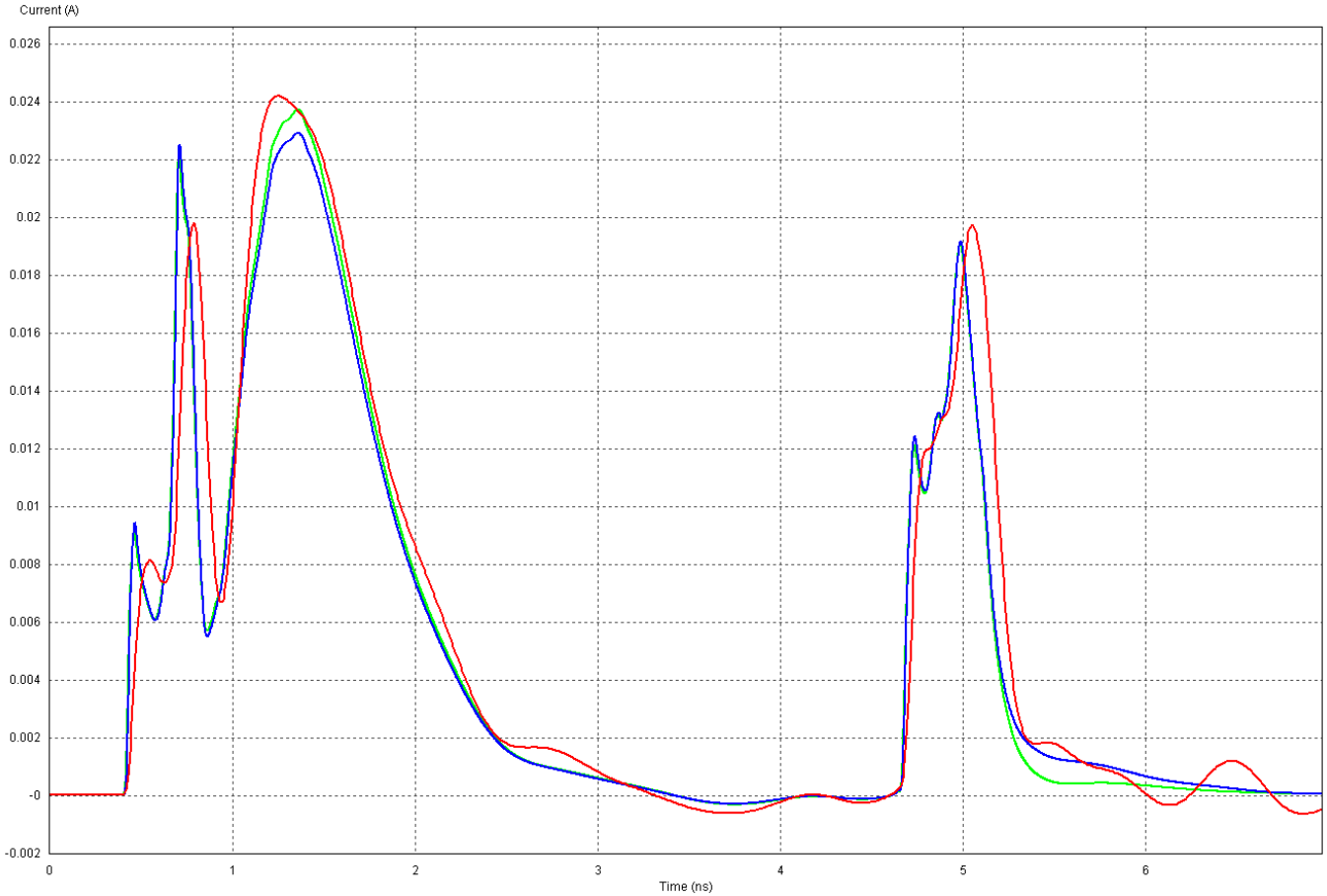
SSO waveforms with realistic PDS, 10 pF driver load, PWL I(t) in parallel with the IBIS device



HSPICE transistor – Red HSPICE IBIS – Green Speed2000 IBIS – Blue

Current waveforms for the new methodology

Total VDDQ current; 10 pF loading; realistic PDS



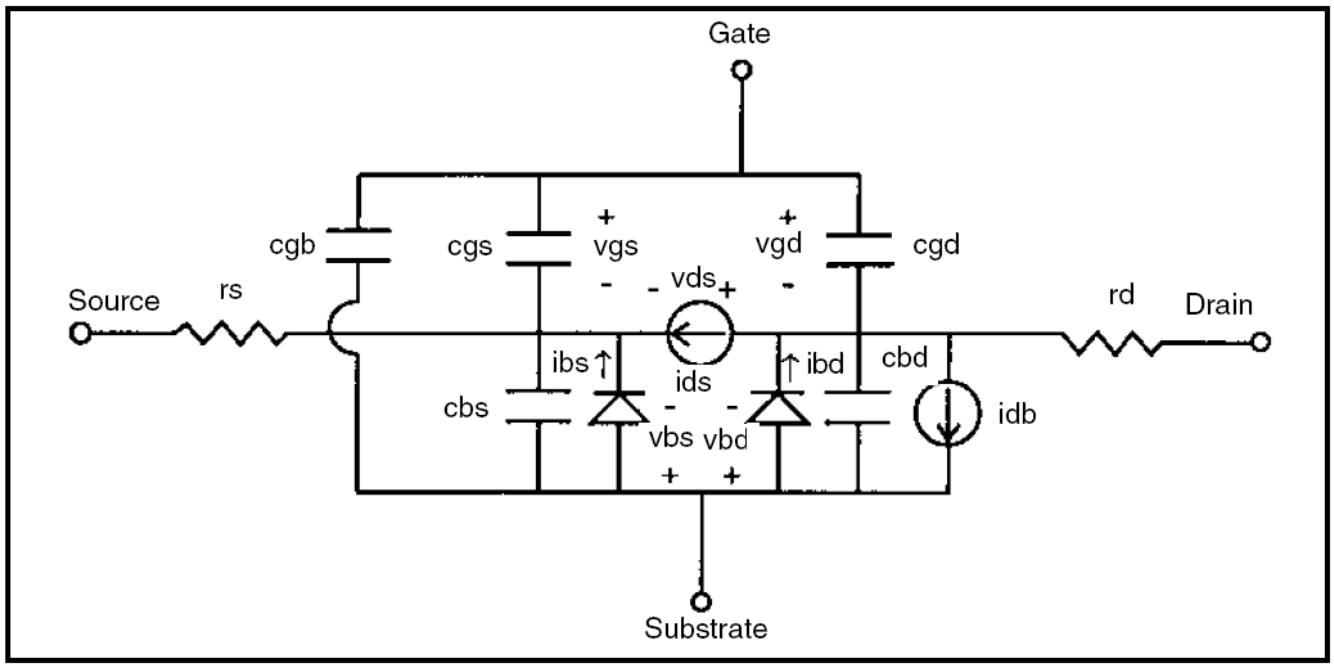
HSPICE transistor – Red HSPICE IBIS – Green Speed2000 IBIS – Blue

The PWL pre-driver current has a higher dI/dt than the realistic pre-driver current. The difference is because the PWL pre-driver current was extracted with an ideal PDS that facilitated the optimistic dI/dt.

The situation can be improved: certain parasitics of the circuit have been overlooked at this point…

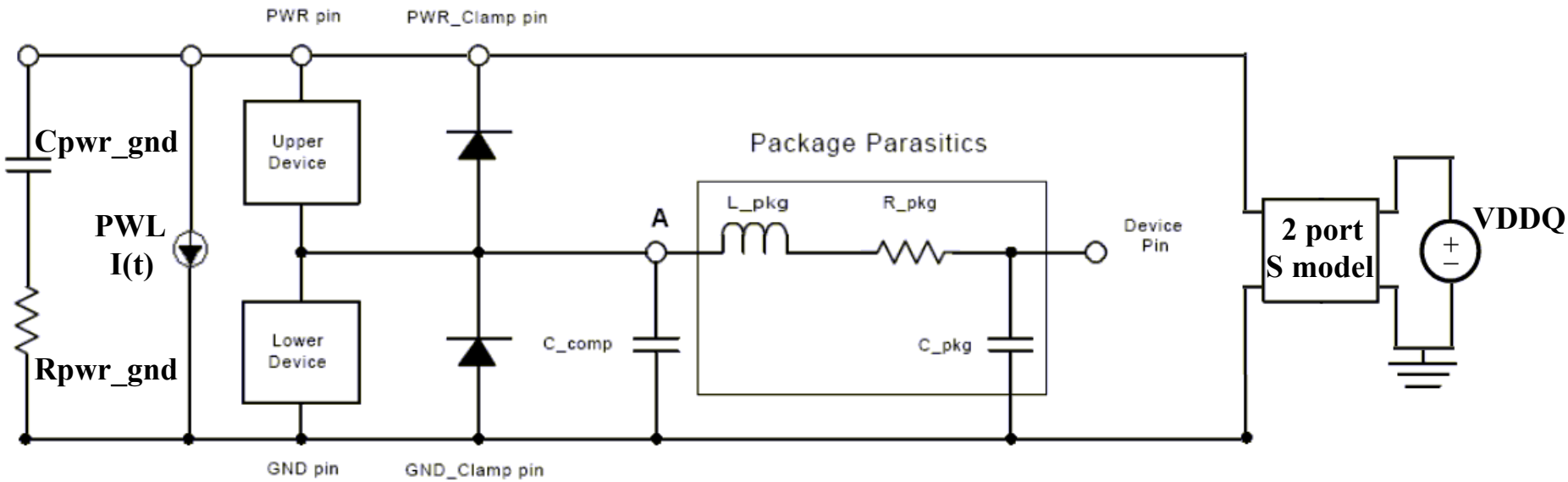
Total current for the two IBIS simulations are very similar. The primary difference is in the crowbar current algorithm.

What is the model missing?



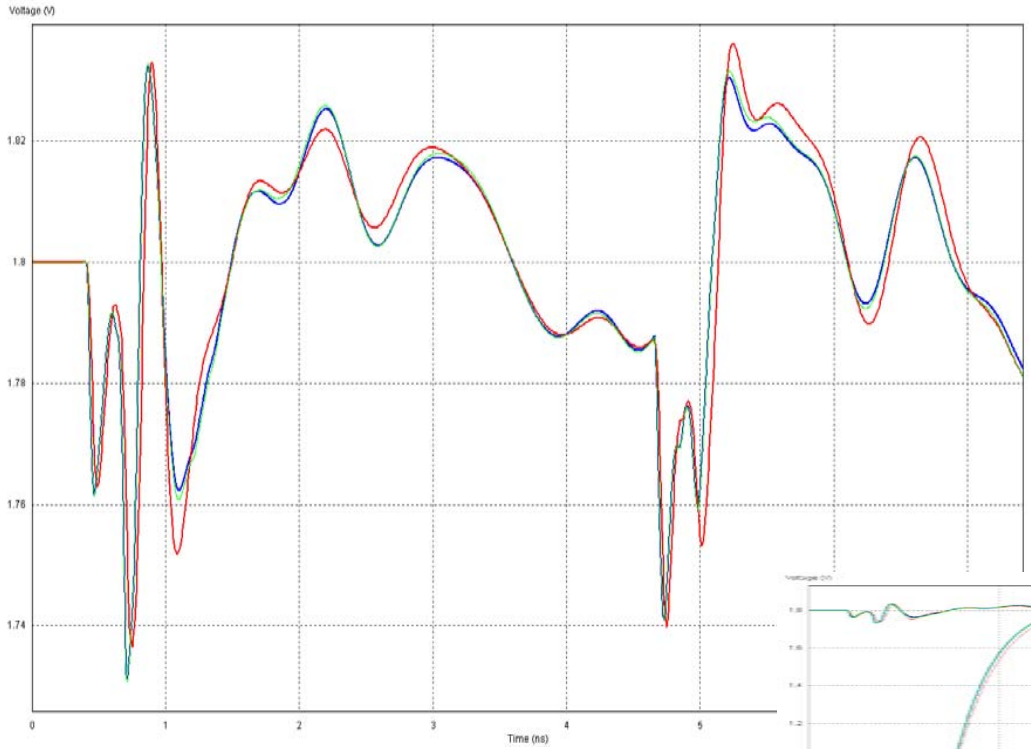
- **Parasitic capacitance exists between all MOSFET terminals**
- **For the I/O pin, this is modeled in IBIS by C_comp**
- **A new compensation capacitor is needed for the power and ground parasitics to maximize SSO correlation with realistic PDS models**

Suggested schematic to maximize correlation



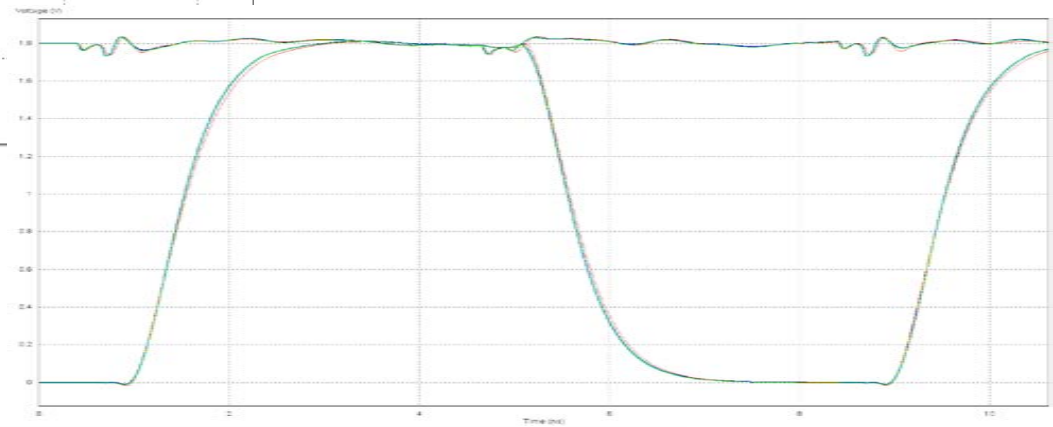
- A frequency domain analysis was performed to determine the impedance between power and ground for the transistor level model
- The impedance was curve fit to a series RC circuit for time domain analysis
- This circuit was added in parallel to the PWL current and IBIS driver

Voltage waveforms for the suggested improvement



The IBIS simulations now show excellent correlation with the SPICE results over the full simulation. With the addition of the RC circuit, the oscillations occur at the proper frequencies and the SSO magnitude is correct.

As before, waveforms from both IBIS simulations were similar and no artifacts were observed.



SSO waveforms with realistic PDS, 10 pF driver load, PWL I(t) and RC circuit in parallel with IBIS device

HSPICE transistor – Red HSPICE IBIS – Green Speed2000 IBIS – Blue

Summary and Observations

- IBIS algorithms attempt to model the crowbar current of the final drive stage
  - Correlation is dependant on load conditions; a new modeling method is definitely needed for highly accurate SSO analysis with arbitrary loading
- BIRD95 shows great promise
  - The parasitic current extractions are relatively easy to generate
  - Pre-driver currents can be accurately modeled with this technique
  - Algorithm research is needed to accurately extrapolate crowbar currents for arbitrary loads that are not explicitly included as parasitic I(t) tables
- A power / ground impedance model is necessary for optimal correlation
- This study only examined an HSTL buffer – additional investigations should be performed on other buffer types for verification (SSTL, PECL, etc.)
- The IBIS-based SSO simulations were significantly faster than SPICE

References and Acknowledgements

[1] Perivand F. Tchrani, Yuzhe Chen, Jiayuan Fang, "Extraction of Transient Behavioral Model of Digital I/O Buffers from IBIS", 46th *IEEE Electronic Components & Technology Conference*, Orlando, May 28-31, 1996, pp 1009-1015.

[2] Ying Wang and Han Ngee Tan,"The Development of Analog SPICE Behavioral Model Based on IBIS Model", *Proceedings of the Ninth Great Lakes Symposium on VLSI*, March 1999.

[3] Raymond Y. Chen, "Adding On-Chip Capacitance in IBIS Format for SSO Simulation", *IBIS Summit*, February 2004.

[4] "HSPICE MOSFET Models" User Manual, Synopsys, September 2004.

Many thanks to Cisco Systems, Inc. for providing the SPICE and IBIS models used in this analysis and especially to Dr. Zhiping Yang for his invaluable ideas and discussions.

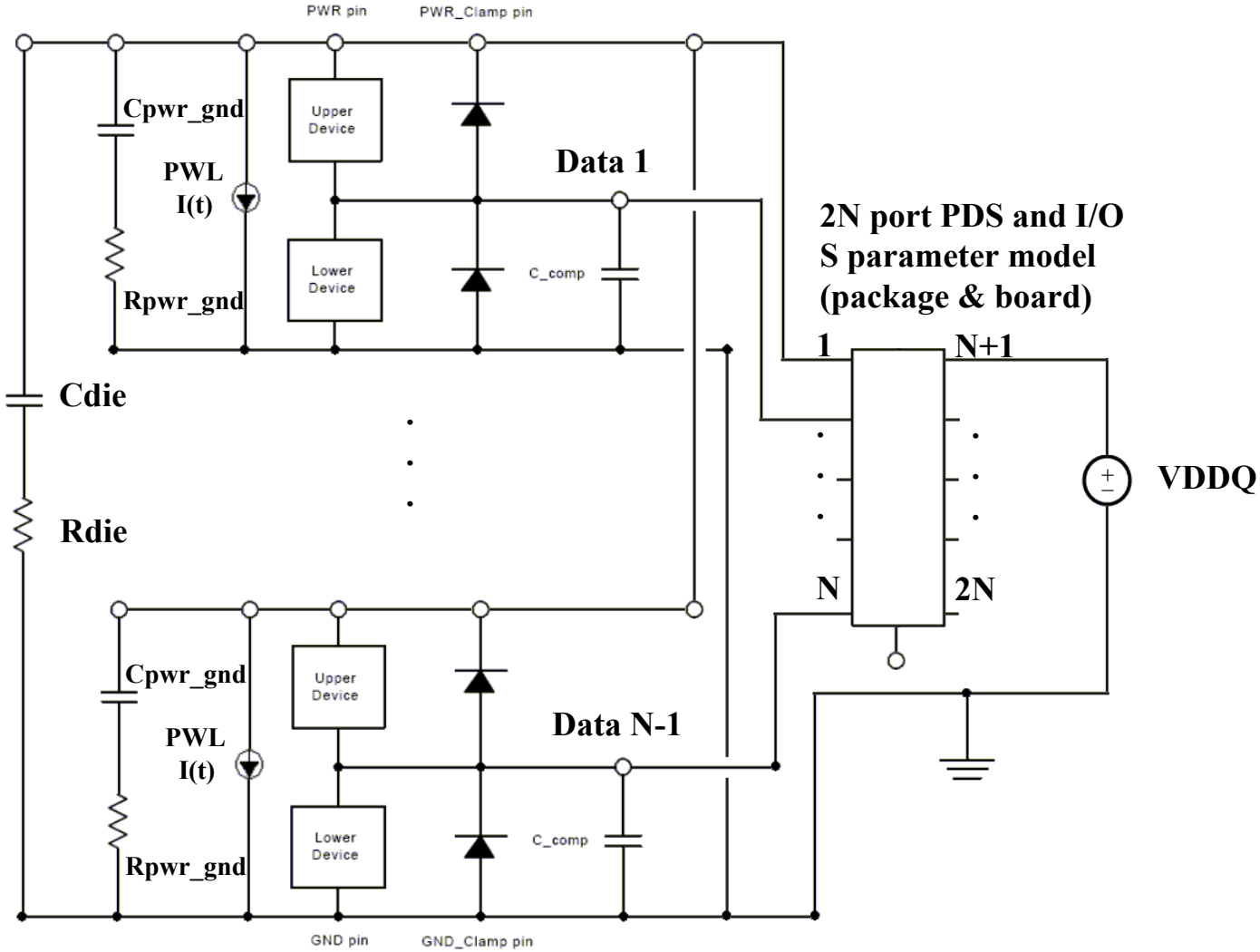
Appendix

- System-level SSO schematic
- Procedure used to obtain Cpwr_gnd and Rpwr_gnd

System-level SSO schematic

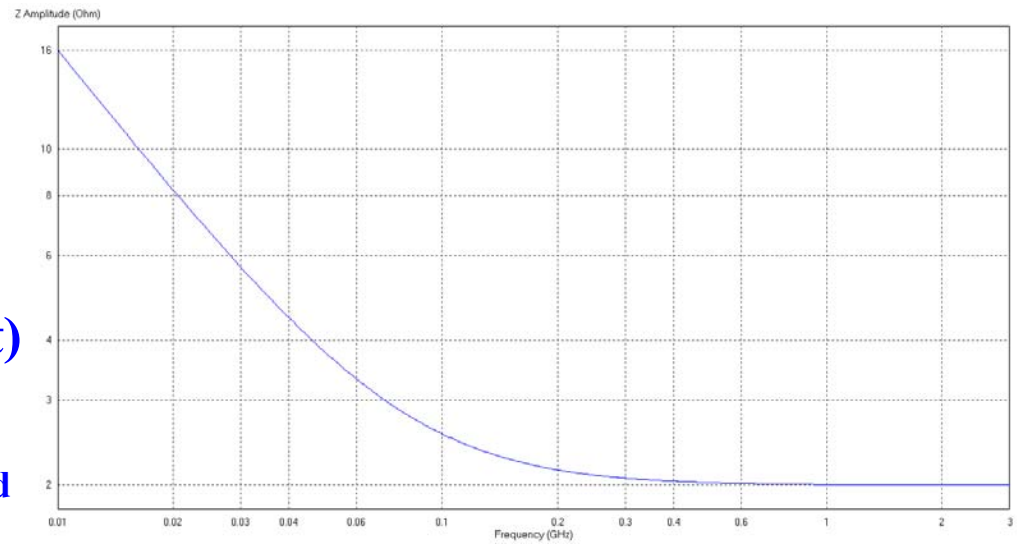
Cdie and Rdie model the total on-die capacitance.

These elements are different from the "unit cell" R and C parasitics.



Procedure used to obtain Cpwr_gnd and Rpwr_gnd

- **Perform an AC sweep on the SPICE circuit**
  - **Connect a voltage source across the power & ground SPICE terminals**
  - **Sweep the voltage source over an appropriate frequency range**
  - **Measure the current through the voltage source**
  - **Calculate Z(f) based on this current: V(f) = I(f) x Z(f)**
- **Fit Z(f) to an appropriate time domain model by inspecting Re[Z] and Im[Z] (series R and C for this circuit)**



Note that this impedance curve is for reference only. It is not the impedance that was measured in this study.