IBIS in the Design Chain of Noise Modelling

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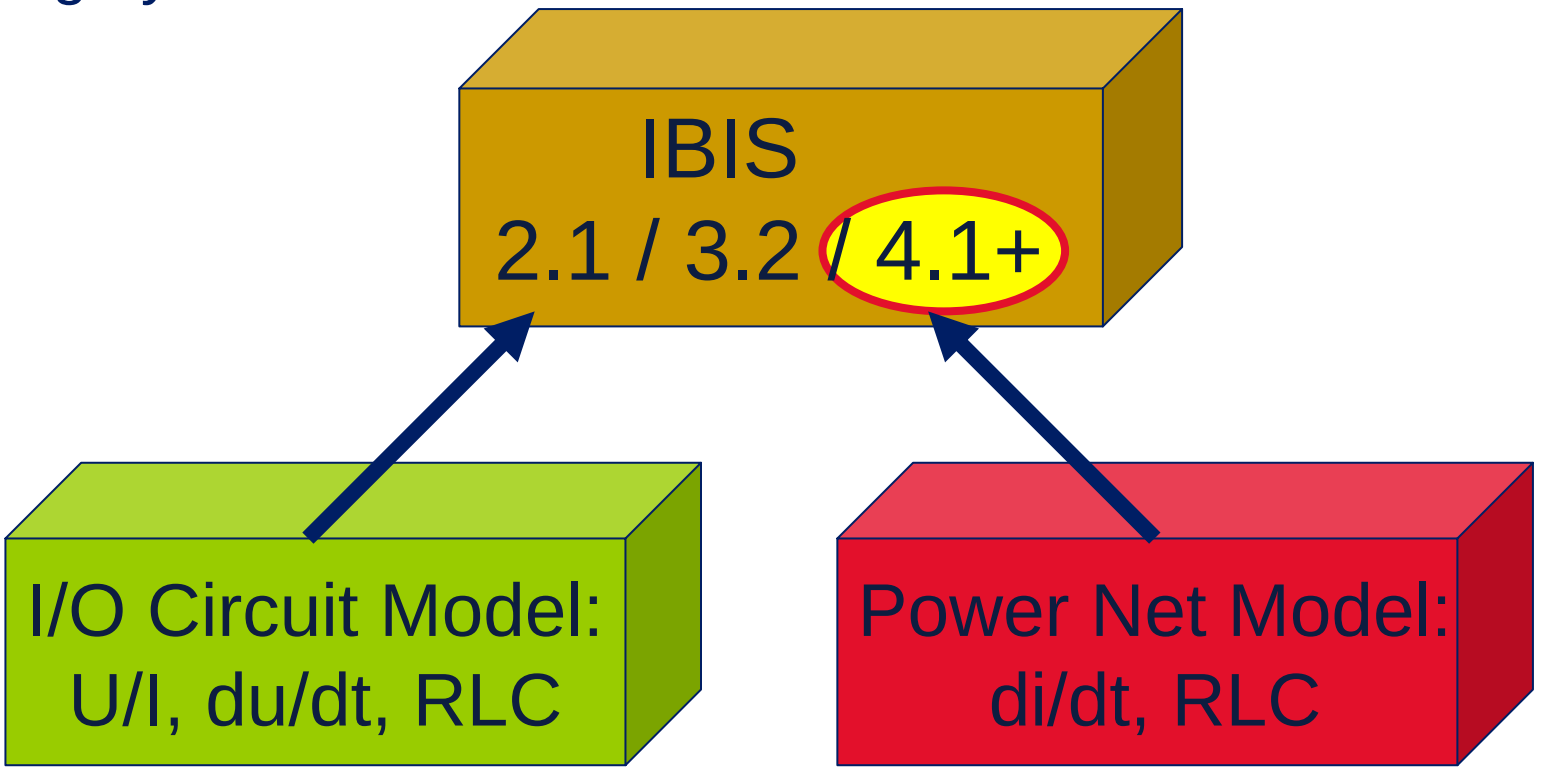
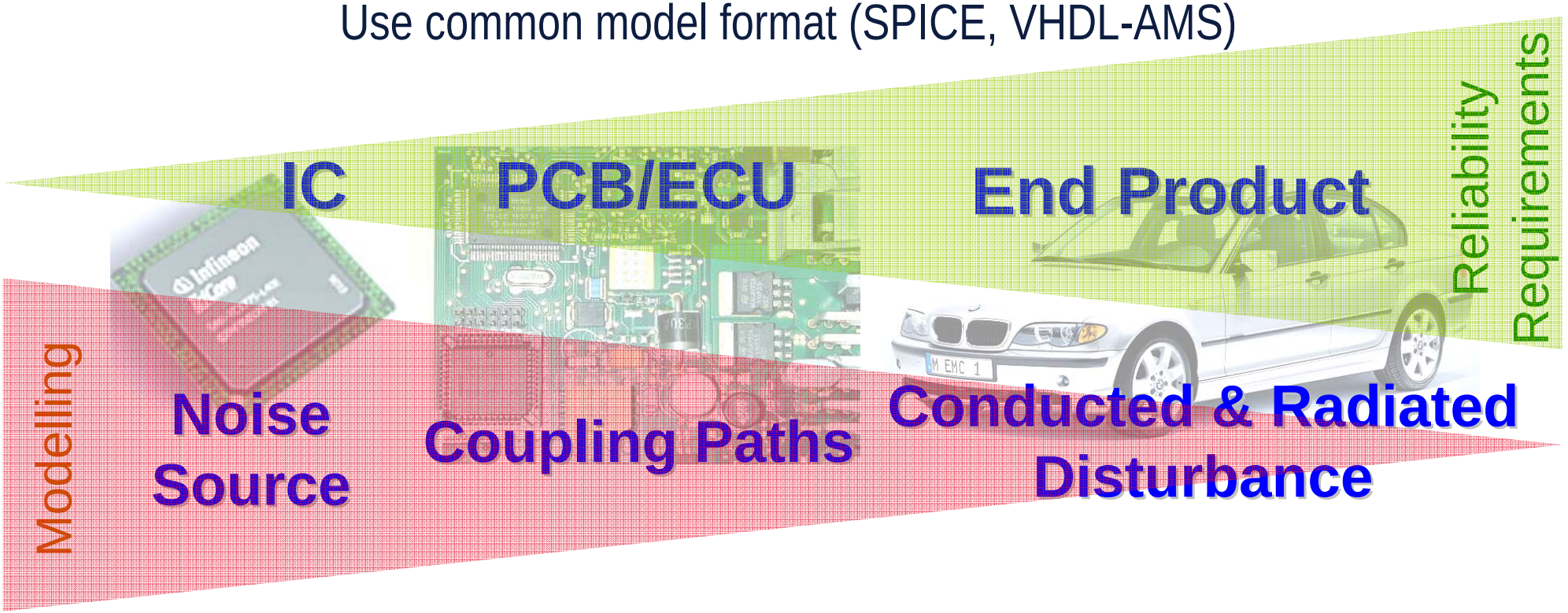
Motivation

- Signal Integrity ✓
- Power Integrity + EMI !



Design Chain

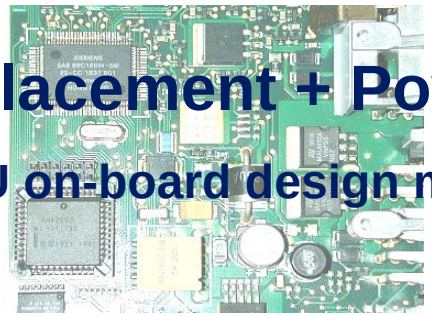
- Goal = High reliability of end customer products
- Process = Reliability requirements for all components (top-down)
  Standardized EMI Models along design hierarchy (bottom-up)
  Use common model format (SPICE, VHDL-AMS)



Model Hierarchy (1)

- **Level „IC“ (Chip Floorplan + IC Package):**
  - **Minimize EMI by on-chip design measures and block place+route**
  - **Minimize EMI by in-package design measures and substrate routing**

- **Level „ECU“ (IC Placement + Power/Signal Routing):**
  - **Minimize EMI by ECU on-board design measures and IC place+route**

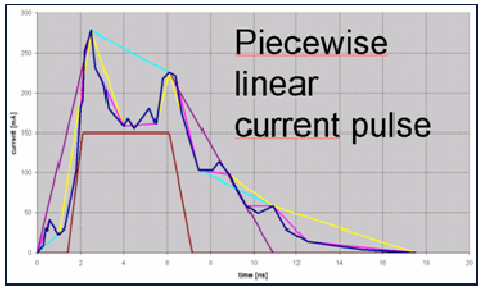


- **Level „Car“ (ECU+Antenna Placement + Harness Routing):**
  - **Minimize EMI by in-car design measures and improved control unit position & harness interconnects**

Model Hierarchy (2)

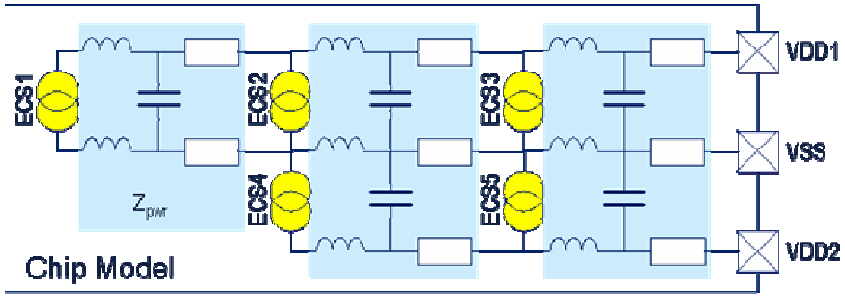
- **Level „IC“ (Chip Floorplan + IC Package):**
  - **ECS = Equivalent current source, describes i(t) of every IC function block**
  - **CEM = All ECS of a chip, connected by RLC of on-chip power networks**
  - **ICEM = Chip (CEM) as „black box“ + RLC of IC package**

i(VDDx) = i(t)



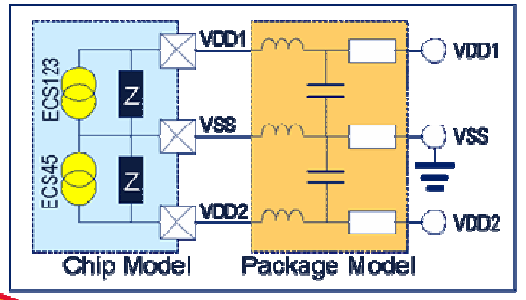
ECS = Equivalent Current Source

i(VDDx) = f [i(t), pwr.net.die]



CEM = Chip Emission Model

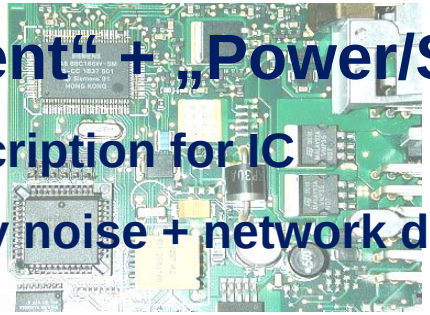
i(VDDx) = g { f [i(t), pwr.net.die], pwr.net.pkg }

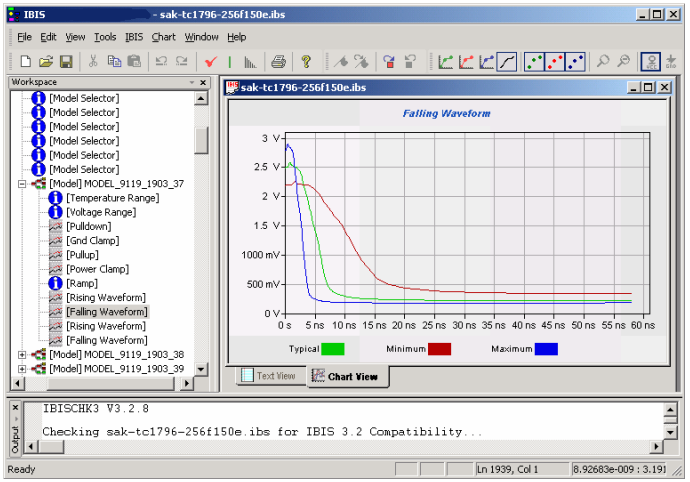


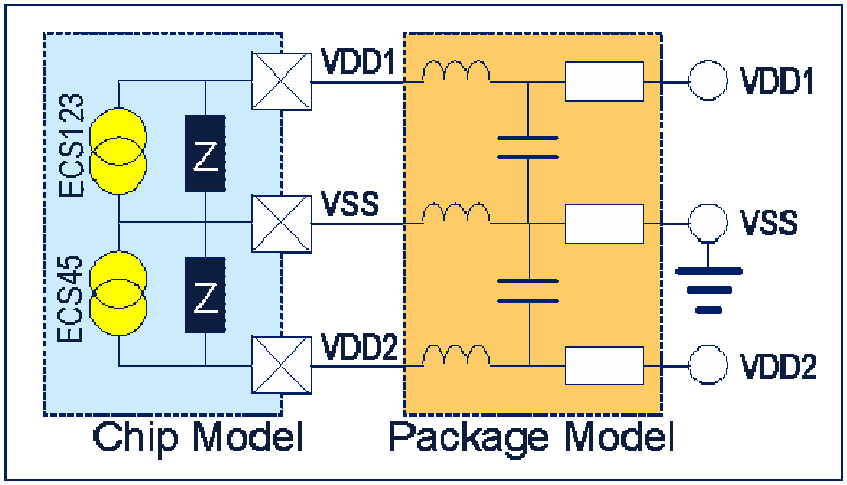
ICEM = Integrated Circuit Emission Model

Model Hierarchy (3)

- **Level „IC Placement“ + „Power/Signal Routing“:**
  - **IBIS = I/O buffer description for IC**
  - **ICEM = Power supply noise + network description for IC**







Model Integration

- ICEM can be integrated into IBIS in two ways:
  - as i(t) table
  - as executable SPICE model
- i(t) table requires IBIS standard extension
- Executable SPICE is supported by IBIS 4.1+
  - Proposals by Bob Ross (2003), Syed Huq et al (2004)

```
| Some additions to the IBIS model:
|*****************************************************************
[Circuit Call]  ICEM
| mapping  port      node
Port_map    vdd_ic    12
Port_map    vss_ic    14
[End Circuit Call]    | Code connecting vdd_ic to pin 12 and vss_ic to
                      | pin 14.
|*****************************************************************
[External Circuit] ICEM
Language SPICE
| Corner     corner_name     file_name      circuit_name (.subckt name)
Corner       Typ             icem_d60.spi   icem_typ
| Ports are in same order as defined in SPICE
Ports        vdd_ic     vss_ic
[End External Circuit]
|*****************************************************************

*  Separate SPICE file icem_d60.spi
*****************************************************************
.SUBCKT icem_typ vdd_ic vss_ic
RVDD Vdd_ic Vdd_n1  2
LVDD Vdd_n1 Vdd_n2  2.2n
Cd Vdd_ic Vss_ic  3.2n
Cb Vdd_n2 Vss_n2  50p
RVSS Vss_ic Vss_n1  2
LVSS Vss_n1 Vss_n2  2.2n
Ib Vdd_n2 Vss_n2 PULSE(0.01 0.4 10ns 1.0ns 1.0ns 0.01ns 31.25ns)
.ENDS icem_typ
*****************************************************************
```

IBIS viewpoint of ICEM Models

- Why ICEM – Model from IBIS viewpoint
  - EMI simulation
  - SI simulation under more realistic Vdd/GND connections
- Model Structure
- Model placement
- What is required in practice?
  - the ICEM – model
  - BIRD95.1(2)
- Conclusions

ICEM Model Structure

- 2 x Current generator
  - different behavior at rising / falling CK-edge
    - different amplitude
    - different pulse width
    - PWL current shape (1. approx. triangle)
  - coupled by variable timing relation ➔ frequency
- RLC package / bonding / die
  - conform to the IBIS specification

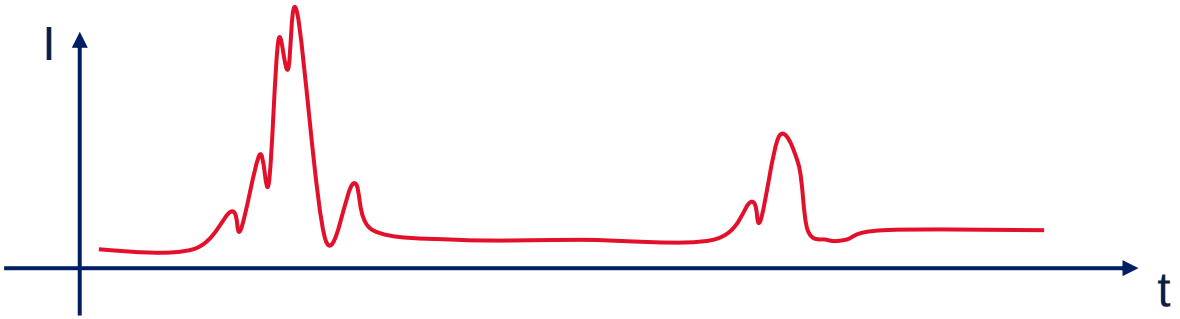
- BIRD95.1 describes the placement of the ICEM model
  - [External Circuit] ICEM_xx
  - [Circuit Call] ICEM_xx

ICEM Model Example

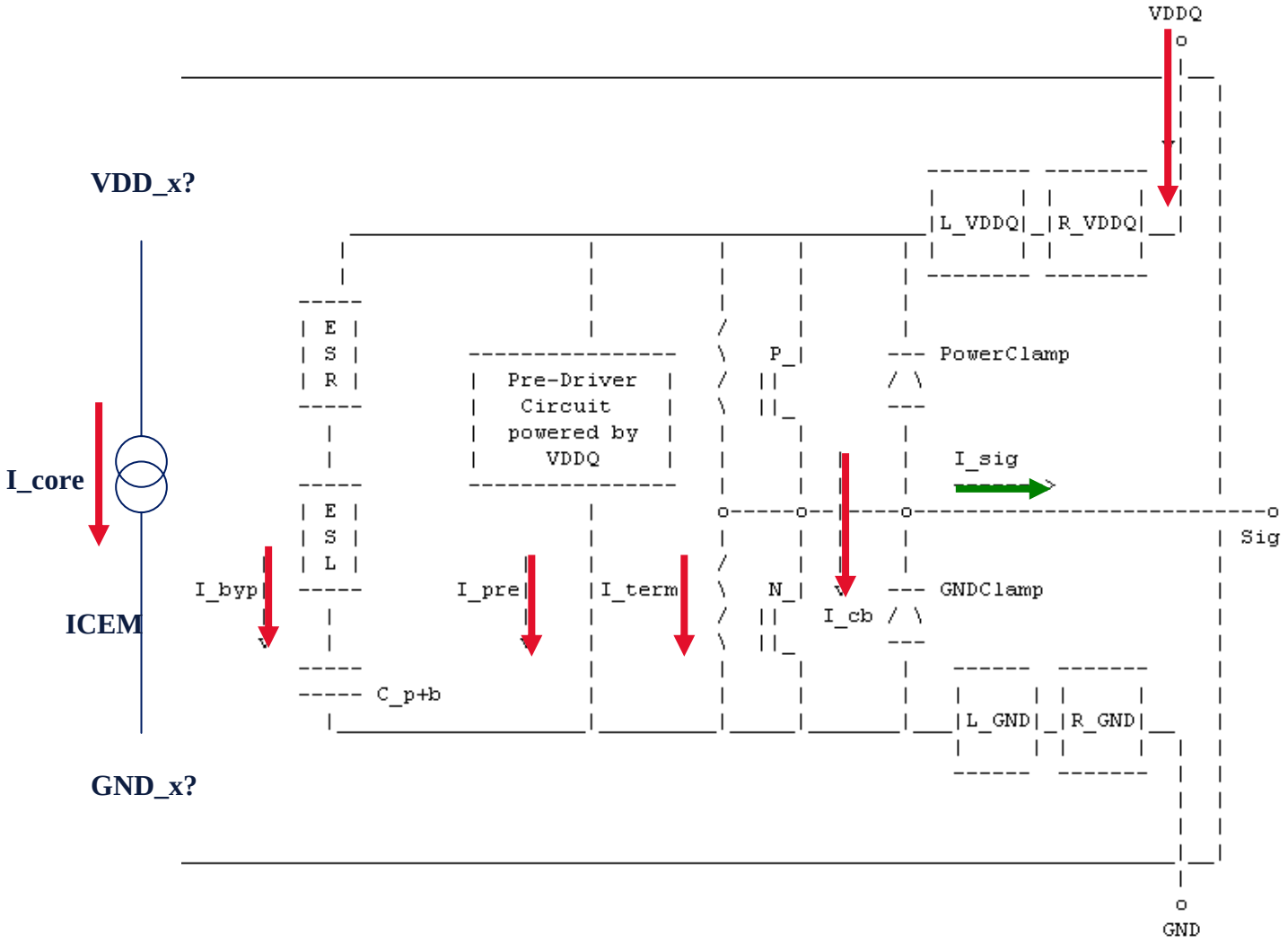
- SPICE subcircuit

```
.SUBCKT ICEM1_typ    vdd_ic   vss_ic   t_dl_12
R_vdd       vdd_ic     vdd_n1     2
L_vdd       vdd_n1     vdd_n2     2.2n
C_d         vdd_ic     vss_ic     3.2n
C_b         vdd_n2     vss_n2     50p
R_vss       vss_ic     vss_n1     2
L_vss       vss_n1     vss_n2     2.2n
I_b1        vdd_n2     vss_n2     PULSE (0.01  0.4  10ns            1.0ns  1.0ns  0.03ns 31.25ns)
I_b2        vdd_n2     vss_n2     PULSE (0.01  0.3  ‚10ns+t_dl_12‘  1.0ns  1.0ns  0.01ns 31.25ns)
.ENDS ICEM1_typ
```

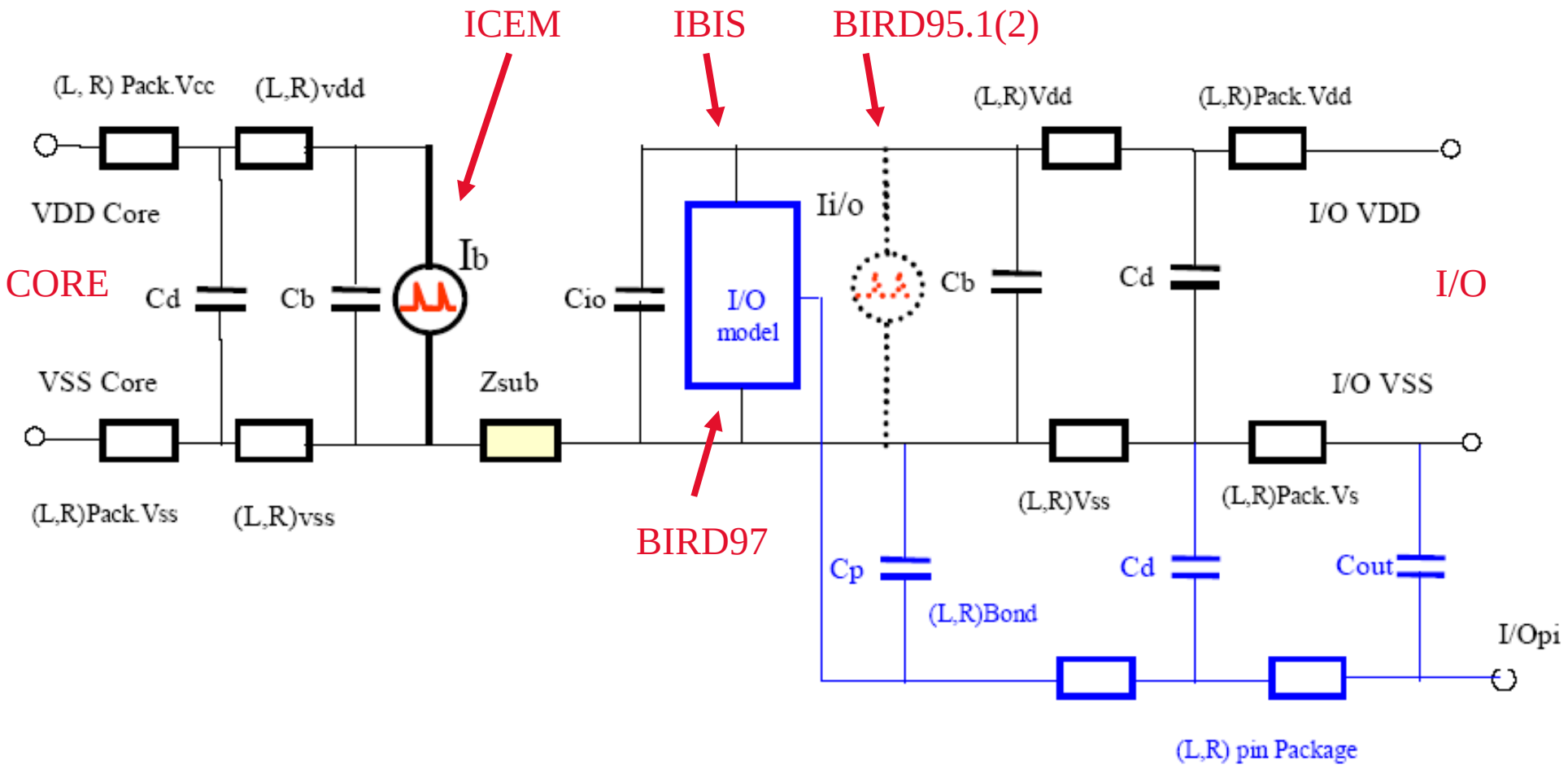
- PWL table



BIRD 95.1(2)


VDDQ
VDD_x?
L_VDDQ
R_VDDQ
E S R
Pre-Driver Circuit powered by VDDQ
P_
PowerClamp
I_core
I_sig
E S L
I_byp
I_pre
I_term
N_
I_cb
GNDClamp
Sig
ICEM
C_p+b
L_GND
R_GND
GND_x?
GND

Model Placement



Summary and Conclusion

- **ICEM models** in the actual format are suitable to IBIS 4.1+
  - no model modification needed
  - mathematical function or PWL format
  - parameter for ICEM model tuning are possible, but not desired
- **RLC** for *package* + *bonding* + *die* **only** in the IBIS-file
  - to avoid double counting
  - better accuracy required
- **Power/GND-Pin assignment** for **I/O** and **CORE**
  - [Pin Mapping]
- **BIRD 95.1(2)**

➔➔➔ **SI** and **EMI simulation**
more accurate by considering the **I(t)** and **Vdd/GND connections**