IBIS Models: the first step towards High Speed Design Kits

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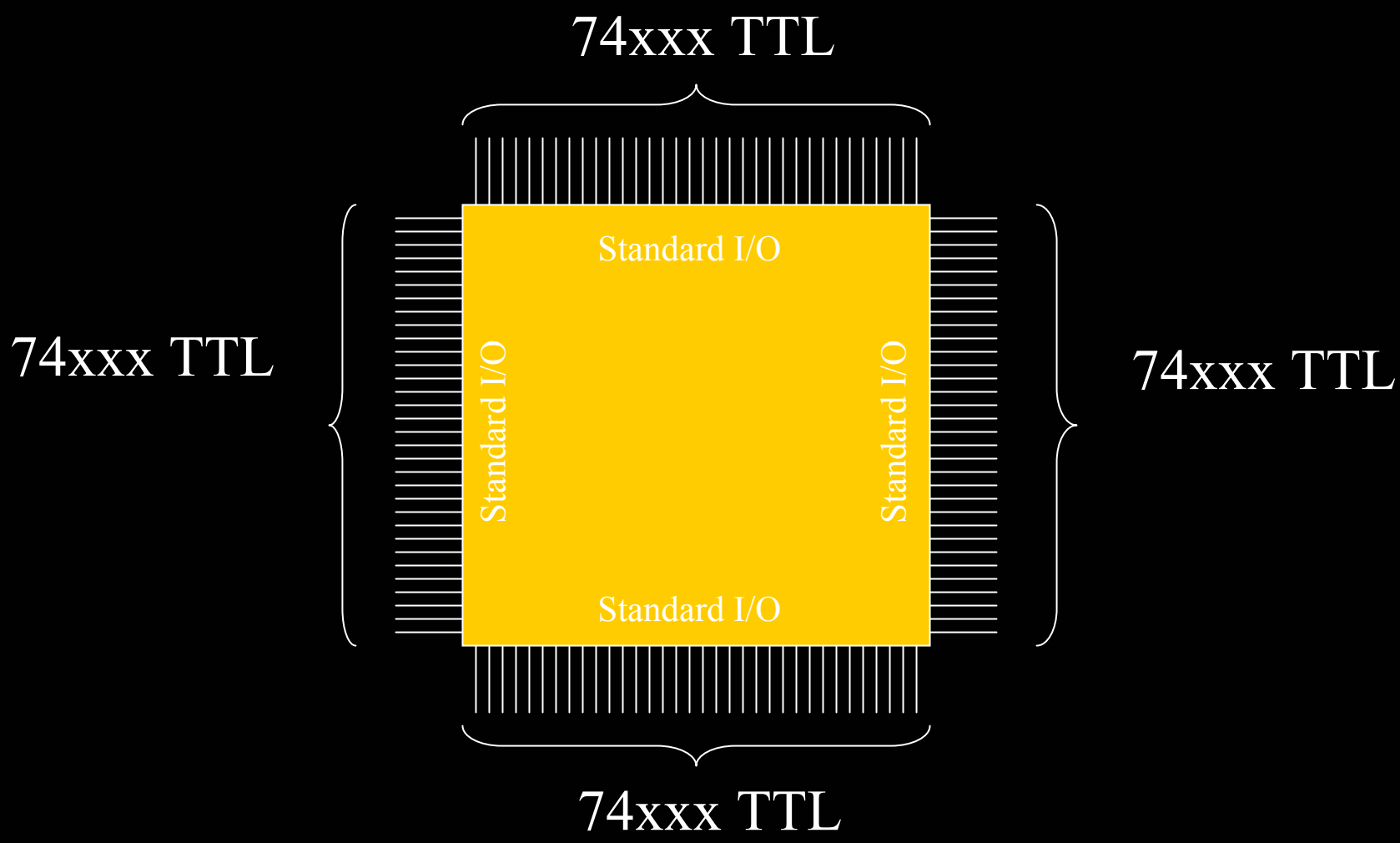
Mentor Graphics®

A Little History …

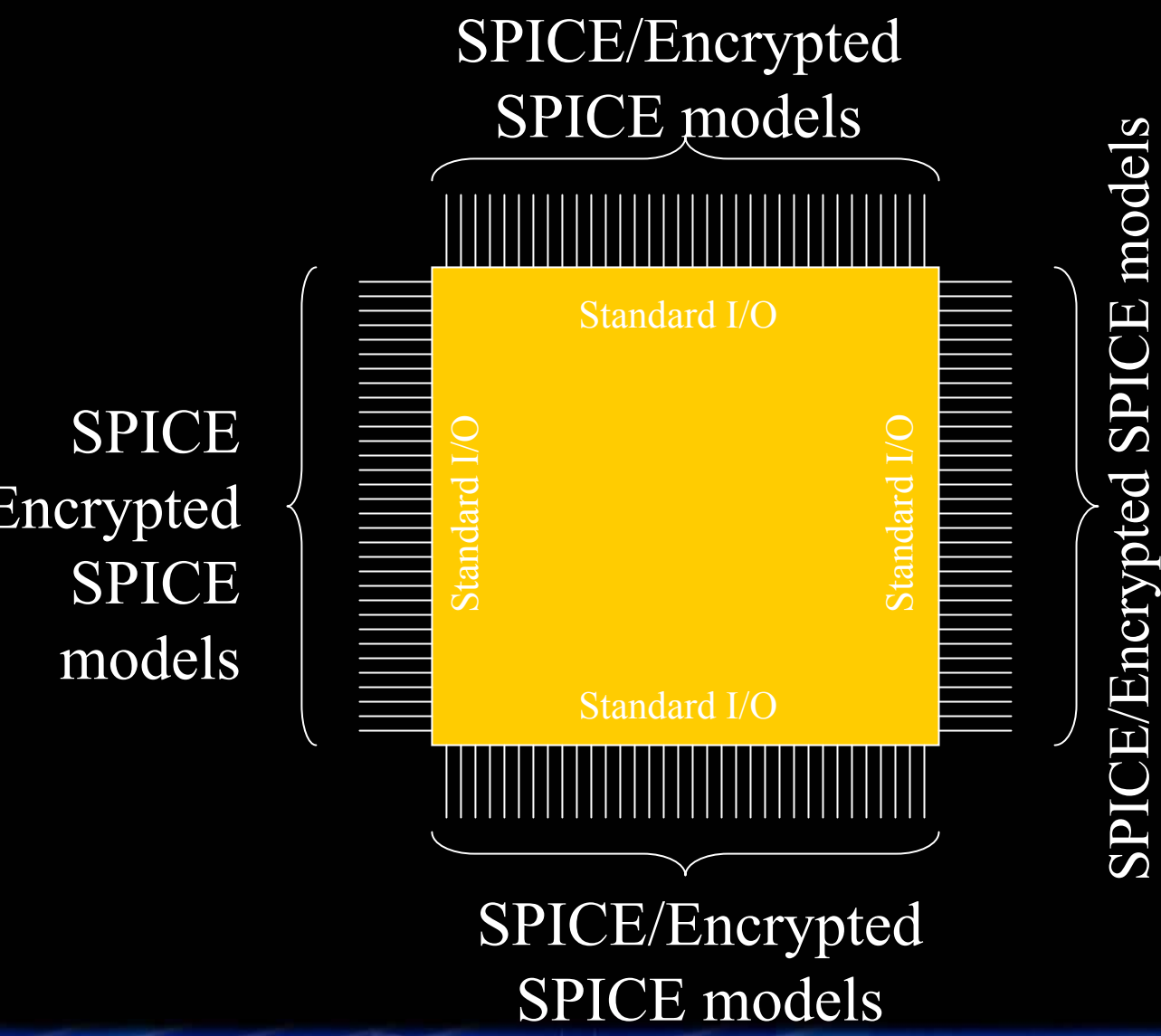
In the Beginning …

1980s



Then, speeds increased …

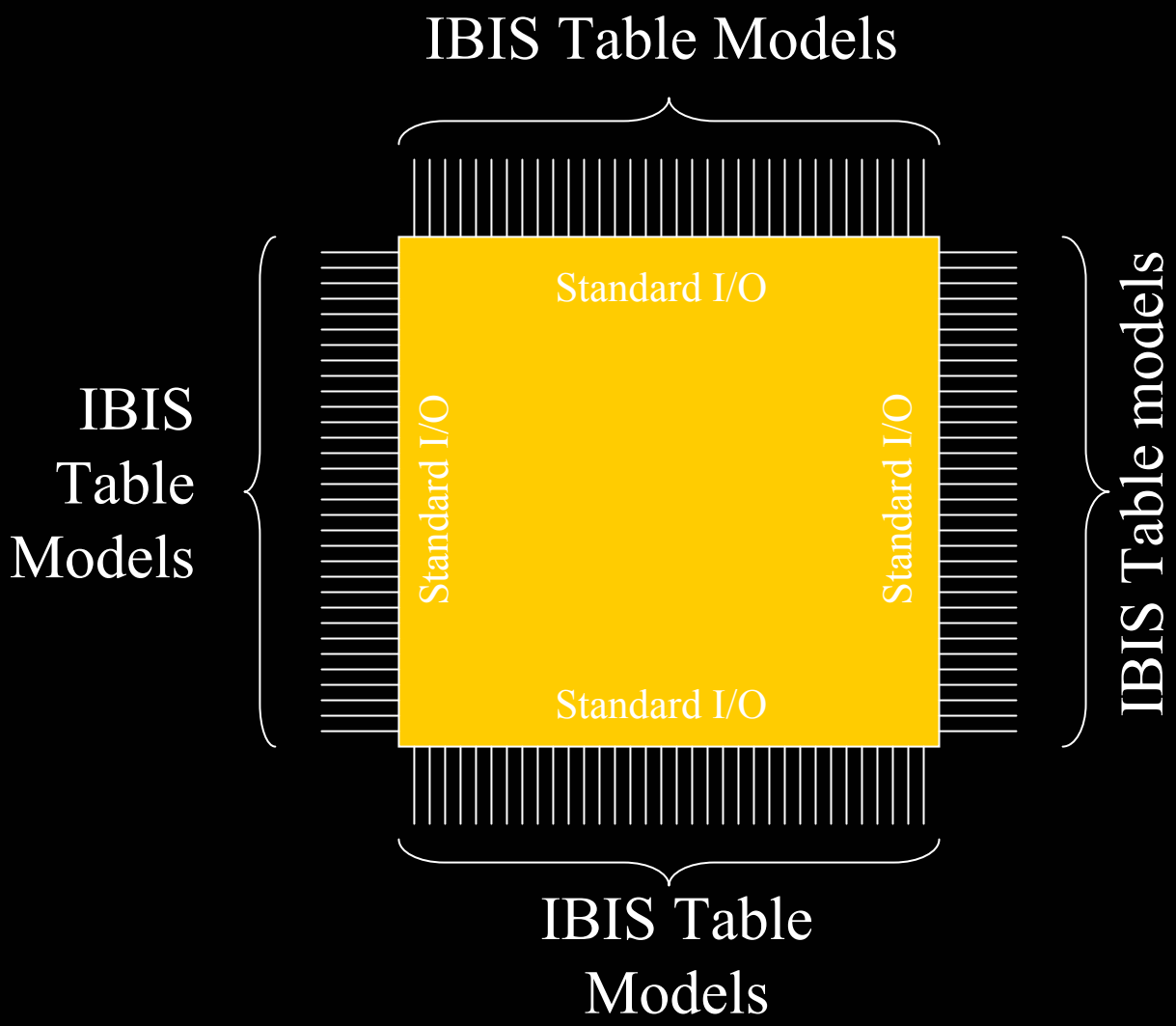
1990



SPICE
- **Slow**
- **Complex**
- **Encrypted**

Then IBIS came to the rescue …

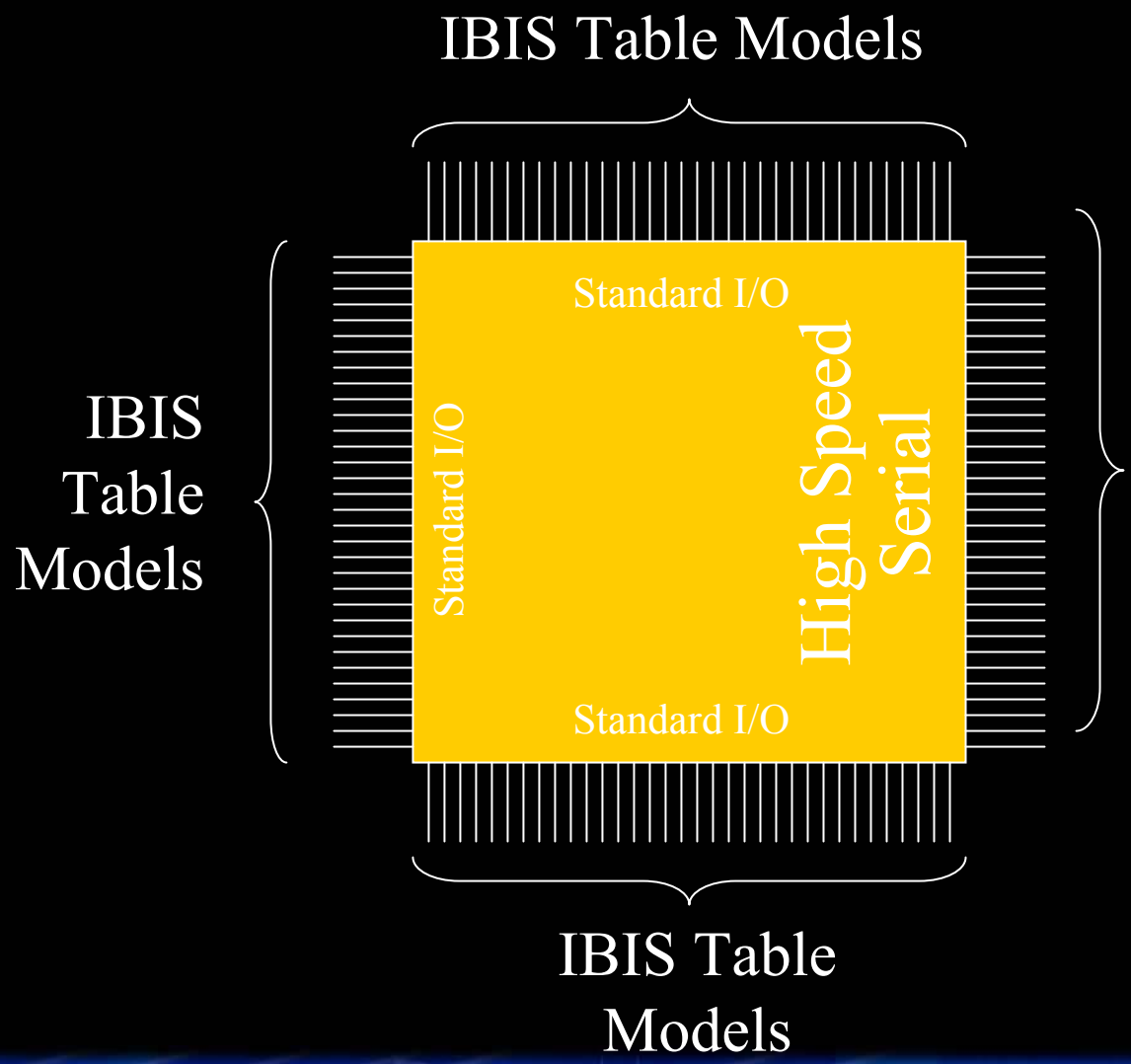
1993



IBIS

- **Fast**
- **Simple**
- **Standard**

Then came High Speed Serial I/O … 2002



SPICE
- **Slow**
- **Complex**
- **Encrypted**

IBIS 4.1 …

2003

IBIS Table Models

IBIS Table Models

Standard I/O

Standard I/O

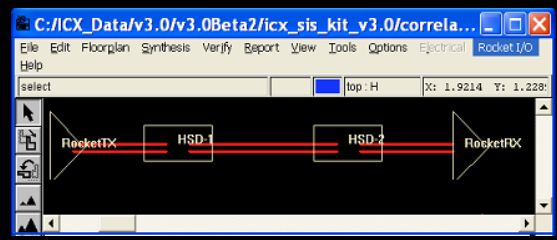
High Speed Serial

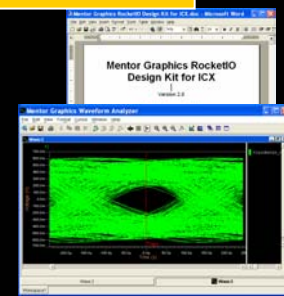
Standard I/O

IBIS 4.1 Wrappers

SPICE Encrypted SPICE Models

IBIS Table Models





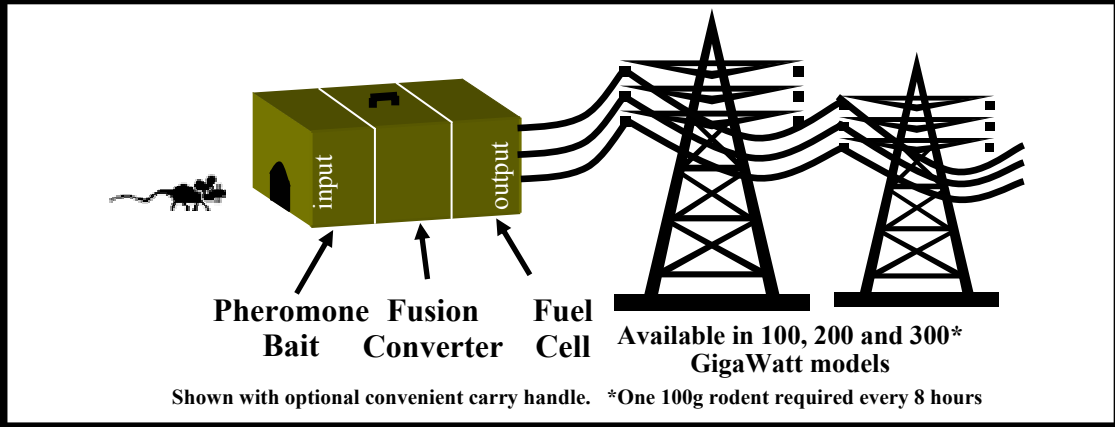
Examples & Documentation

IBIS 4.1 with SPICE

- IBIS
  - Simple to use
  - Fast
  - Unencrypted
  - Standard
- SPICE
  - Complex
  - Slow
  - Encrypted
  - Proprietary
- IBIS 4.1/SPICE
  - Simple 
  - Slow
  - Encrypted
  - Partially Proprietary

Better Mousetraps

IEEE-1076.1 Analog Modeling Language

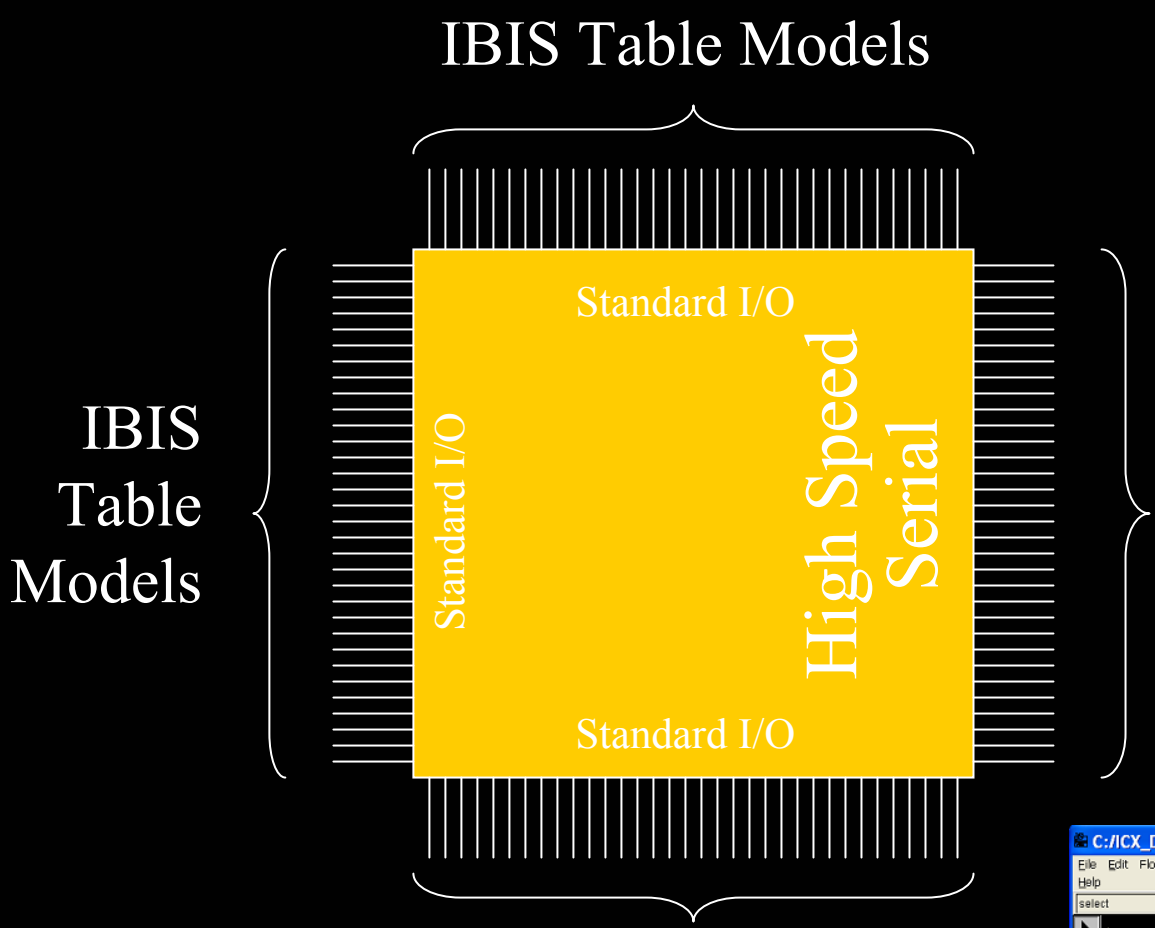


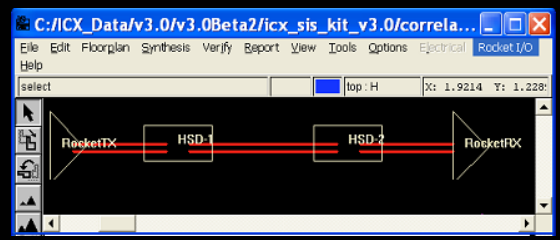

```
library IEEE;
use IEEE.electrical_systems.all;
use IEEE.std_logic_1164.all;

entity sgx_hssi_tx_icx_slow is
  generic (ui_real : real := 320.0e-12);
           type time, internally)
  port (terminal a_drive, a_signal_pos,
     a_signal_neg, pre_emphas2,
     pre_emphas1, pre_emphas0,
     drive_sel2, drive_sel1, drive_sel0,
     termsel1, termsel0 :  electrical);
end entity sgx_hssi_tx_icx_slow;
```

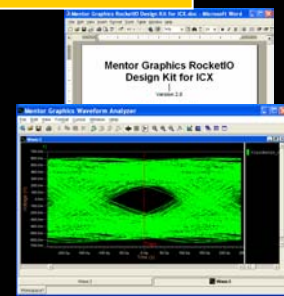
- Solves speed problem
- Shields user from SPICE complexity
- Double IP security
- Industry Standard, Non Proprietary

IBIS 4.1 with IEEE 1076.1 AMS …

2003







Examples & Documentation

IBIS 4.1 with IEEE 1076.1 AMS

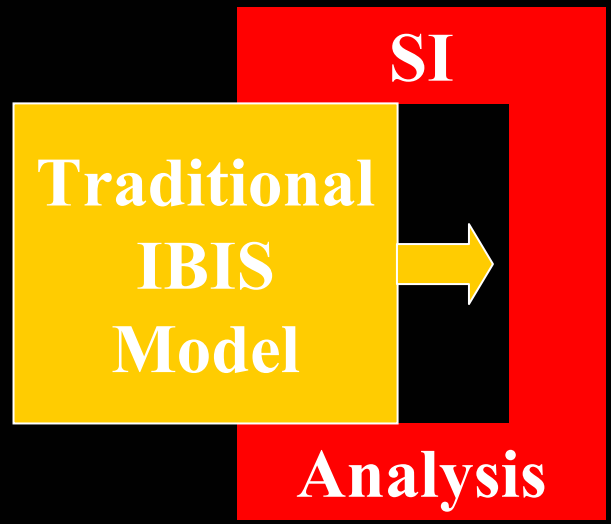
- IBIS
  - Simple to use
  - Fast
  - Unencrypted
  - Standard
- HSPICE
  - Complex
  - Slow
  - Encrypted
  - Proprietary
- IBIS 4.1/SPICE
  - Simple
  - Slow
  - Encrypted
  - Proprietary
- IBIS 4.1/IEEE1076.1
  - Simple
  - Fast
  - Unencrypted
  - Standard

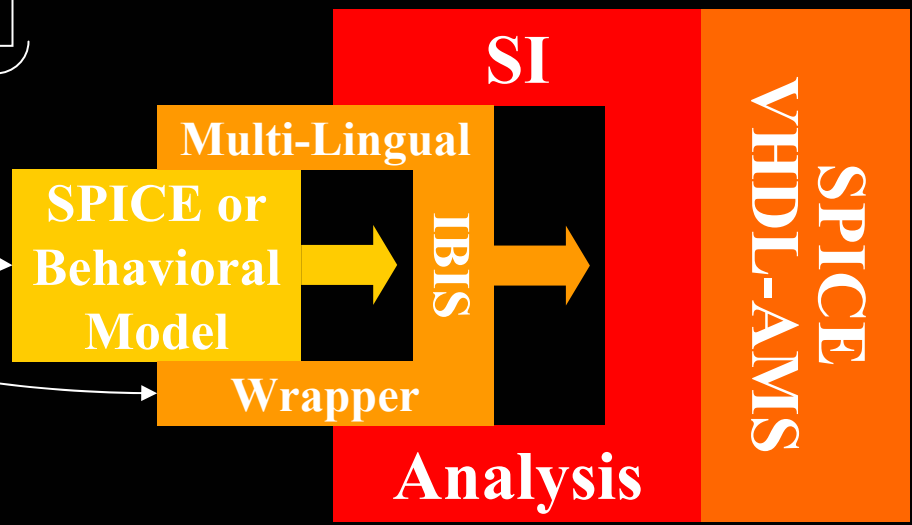
IBIS 4.1 Standard

```
[Pin]
1     dcp          NC
2     dcm          NC
3     bpn          NC
4     bpp          NC
|
|**********************
|
[Diff Pin]
            1      2
            4      3
|
[Series Pin Mapping]
2 3 R_1G_ohm
|

[circuit call] component
port_map inp 1
port_map inm 2
port_map outp 3
port_map outm 4
[end circuit call]

[external circuit] component
language Spice
corner typ comp.sp comp
ports inp inm outp outm
[end external circuit]
```

comp.sp

```
*
.subckt comp
+ inp inm outp outm
*S-parameter model
*RLC SPICE model,
*Transistor model,
*VHDL-AMS Model
.ends
```





What Next ?

- Some more modeling enhancements
- High Speed Design Kits

Symbols

Constraints

Reference Designs

Reuse Blocks

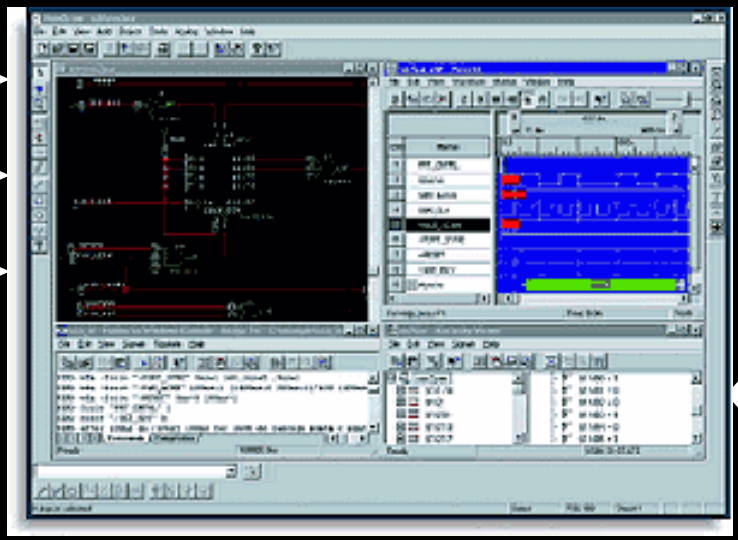
Kit Items

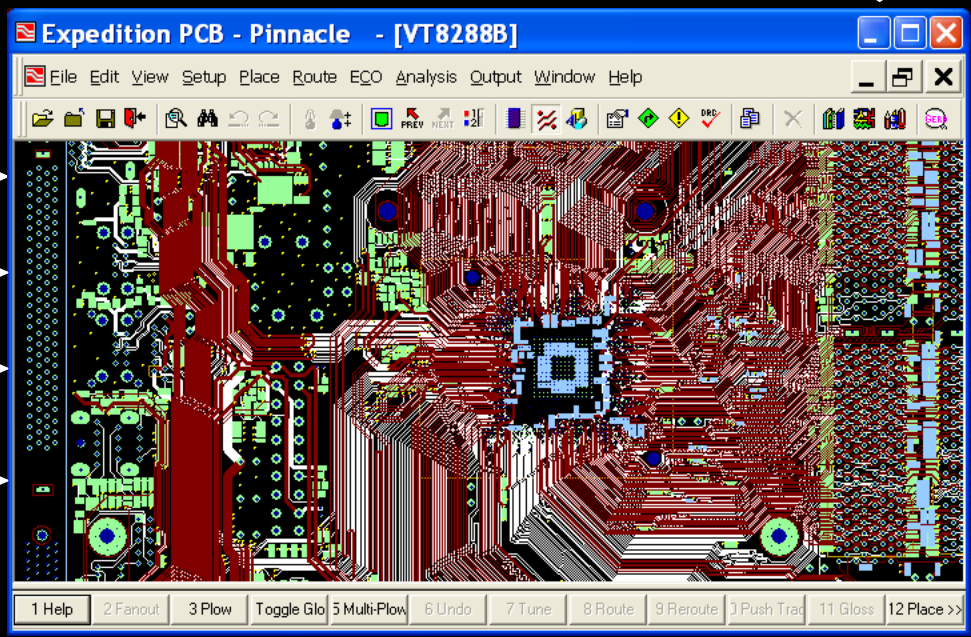
Constraints

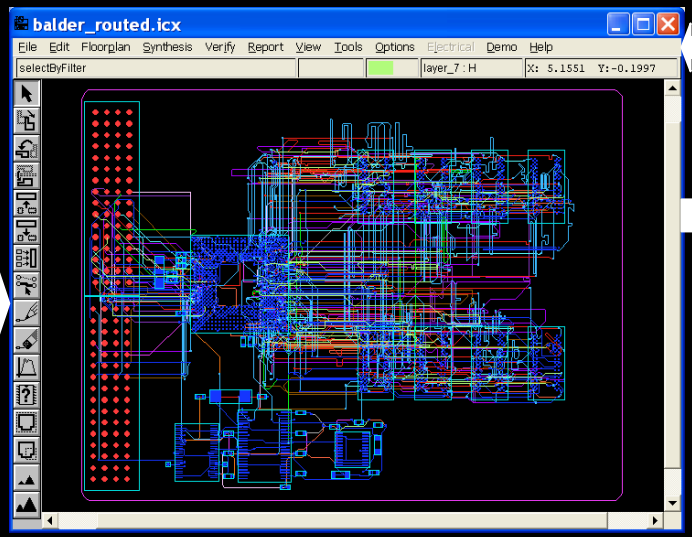
Footprints

Reference Designs

Drop-in Core Layout







Custom Menus

Kit Items

Circuit Description

IBIS Multi-Lingual Wrappers

SI Analysis

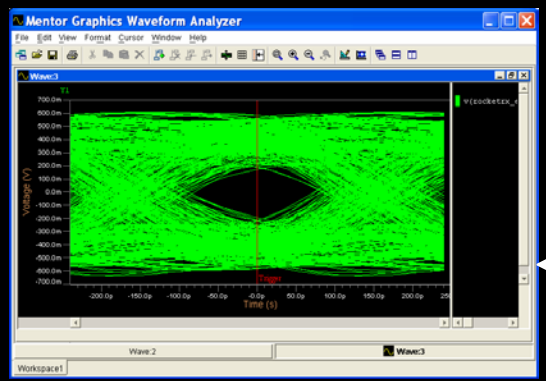
S-Param Models

RLGC Models

Behavioral Models

Transistor Models

IBIS Table Models

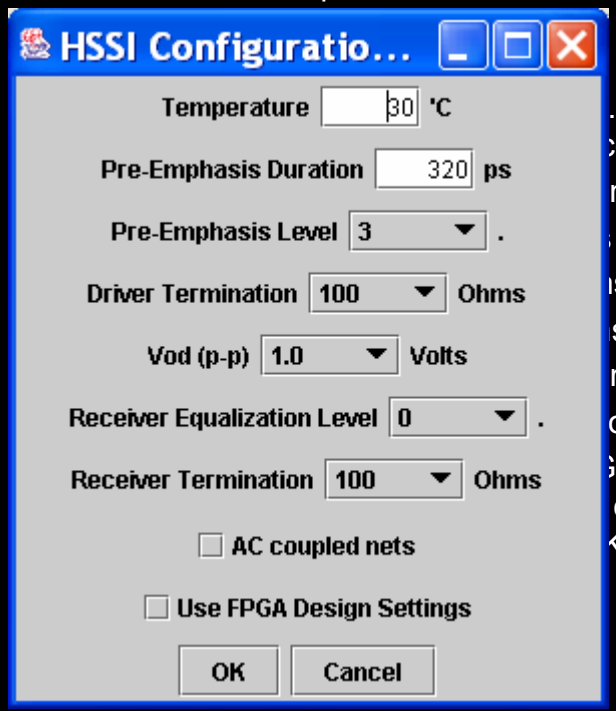


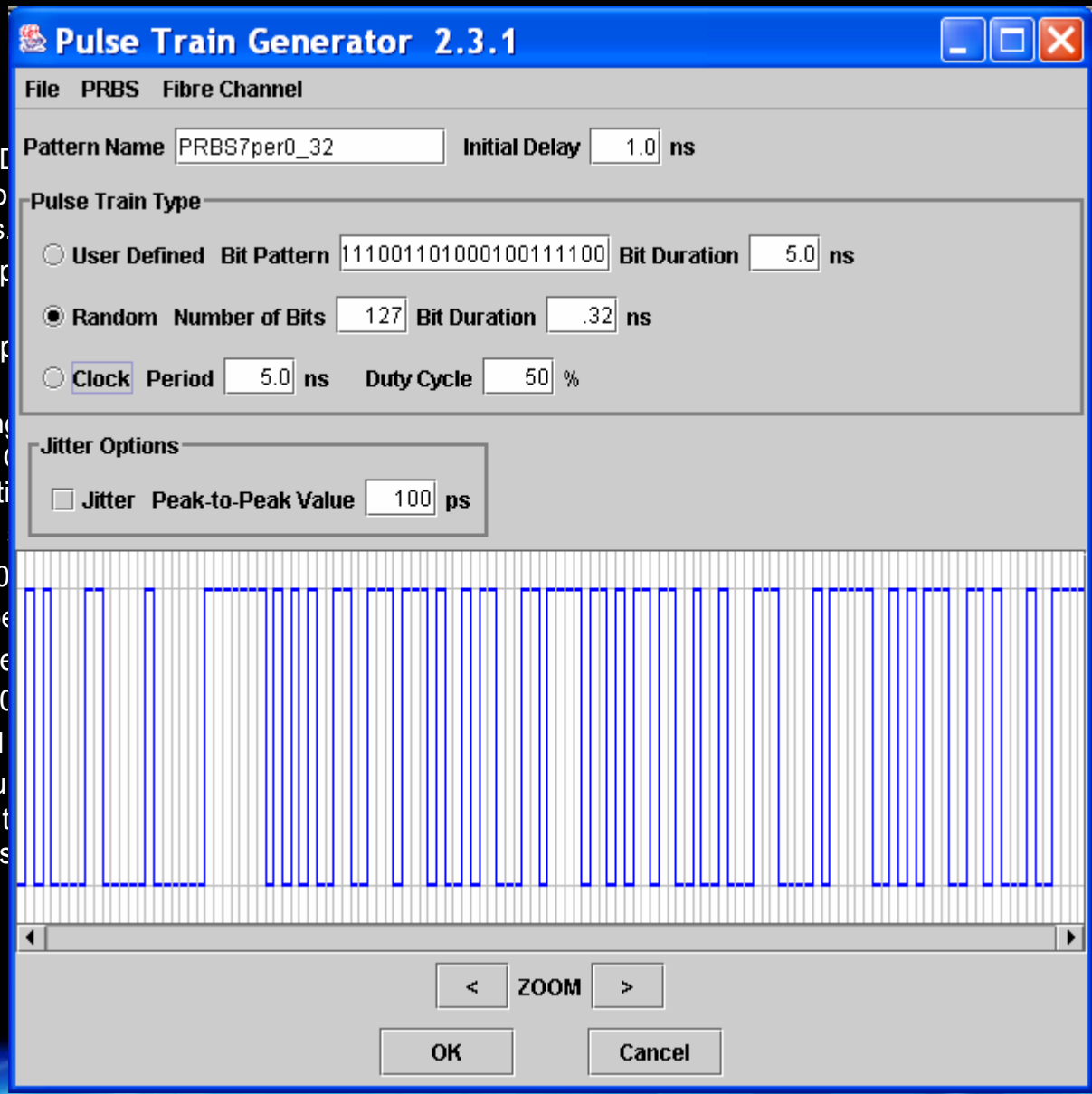
SI Analysis Results

Eye Masks

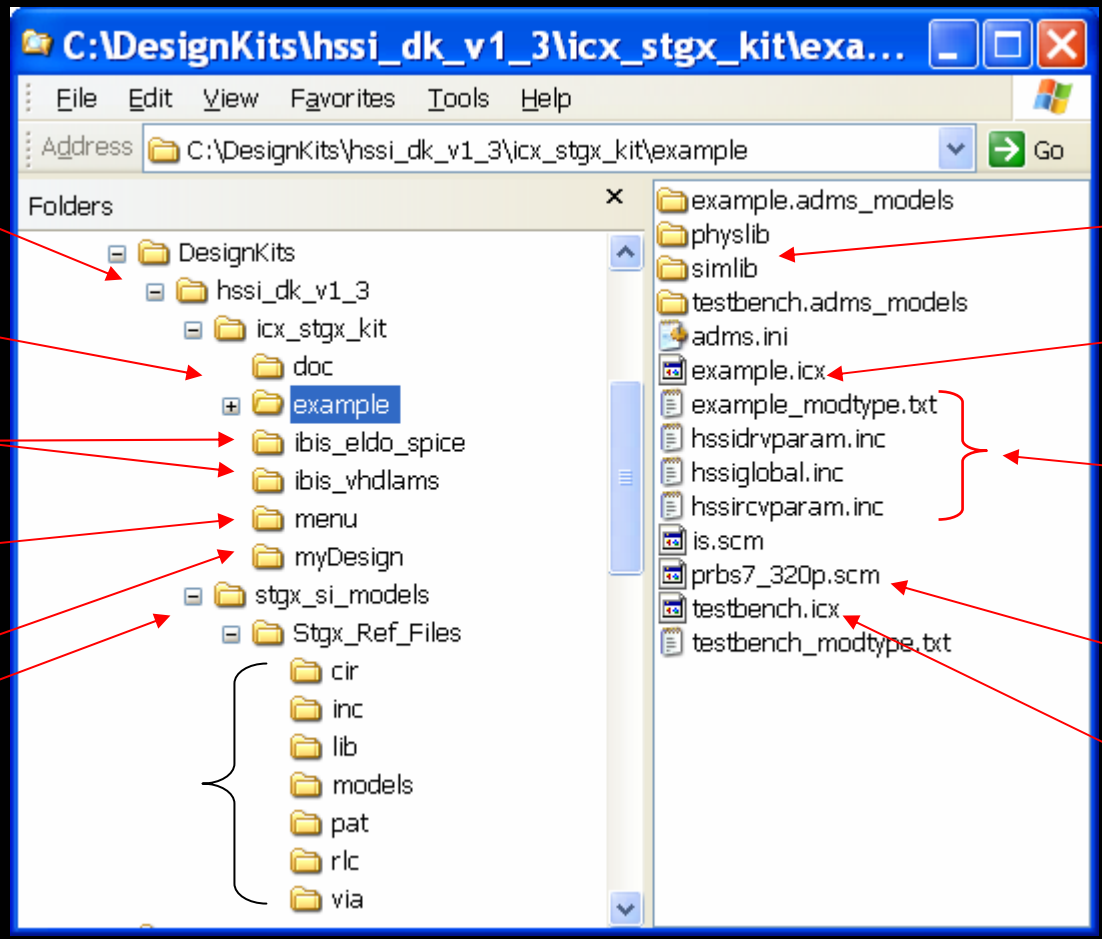
Kit Items

- **Routing Rules**
  - All signals within a given "QD
    FPGA's (U110 and U148) to
    deviation is +/- 0.050 inches.
  - Keep the distance from the p
    less than 750 mils.
  - Keep the distance from the p





Tour de Kit



HSSI Kit

Examples and doc

IBIS 4.1 wrappers

Custom menu

User Design Area

Models

Footprints

Symbols

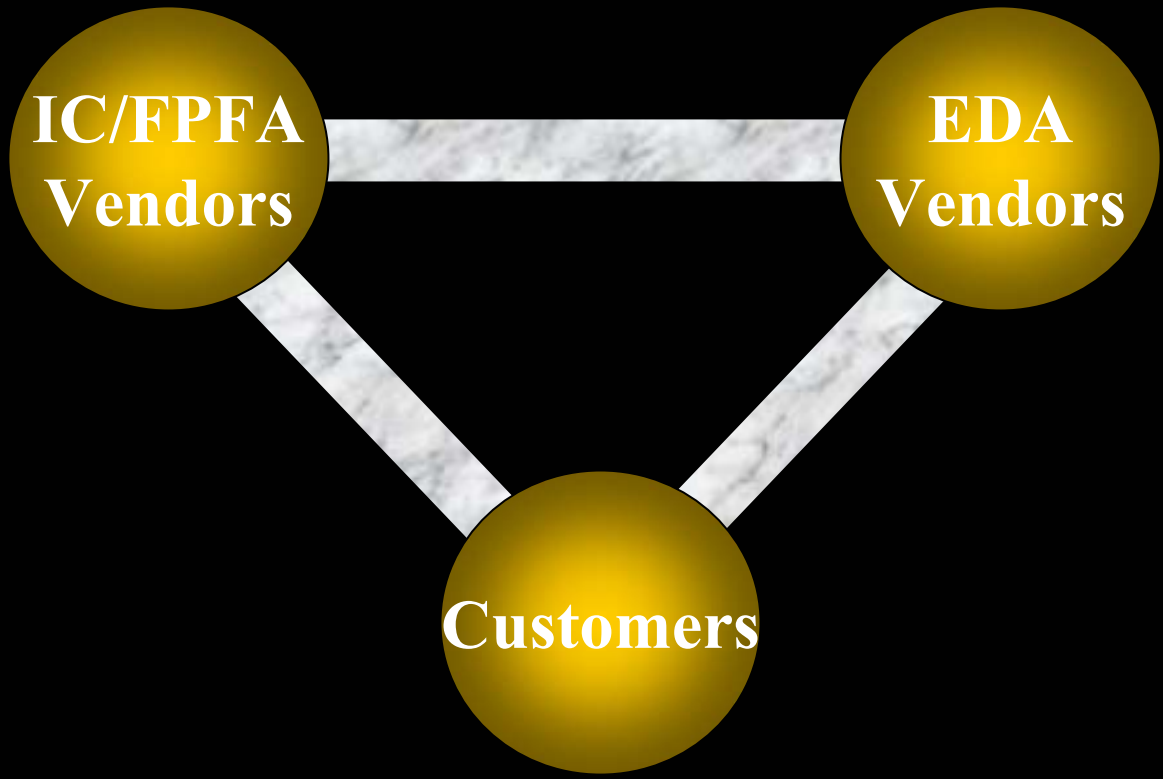
Complex Example

Files to control the HSSI Config

Custom Stimulus

Simple Example

Design Kits Development



Design Kits – Benefits to Customers

- Be up and running faster
- Have access to more than just Models, maximize efficiency and productivity
- Saves significant time
- Saves valuable resources
- Saves cost

Design Kits – Benefits to IC/FPGA Vendors

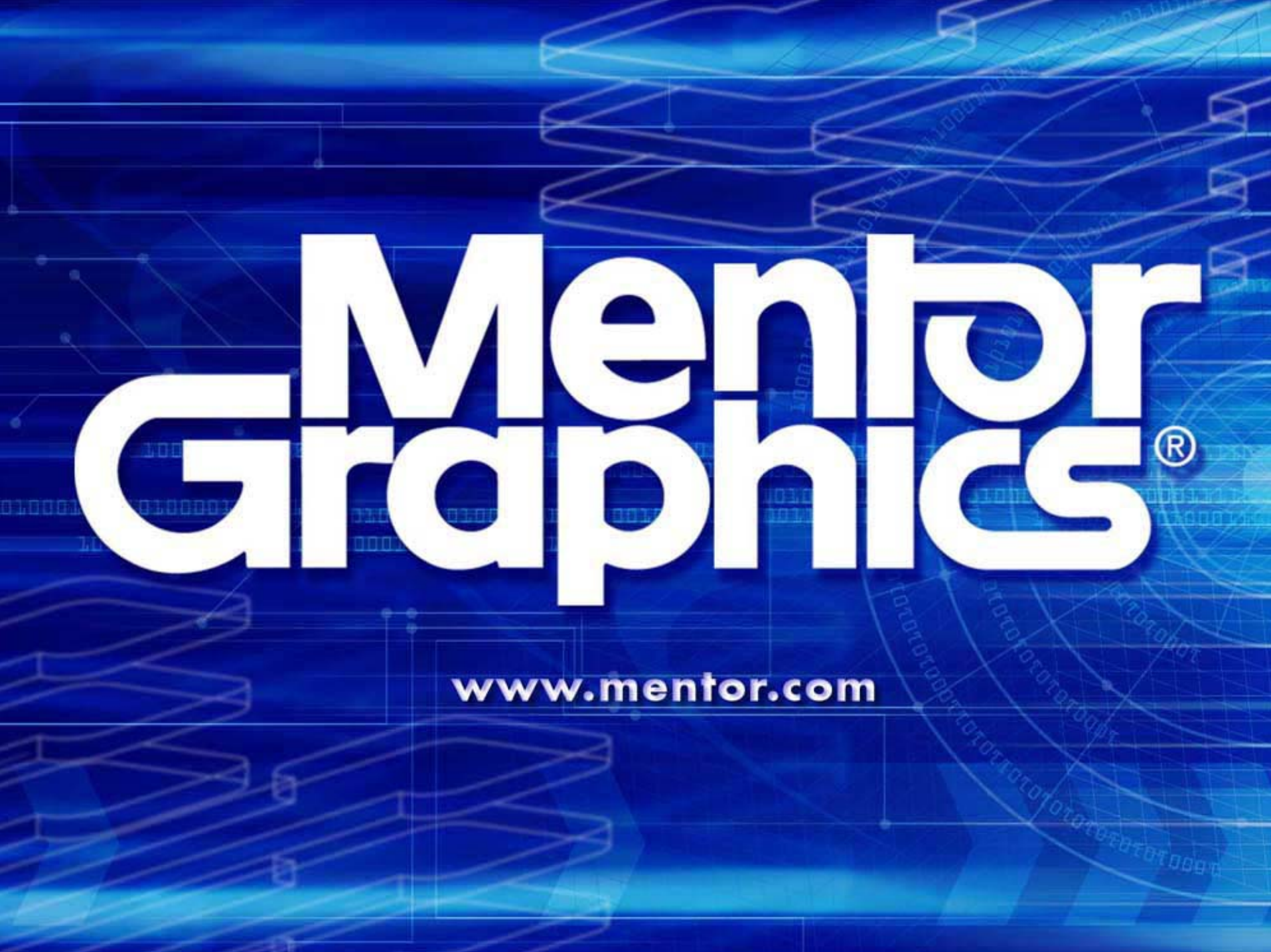
- Facilitates adoption of vendor silicon
- Better service to their customers

Design Kits – Benefits to EDA vendors

- Facilitates adoption of tools
- Maximize tool usage
- Better service to their customers

IBIS Committee/Forum

- Should maybe be another place to drive High Speed Design Kits requirements and make proposal for a common format/content?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