Considerations on Switching Characteristics

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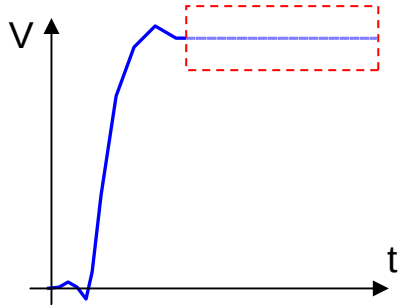
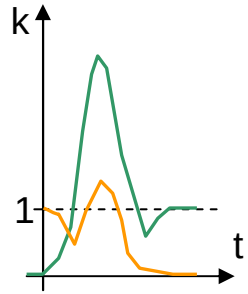
General Considerations

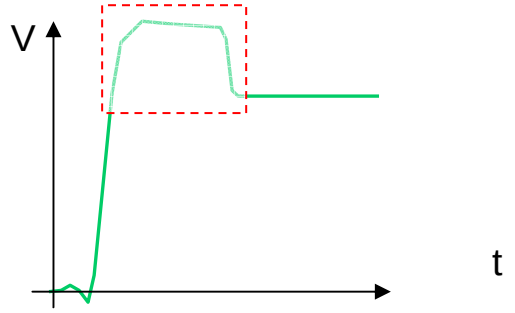
- Inadequate waveforms with data trailing the transition.



- Over-clocking especially in case of strong non-monotonic switching characteristics (SC).



- SCs including special buffer behaviour.

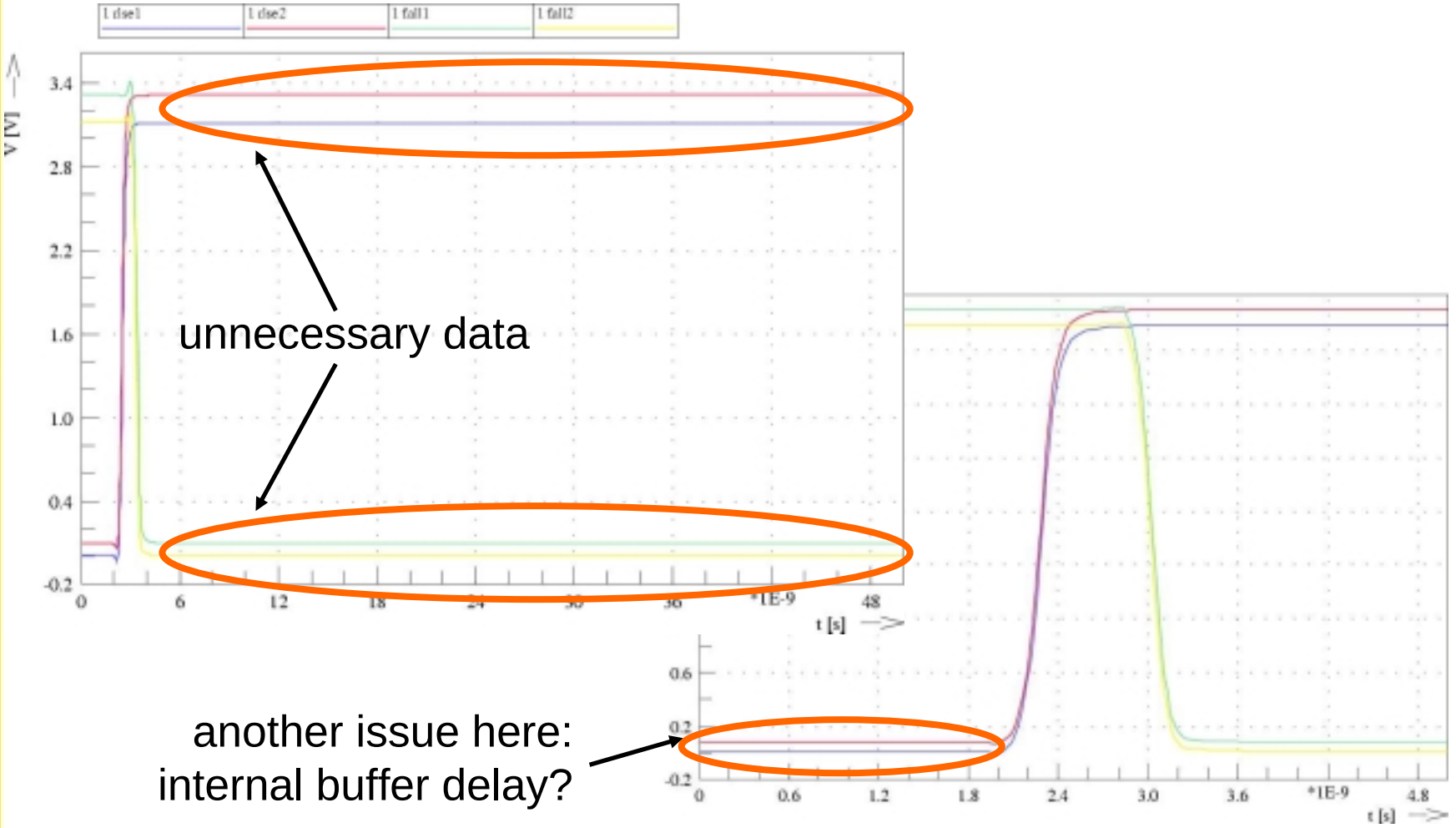


Transition Trailing Data

- Switching is not finished as long as SC data is still valid in time, although a steady state has been reached already.
- Depending on the quality of trailing data simulation results might be effected.
- Potential loss of accuracy due to waste of data points not used for transition description.

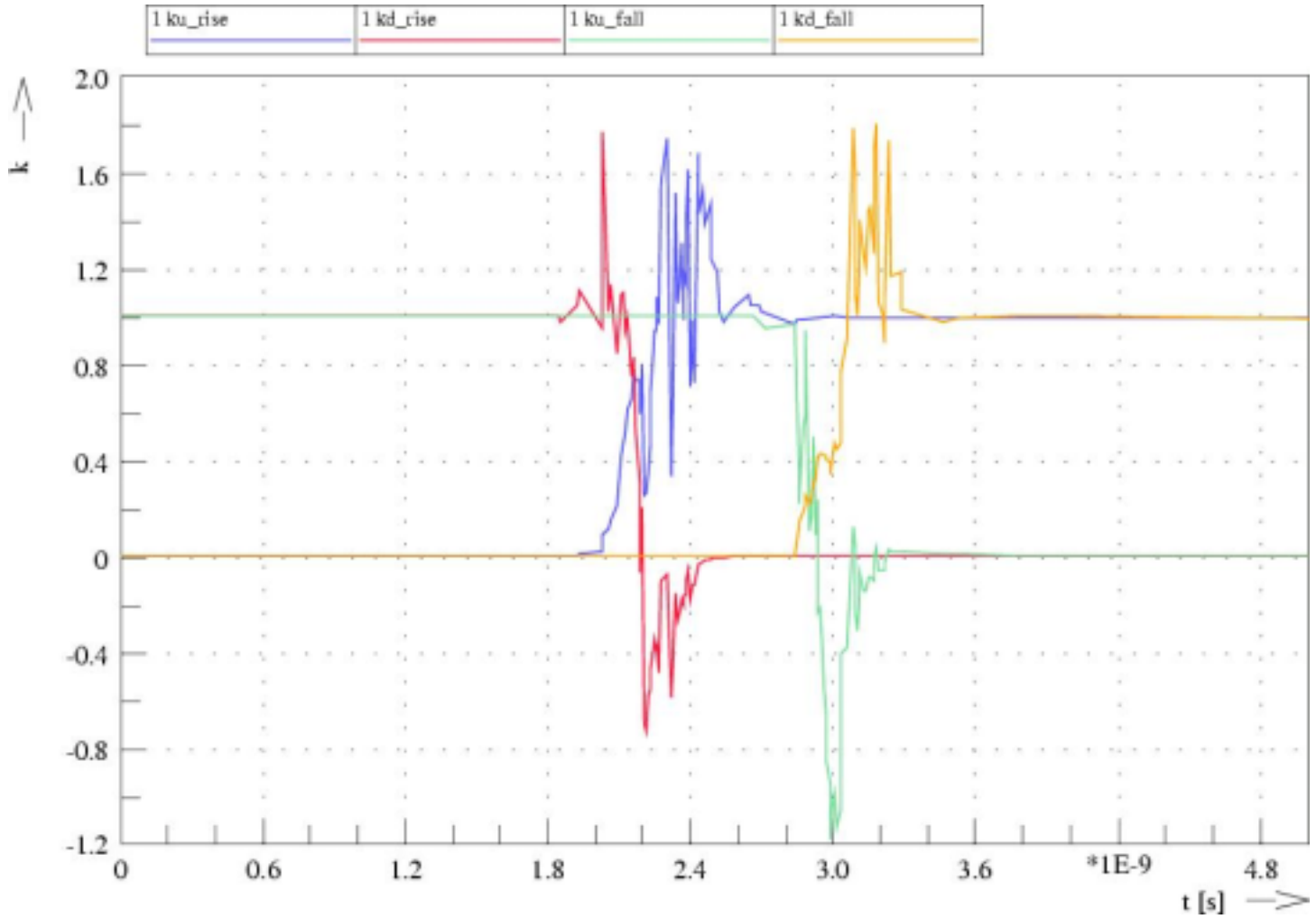
Transition Trailing Data

Rising/Falling Waveforms ALVC164245_BIO_33



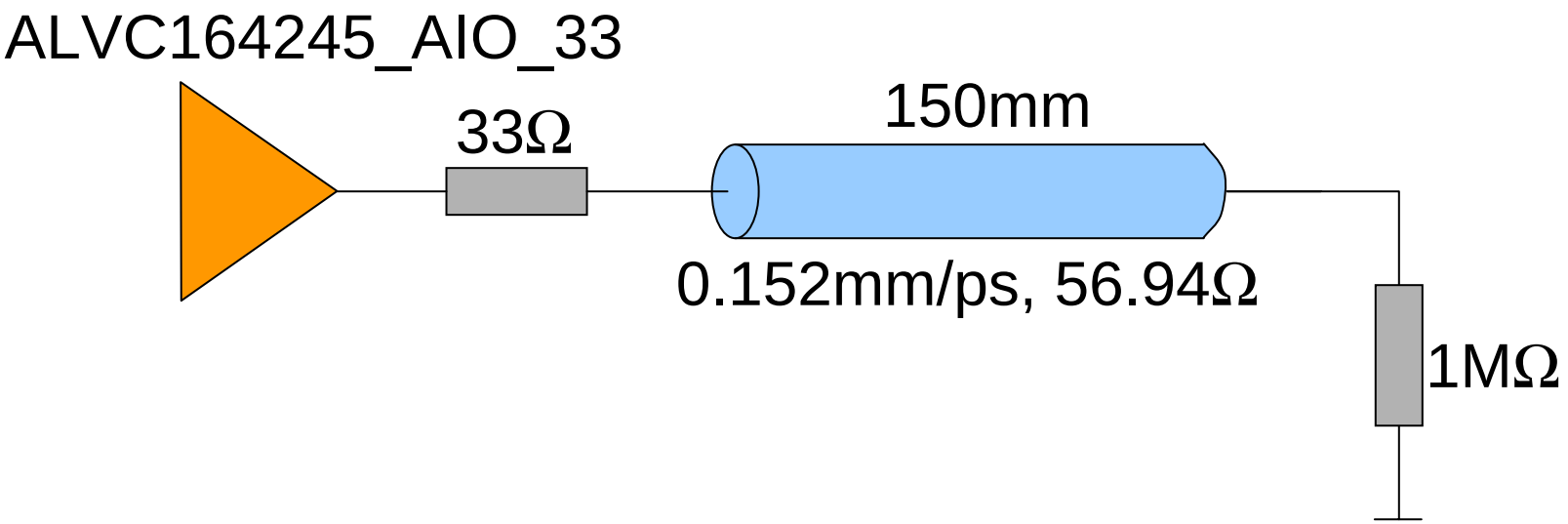
Transition Trailing Data

Switching Characteristics ALVC164245_AIO_33 (mod.)



Transition Trailing Data

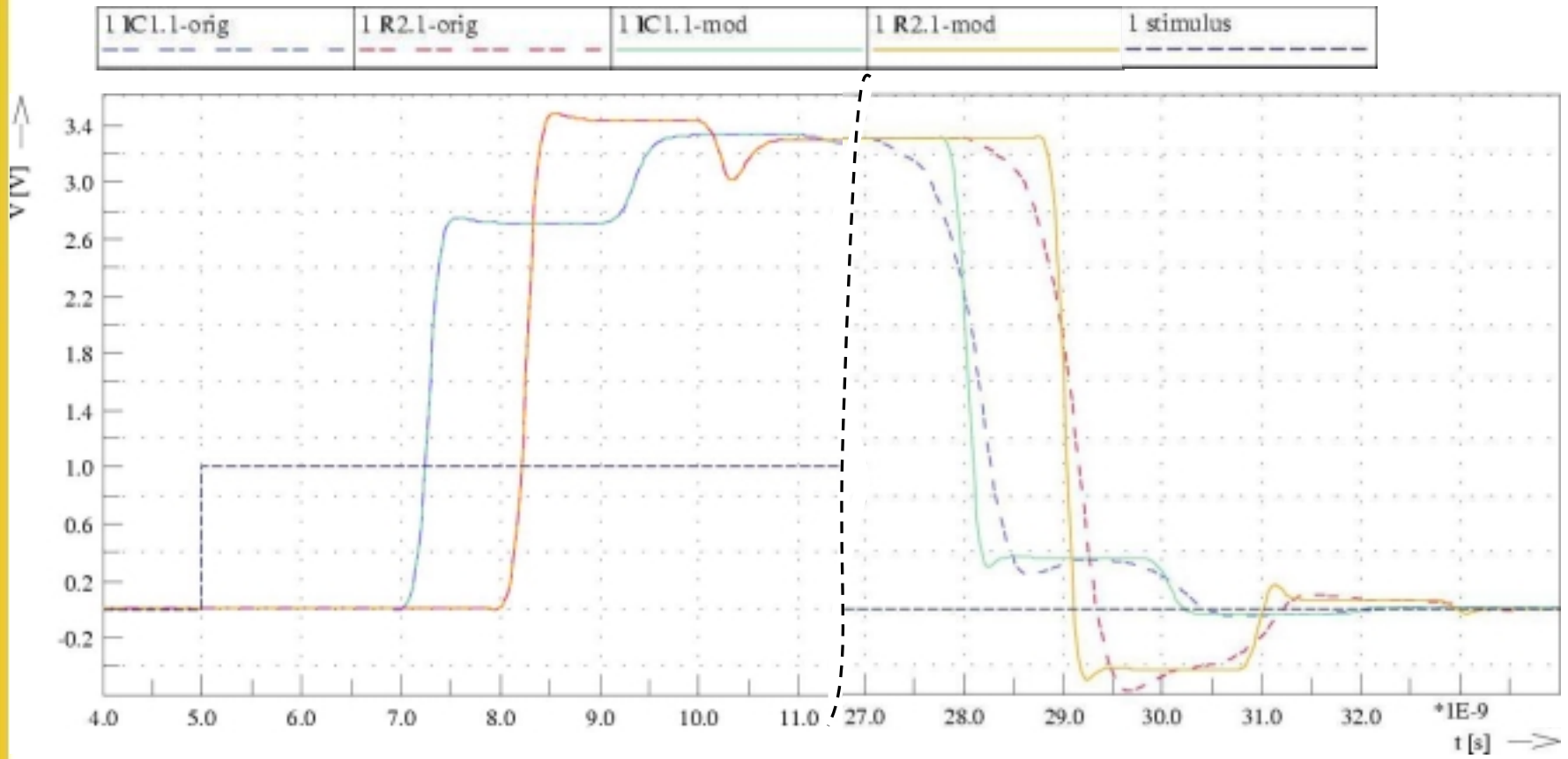
Simulation Scenario



Transition Trailing Data

HSPICE Simulation Results: original vs. modified model

No effect on 1st rising edge, but strong effect on falling edge!

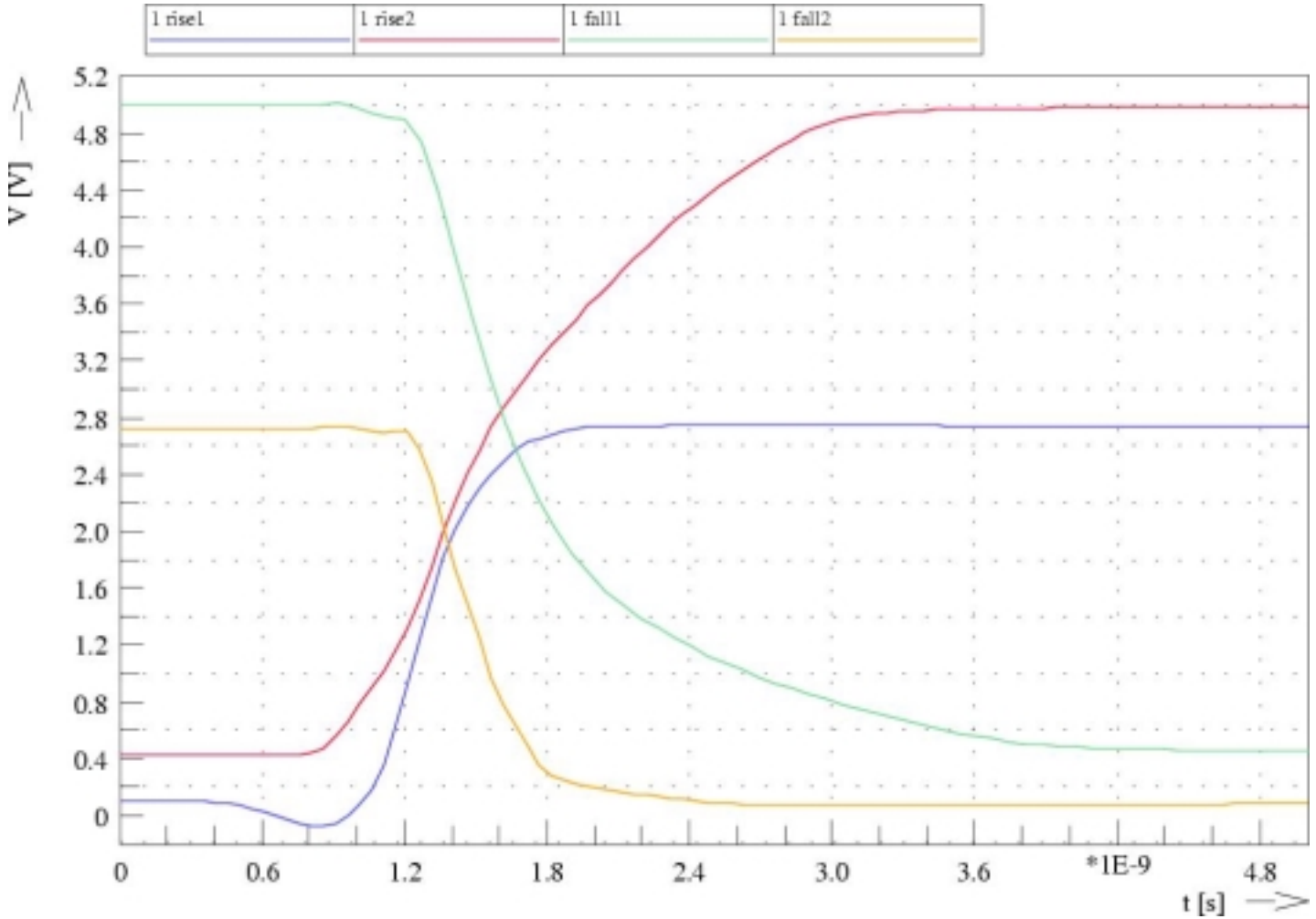


Over-clocking

- Transition has not been finished.
- Even more, transition changes before a steady state is reached.
- Likely to get an artificial buffer output impedance glitch.

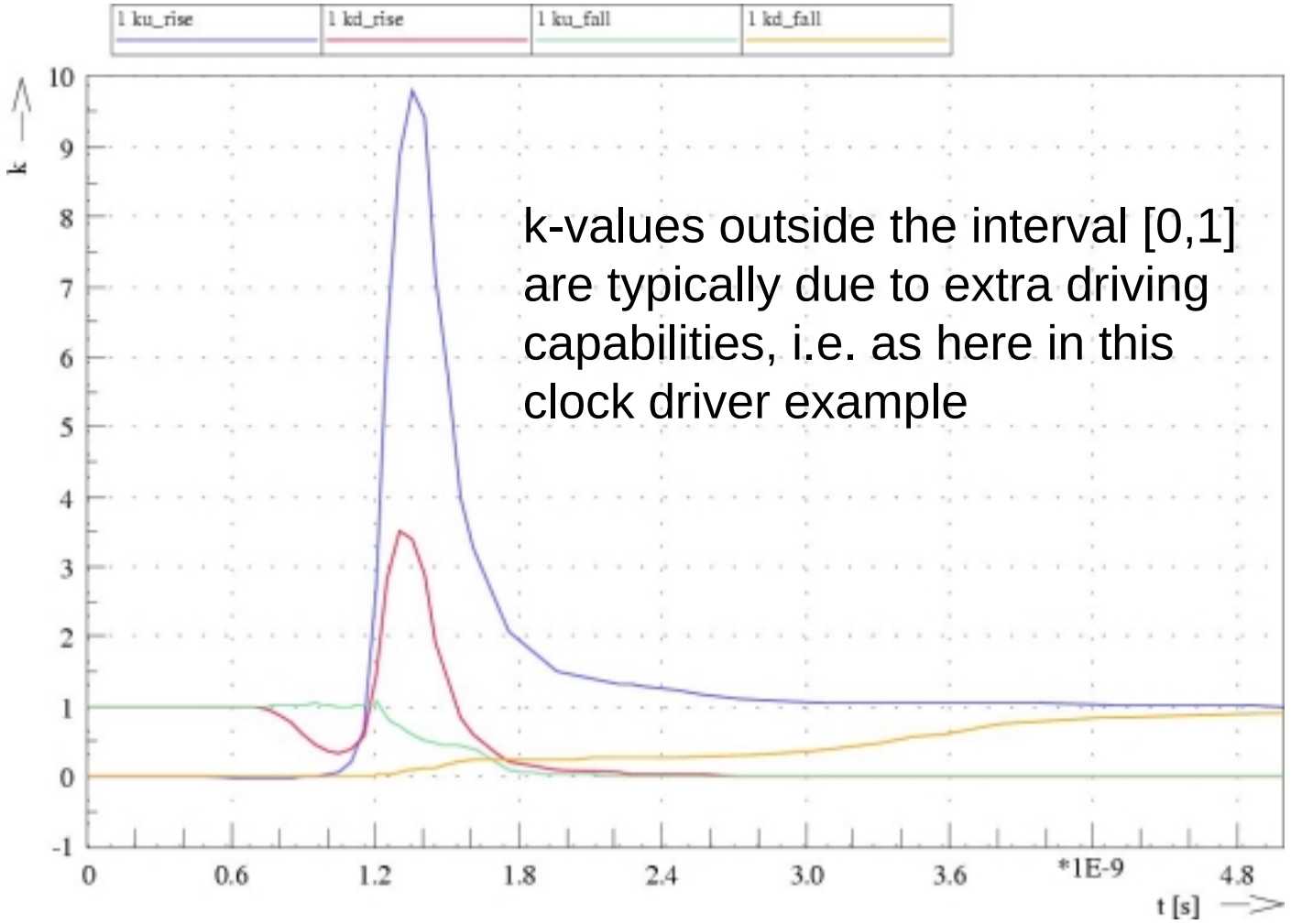
Over-clocking

Rising/Falling Waveforms CDC328A Driver



Over-clocking

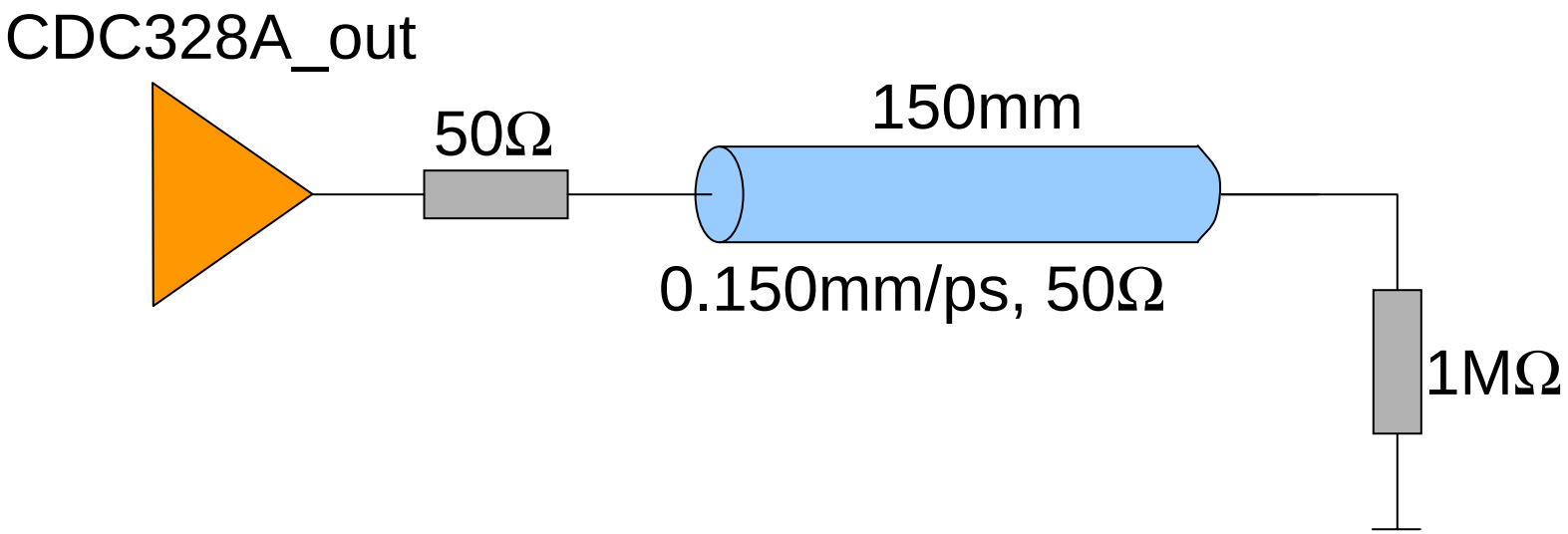
Switching Characteristics CDC328A Driver



k-values outside the interval [0,1] are typically due to extra driving capabilities, i.e. as here in this clock driver example

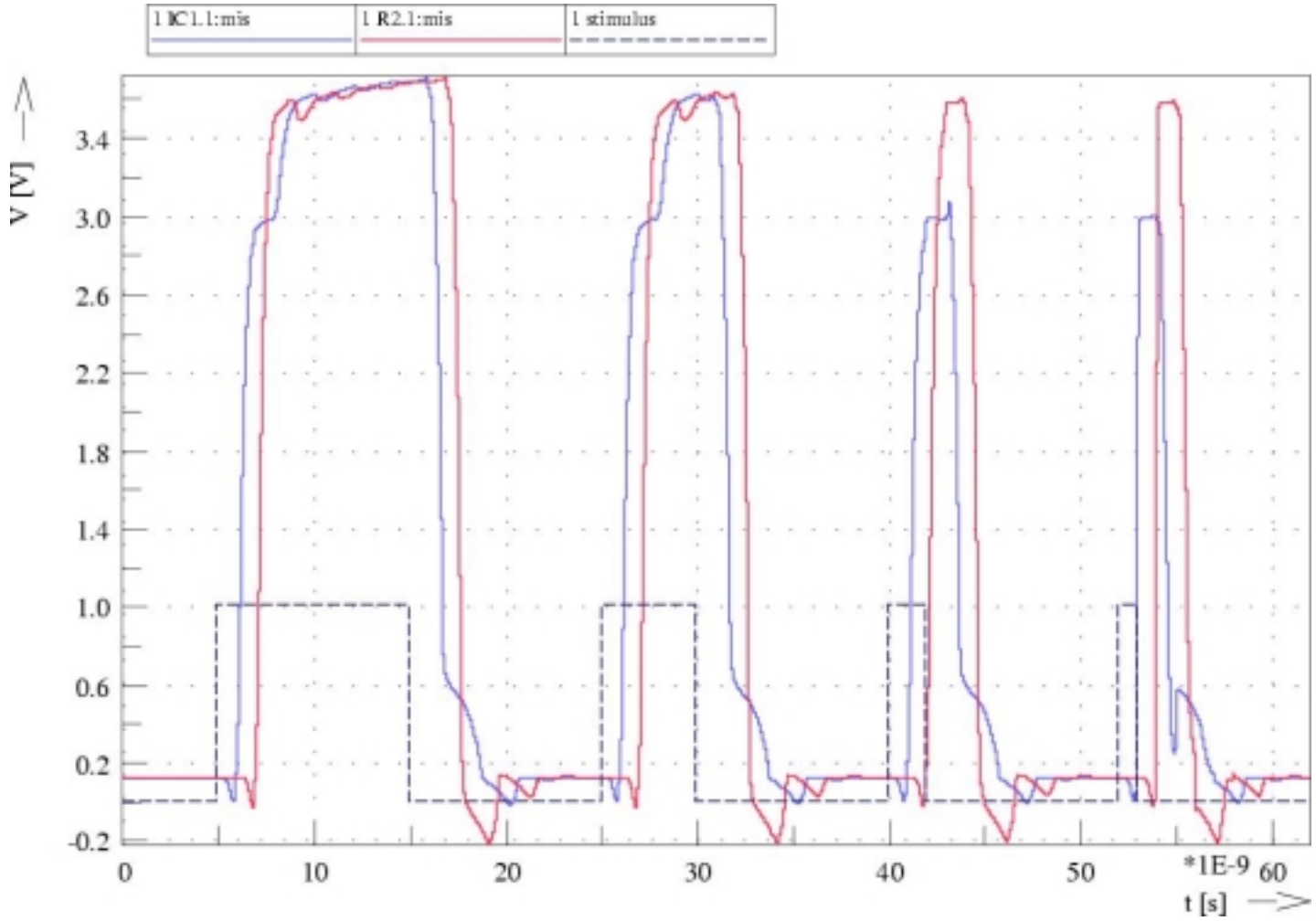
Over-clocking

Simulation Scenario



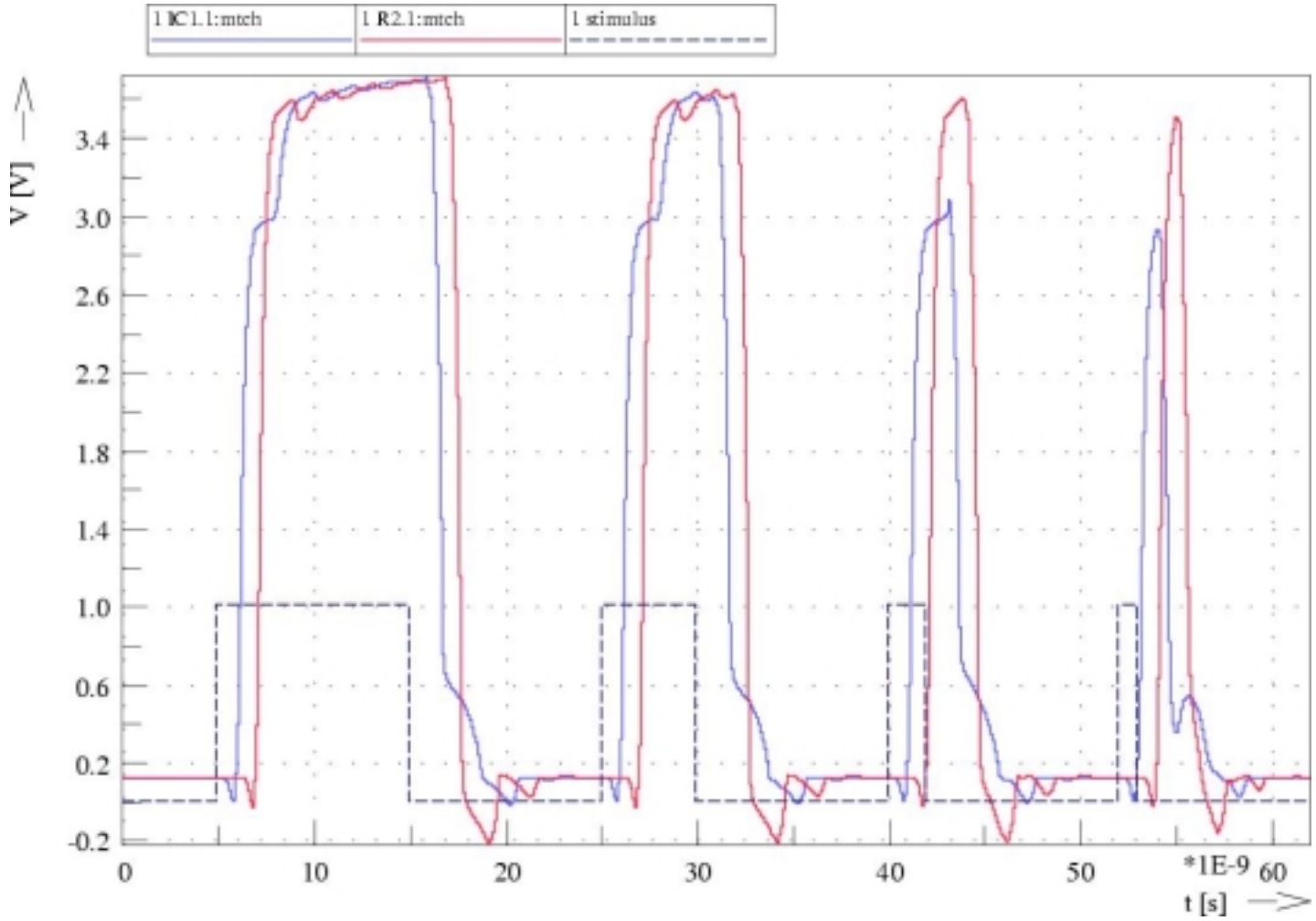
Over-clocking

Zuken Simulation: discontinuous output impedance



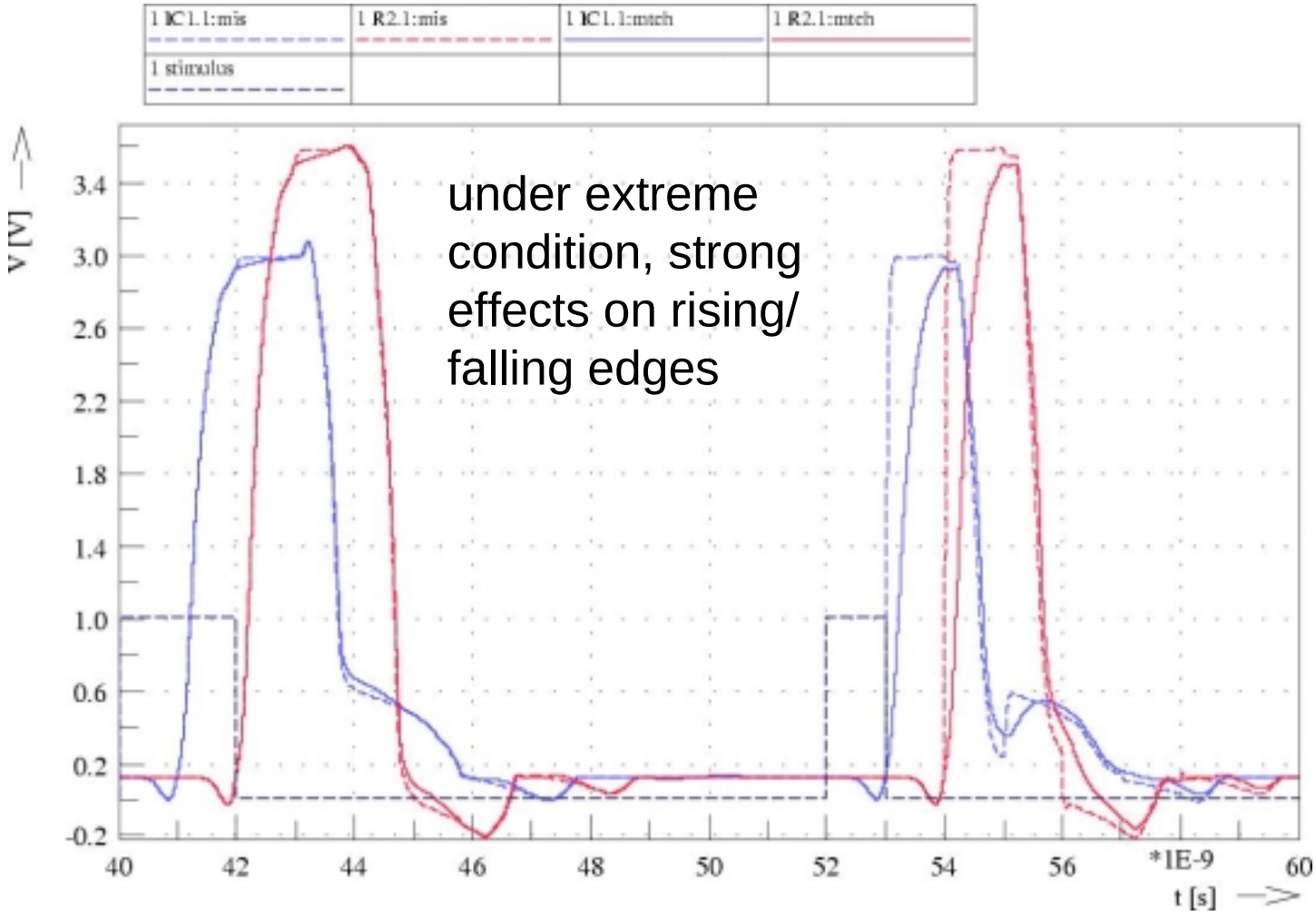
Over-clocking

Improved Zuken Simulation: continuous output impedance



Over-clocking

Simulation Results: discontinuous vs. continuous



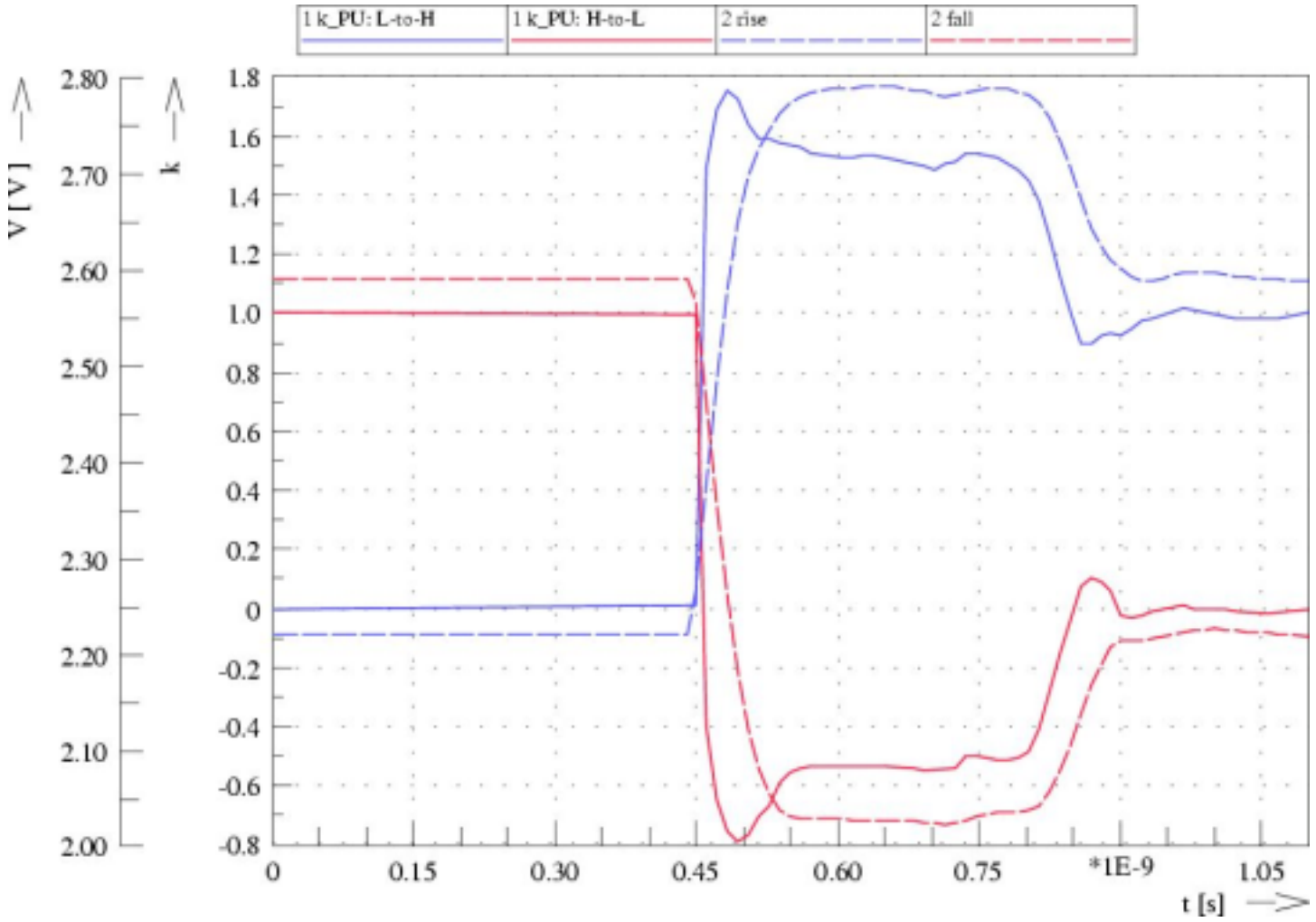
Special Buffer Behaviour

Customer Case SerDes Device:

- High speed serial I/O, data rate 1.25Gbps.
- Differential ECL driver.
- Rise/Fall times of about 70ps.
- Including programmable pre-/de-emphasis (none, nominal, maximum)
- Modelled as single stage IBIS buffer!

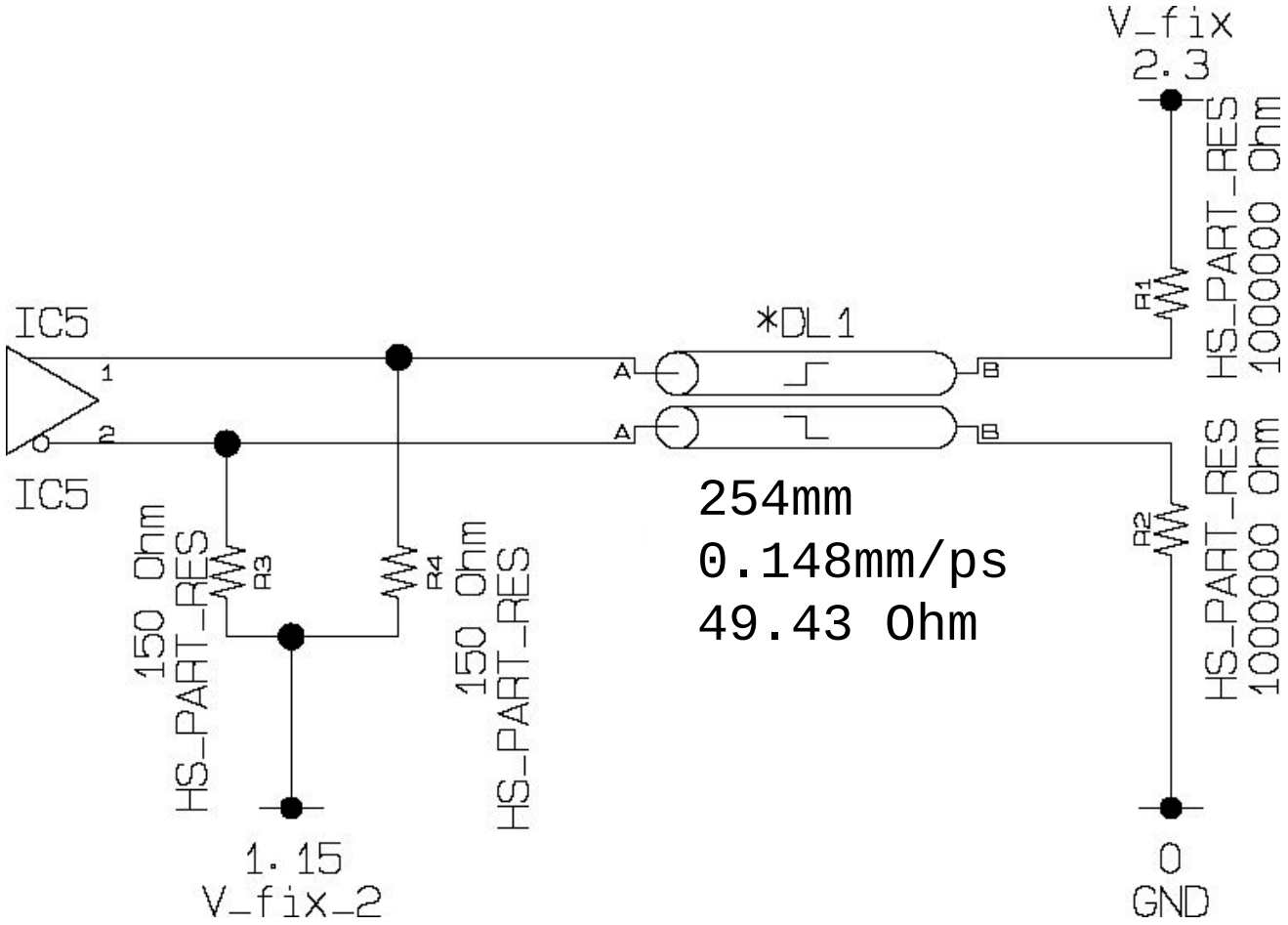
Special Buffer Behaviour

Waveforms and Switching Characteristics (nom. emph.)



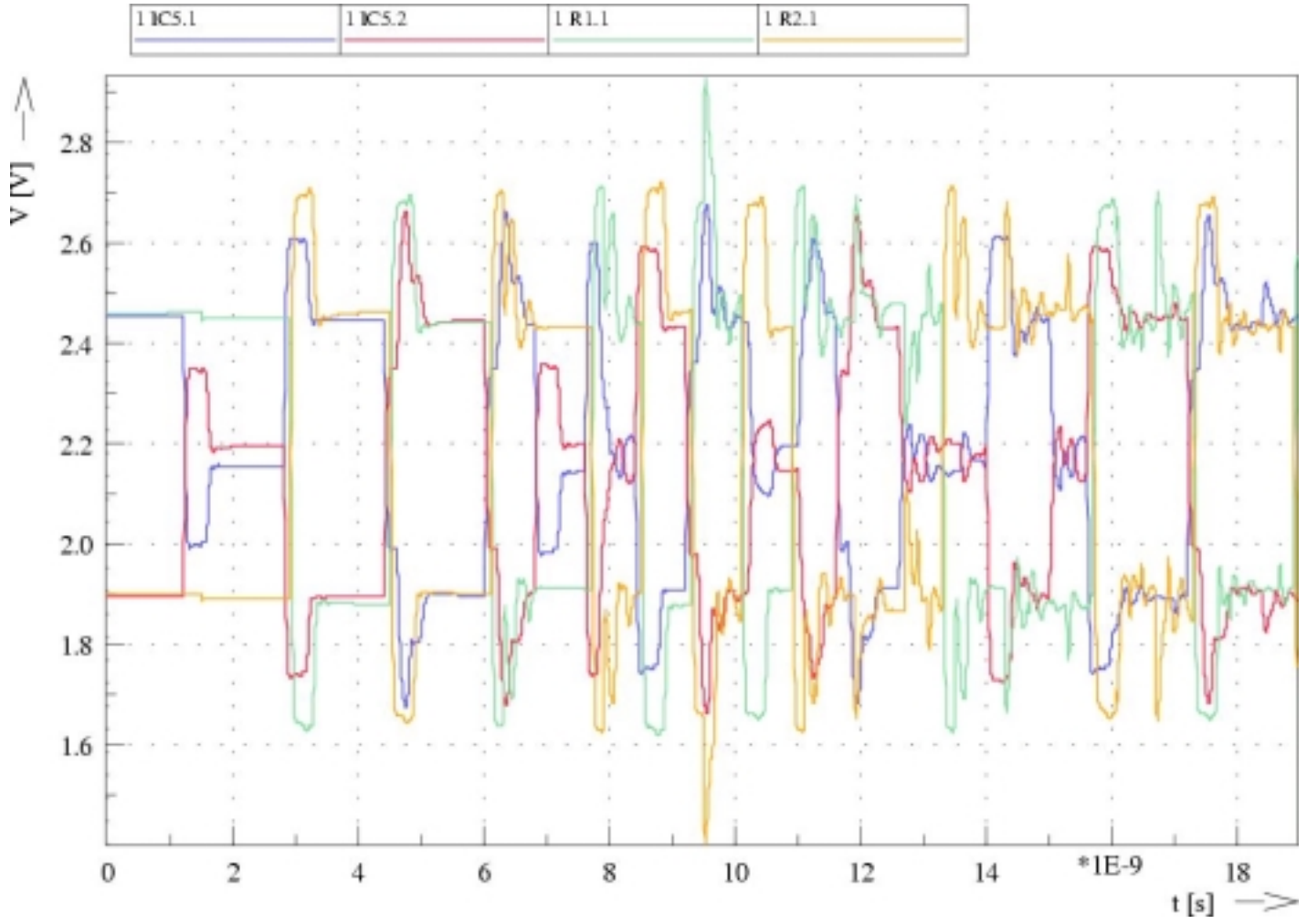
Special Buffer Behaviour

Simulation Scenario



Special Buffer Behaviour

Zuken Simulation Results with nom. emphasis model
625MHz, Pattern 01100110101000111001100 0



Special Buffer Behaviour

- Here, both issues shown before become valid:
  - Trailing transition data includes pre-/de-emphasis information.
  - An over-clocking like effect occurs at maximum data rate.

Special Buffer Behaviour

- Although this is a formally correct IBIS model, is this a valid modelling approach?
- Can pre-/de-emphasis modelled this way at all?

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