Computer-Assisted Modeling of Digital I/O Buffers for IBIS

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Discussion within CPMT – TC12

Electrical Design, Modeling and Simulation (EDMS, TC-12) sub-commitee

http://www.ewh.ieee.org/soc/cpmt/tc12/

- **EDMS sub-committee works on the standardization of design tools and design methodologies in packaging**
- **Initiative for "Practical Macromodels for Digital I/O"**

  → First meeting @ EPEP, Oct. 2004 in Portland, Oregon, USA.
  http://www.ewh.ieee.org/soc/cpmt/tc12/standardization_files/IBIS_TC12a.ppt

SPI (Signal Propagation on Interconnets) IEEE Workshop,
May. 10-13, 2005 in Garmisch-Partenkirchen, Germany
(c.f.p. at http://www.spi.uni-hannover.de/)

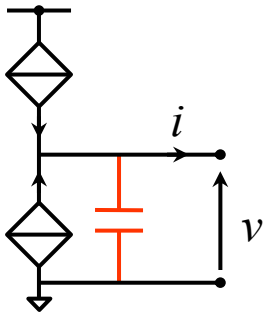
I/O Buffers Macromodeling

- **Required Goals:**
  - **IP protection**
  - **Vendor-independent** format
  - Have to capture TX, RX, and package parasitic essentials
  - Sufficiently accurate to be useful
  - **Easy to automatically generate** from Spice and Measurements
  - Easy to verify
  - Easy and fast to simulate

I/O Buffers Macromodeling
Current status

Circuit-based modeling

(native IBIS)



- standard,
- large data/model libraries,
- EDA tools support...

specification and tools from
http://www.eigroup.org/ibis/

Black-box modeling

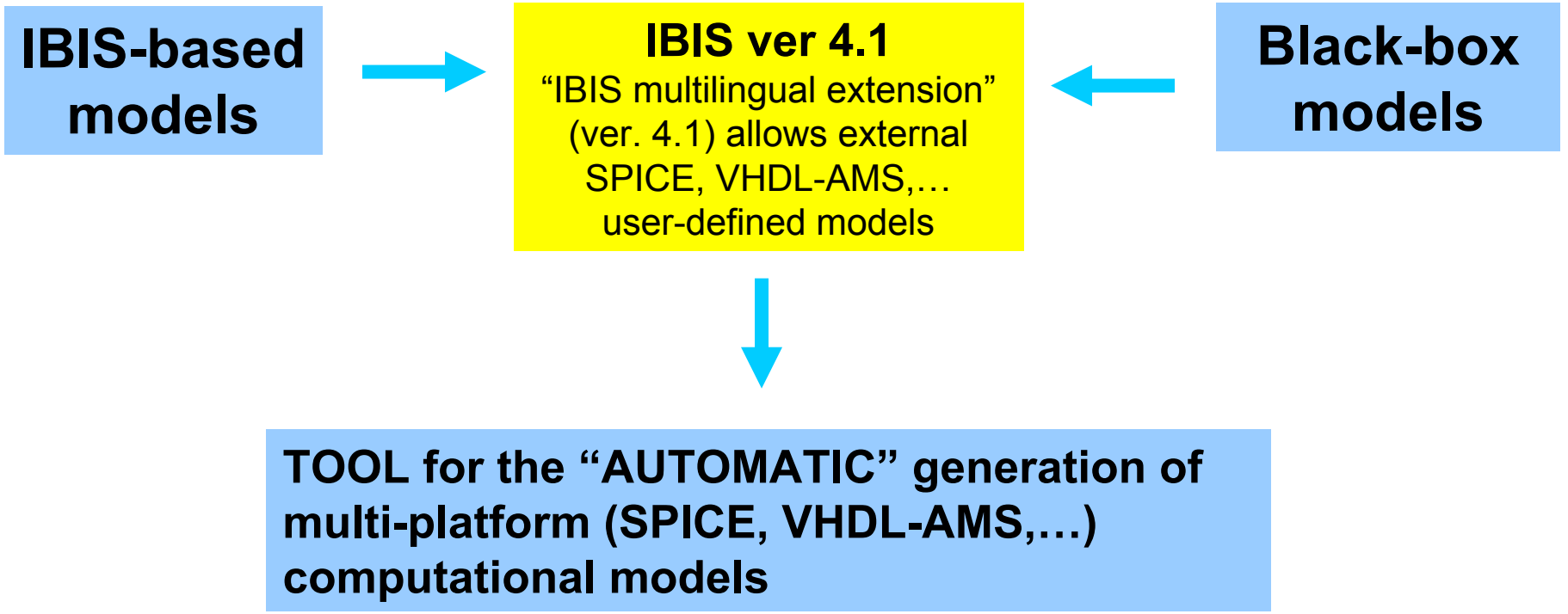
$$i = \mathrm{F}(v, d/dt)$$

…aimed at improving the modeling of latest technologies and high-order effects

- LVDS drivers with pre-emphasis
- DDR memories,
- power supply ports…

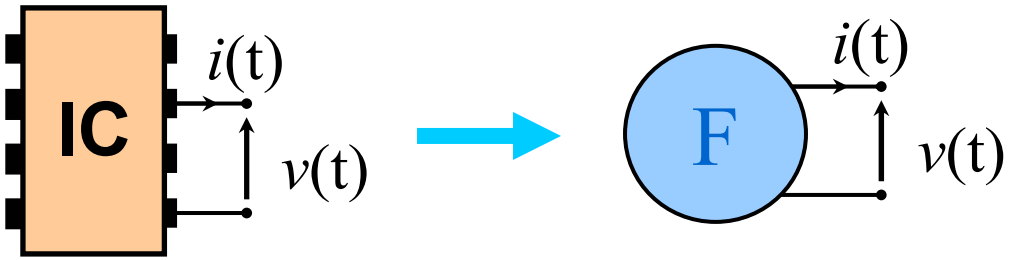
e.g., parametric modeling

I/O Buffers Macromodeling
The way forward



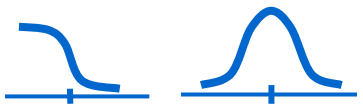
Black-box modeling @ Politecnico di Torino

Mπ*log*© (Macromodeling via parametric identification (π) of logic gates): **Method & Tool**



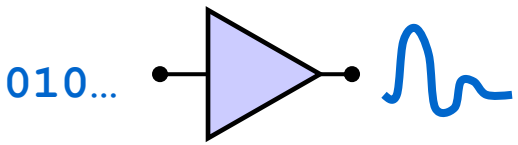
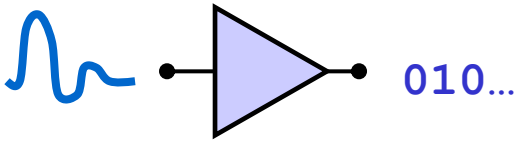
$$i(k) = F(\Theta,[i(k-1)\ldots, i(k-r),v(k),\ldots, v(k-r)])$$

Σ nonlinear basis functions



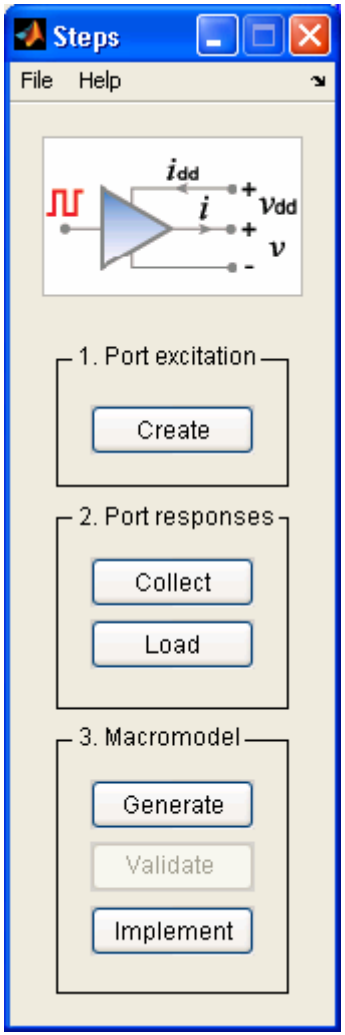
Model parameters (Θ) via system identification methods

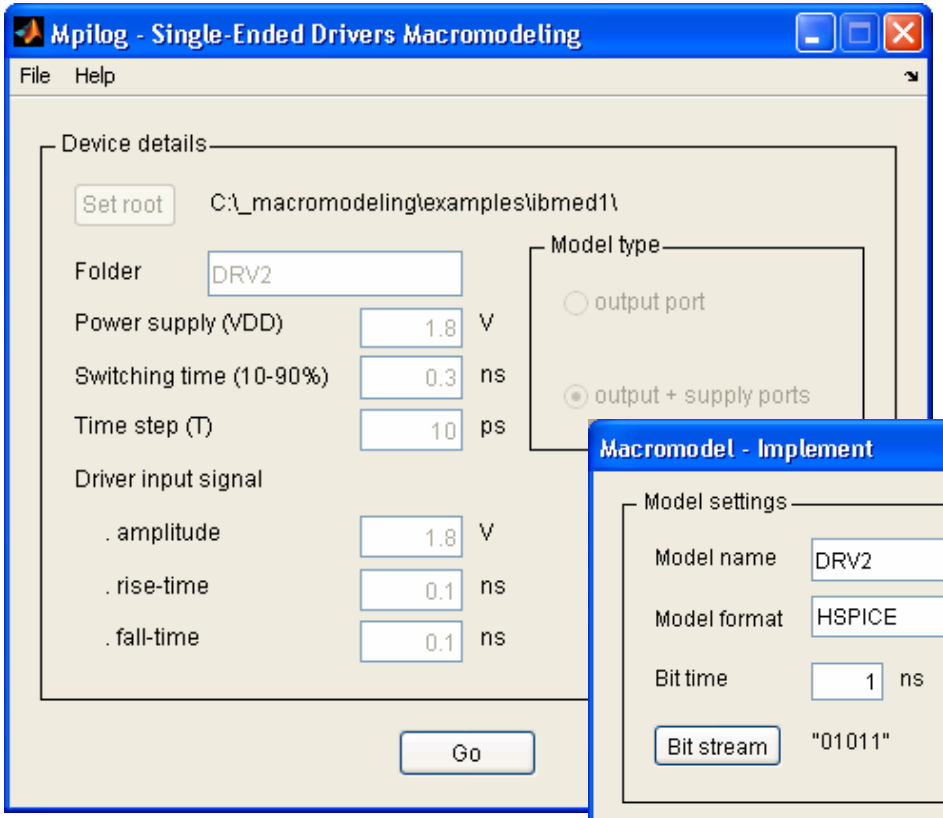
Mπlog features

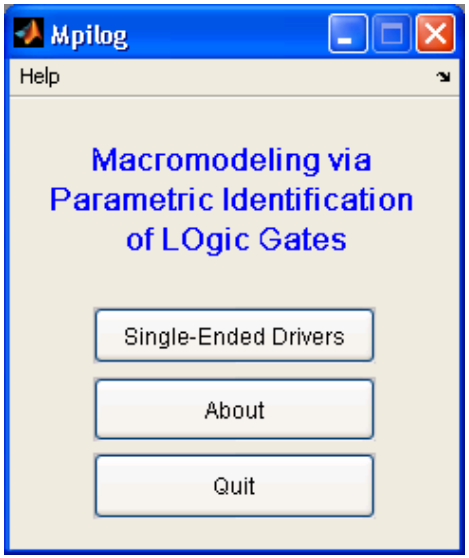
	Single-Ended	Differential
Drivers 	✓	✓
Receivers 	✓	✓

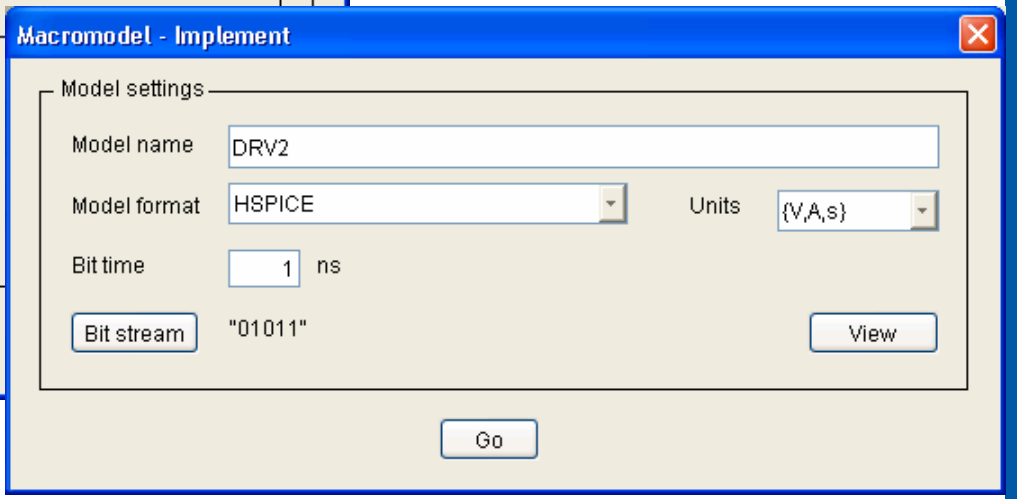
\+ { Power Supply ports
Temperature effects

Mπlog Tool



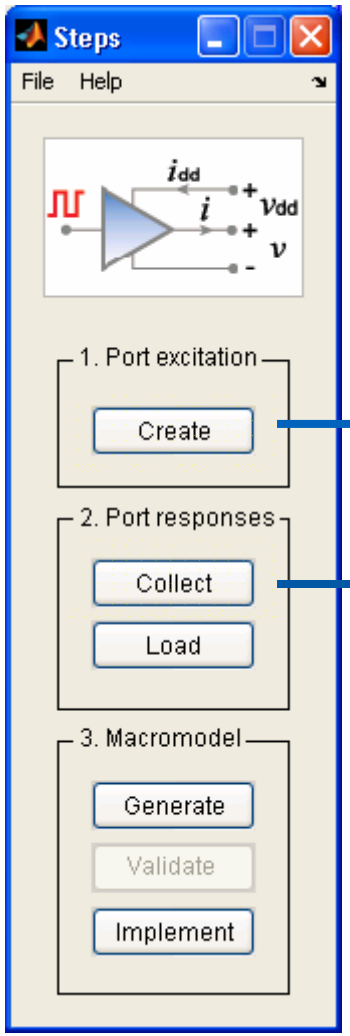


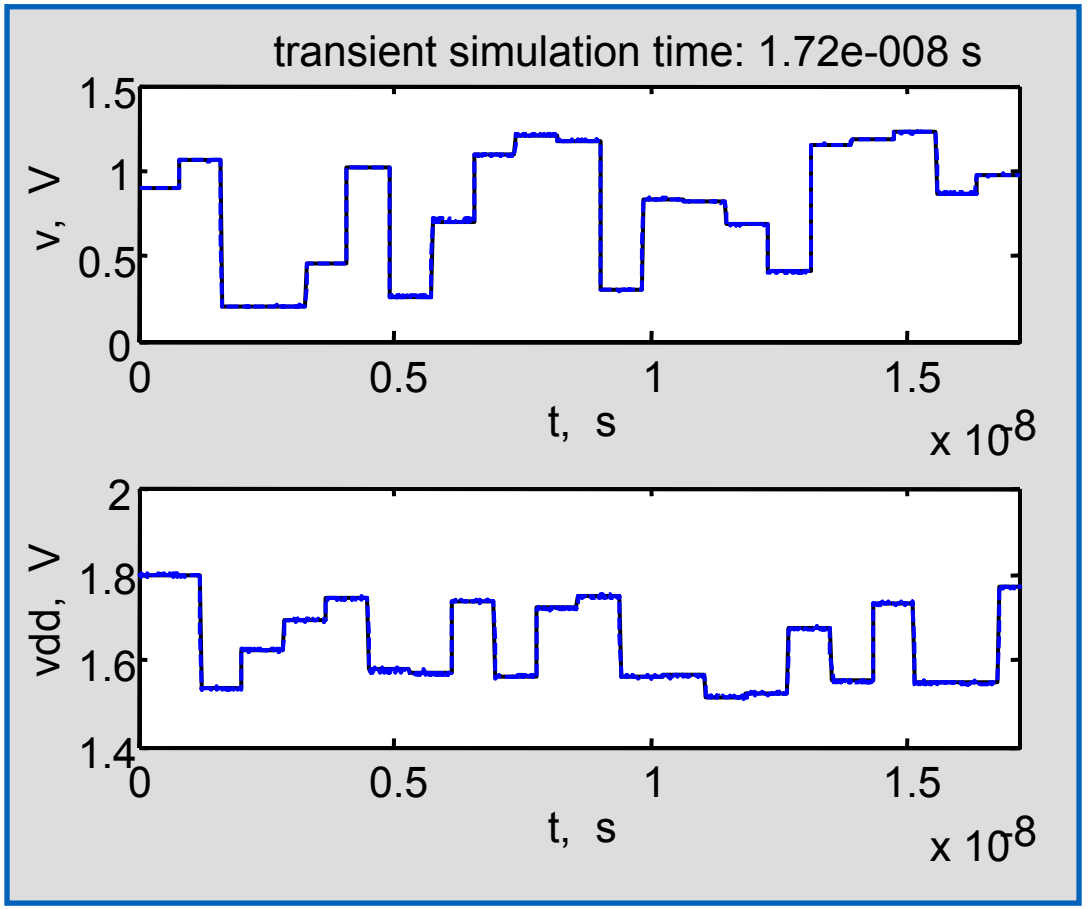




Tool available on request (igor.stievano@polito.it)

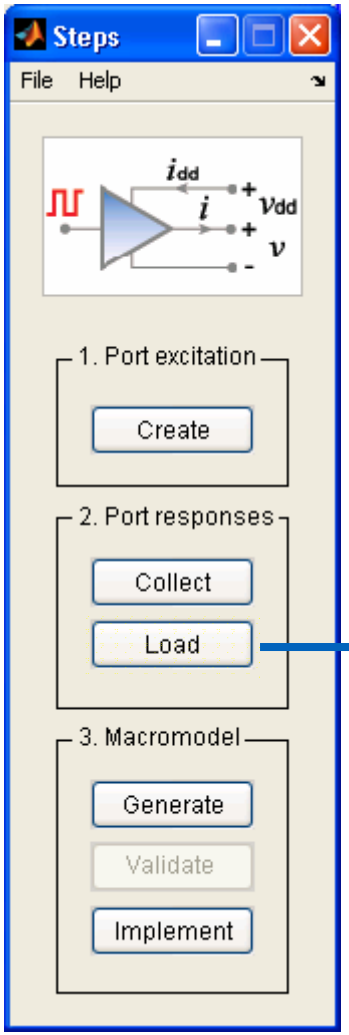
Mπlog Tool

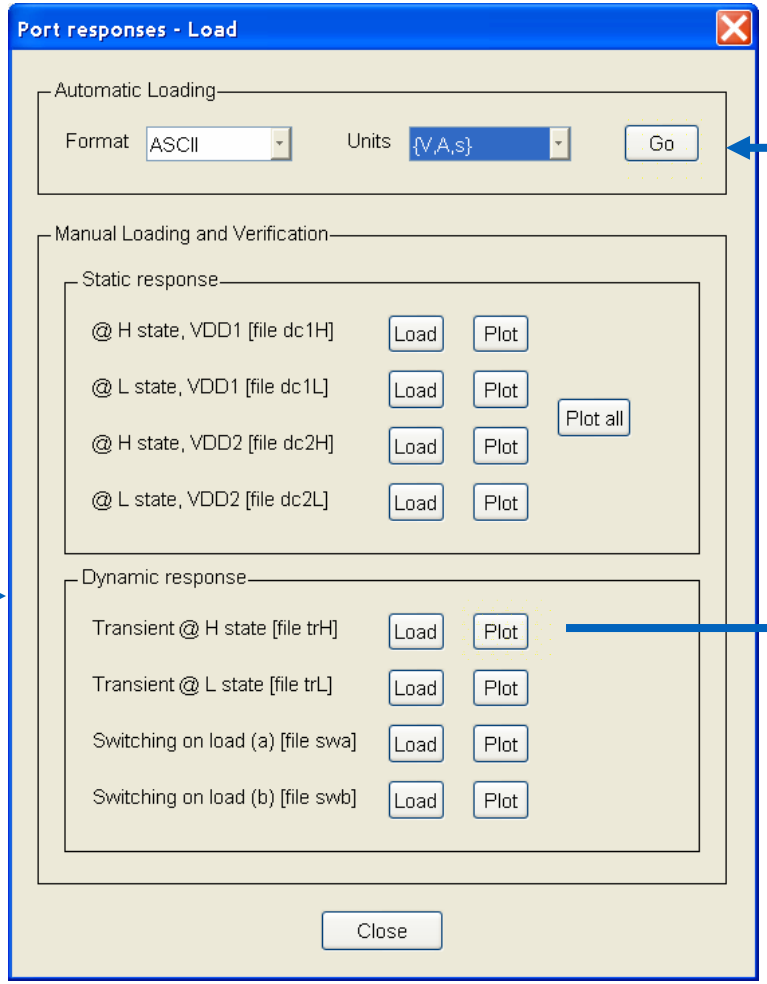




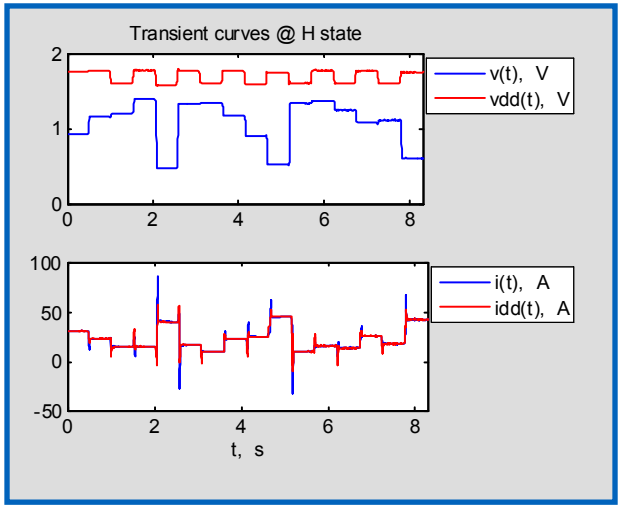
RUN YOUR PREFERRED CIRCUIT SOLVER (e.g. SPICE)

Mπlog Tool

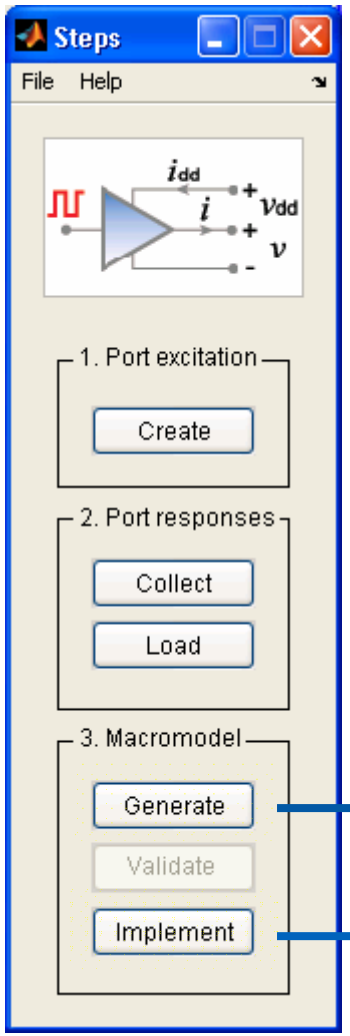


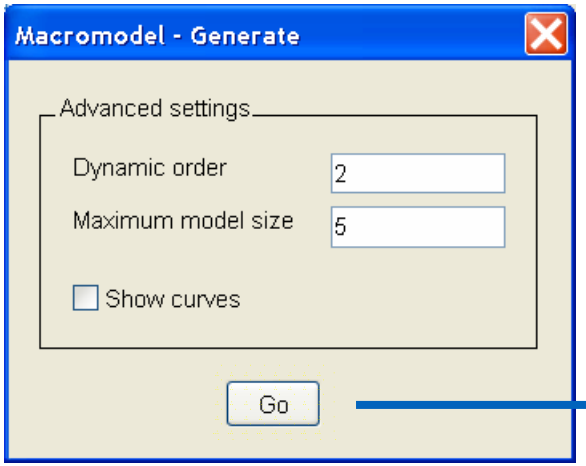


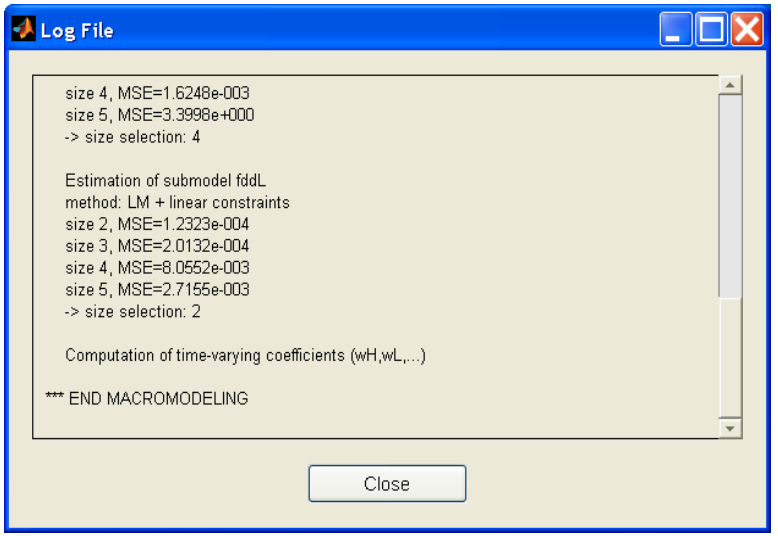
AUTO LOADING

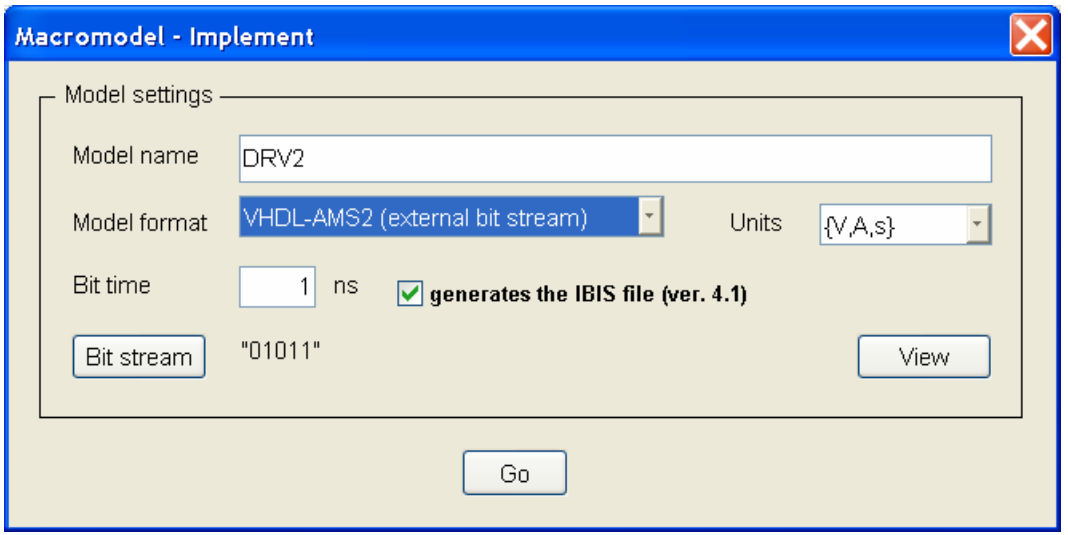


Mπlog Tool


Steps
File
Help
1. Port excitation
Create
2. Port responses
Collect
Load
3. Macromodel
Generate
Validate
Implement


Macromodel - Generate
Advanced settings
Dynamic order
2
Maximum model size
5
Show curves
Go


Log File
size 4, MSE=1.6248e-003
size 5, MSE=3.3998e+000
-> size selection: 4
Estimation of submodel fddL
method: LM + linear constraints
size 2, MSE=1.2323e-004
size 3, MSE=2.0132e-004
size 4, MSE=8.0552e-003
size 5, MSE=2.7155e-003
-> size selection: 2
Computation of time-varying coefficients (wH,wL,...)
*** END MACROMODELING
Close


Macromodel - Implement
Model settings
Model name
DRV2
Model format
VHDL-AMS2 (external bit stream)
Units
{V,A,s}
Bit time
1
ns
generates the IBIS file (ver. 4.1)
Bit stream
"01011"
View
Go

Conclusions (i)

- ☺☺ – **IP protection**
- ☺☺ – **Vendor-independent** format
- ☺☺ – Have to capture TX, RX, and package parasitic essentials
- ☺☺☺ – Sufficiently accurate to be useful
- ☺☺☺ – **Easy to automatically generate** from Spice and Measurements
- ☺☺ – Easy to verify
- ☺☺ – Easy and fast to simulate

Conclusions (ii)

Black-box models are expressed by equations that are used **as they are**, without any interpretation

- no data to model conversion needed
- flexible modeling methods
- model enhancements do not affect IBIS and IBIS simulator structures

The distribution of black-box models would be a valuable complement to the distribution of behavioral data

Acknowledgements

Thanks to

-  for providing the Analog/Mixed-Signal simulator environment (**ADVance MS™ + Eldo™**)
- **Sergio Perazza** (Mentor, Italy) for the technical support on Mentors' products
- **Arpad Muranyi** (Intel) for VHDL templates and code posted on http://www.eda.org/pub/ibis/summits/jun03a/ and http://www.eda.org/pub/ibis/summits/feb04a/