# Multi-Gigabit SerDes Simulation using IBISv4.1(VHDL-AMS) Modeling

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# Authors and Acknowledgements

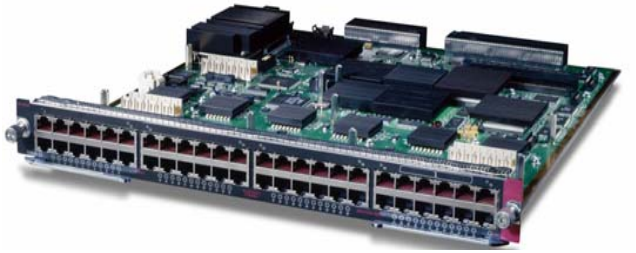


- **Philippe Sochoux – Post Layout simulations**
- **Luis Boluna – Lab Measurements**
- **Eddie Wu – HSPICE correlations, AMS modeling**
- **Jayanthi Natarajan – Pre Layout simulations**
- **Kim Owens – Mentor Graphics**
- **Matt Hogan – Mentor Graphics**

# Simulation Challenges



- 26 layer linecard design
- 100’s of multi-gigabit SerDes interfaces
- 8000+ highly constrainted nets
- SerDes applications for XAUI, CEI-6G, CEI-11G



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# History



- **Originally started by Intel. Presently driven by the IBIS open forum consisting of EDA vendors, Computer Manufacturers, Semiconductor vendors and Universities.**
- **IBIS versions:**

**V1.0 - Original First release April 1993**

**V1.1 - Released June 1993 at DAC, Dallas.**

**V2.0 - Ratified June 1994 at DAC, San Diego**

**V2.1 - Released Dec 1994**

**ANSI/EIA-656 approved Dec 1995(IBISv2.1)**

**IEC 62014-1 - May 1999(IBISv2.1)**

**V3.0 - Ratified June 1997**

**V3.2 - Ratified Aug20, 1999**

**ANSI/EIA-656A(Sept'99)**

**V4.0 – Ratified Jul 2002**

**V4.1 – Ratified Feb, 2004**

# IBIS (v3.2)



- Uses ‘keywords’ to define Model parameters
- This does not scale very well as technologies evolve faster than standards
- Very difficult to add a new keyword to support a new feature because it takes too long to incorporate into a standard
- A more flexible approach is needed

# IBISv4.1



- **Introduces multi-lingual extension through the use of VHDL-AMS, Verilog-AMS, SPICE to expand modeling**
- **No longer dependant on ‘keywords’**
- **Extremely flexible and extendible**
- **Able to model complex features of I/Os**

# Challenges of SerDes Simulation



- **HSPICE runtime is too long**
- **Complex features may not be modeled with SPICE alone.**
- **Matlab and Transfer functions used in modeling**
- **Difficult to simulate many multi-gigabit links simultaneously**

# Advantages of VHDL-AMS



- **International Standard**
- **Tool independent**
- **Does not contain proprietary information**
- **No encryption or NDAs are required**
- **Users are free to develop their own methodology**
- **Leverages feature rich and powerful *programming languages***
- **Fast!**

# What is being Modeled with IBISv4.1(VHDL-AMS)



- **XAUI (3.125Gbps)Test case includes:**
  - **A 1-tap FFE Transmitter (ASIC)**
  - **Multiple levels of Pre-emphasis**
  - **Receiver equalization (ASIC)**
  - **Mixed mode model ranging from SPICE, S-parameter and transfer function**

# IBISv4.1 (VHDL-AMS) Transmitter building block

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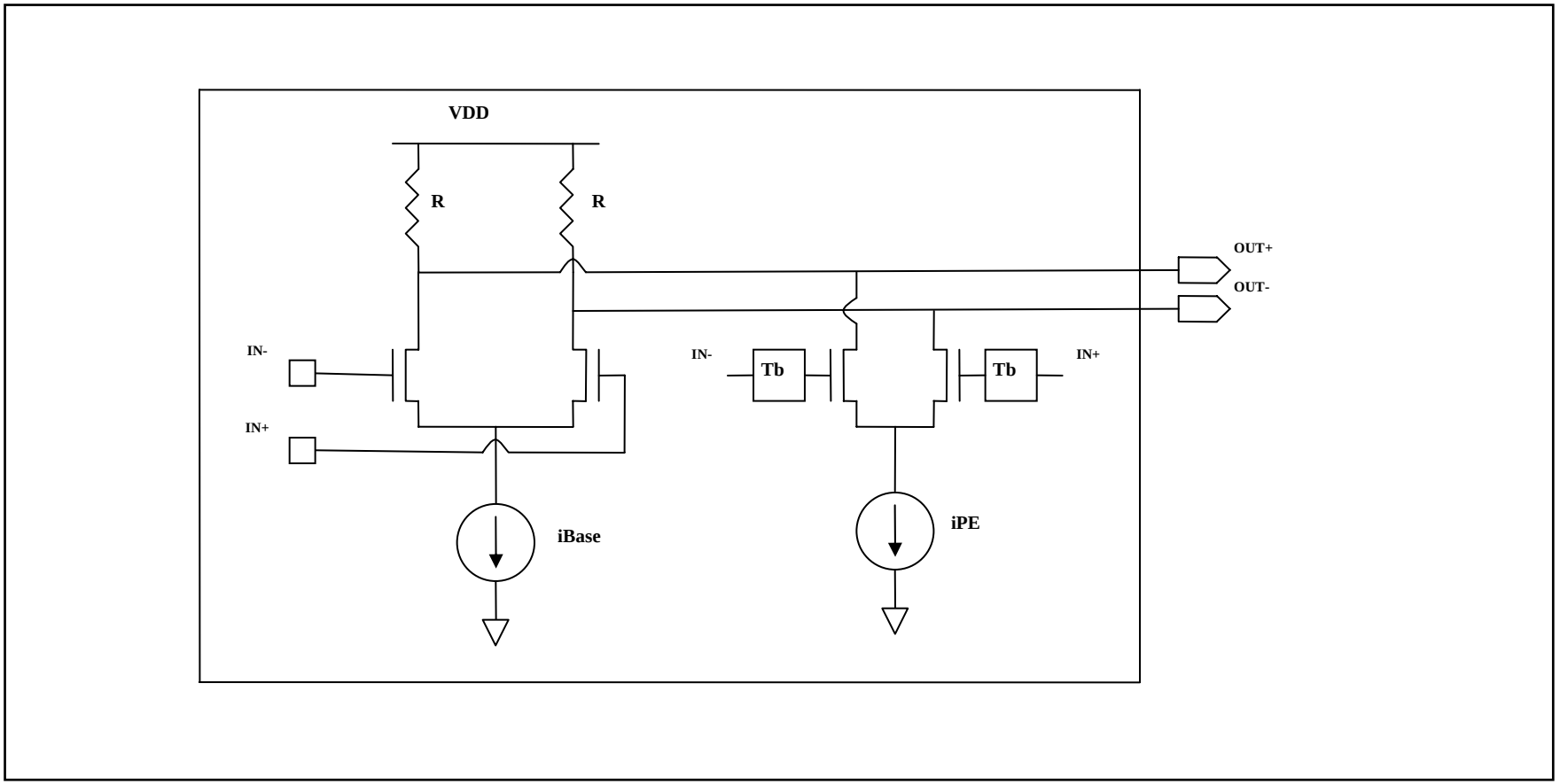
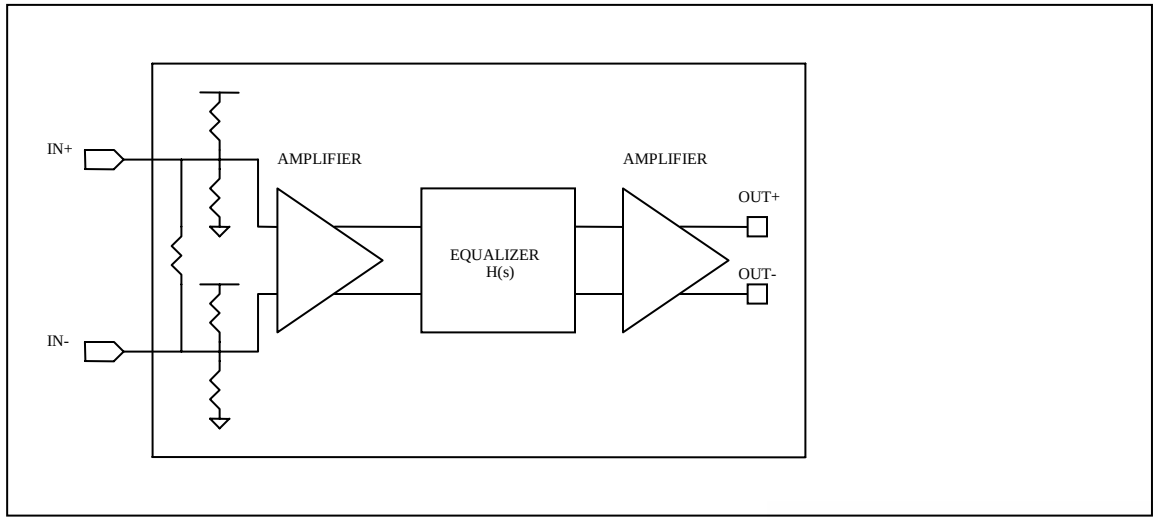
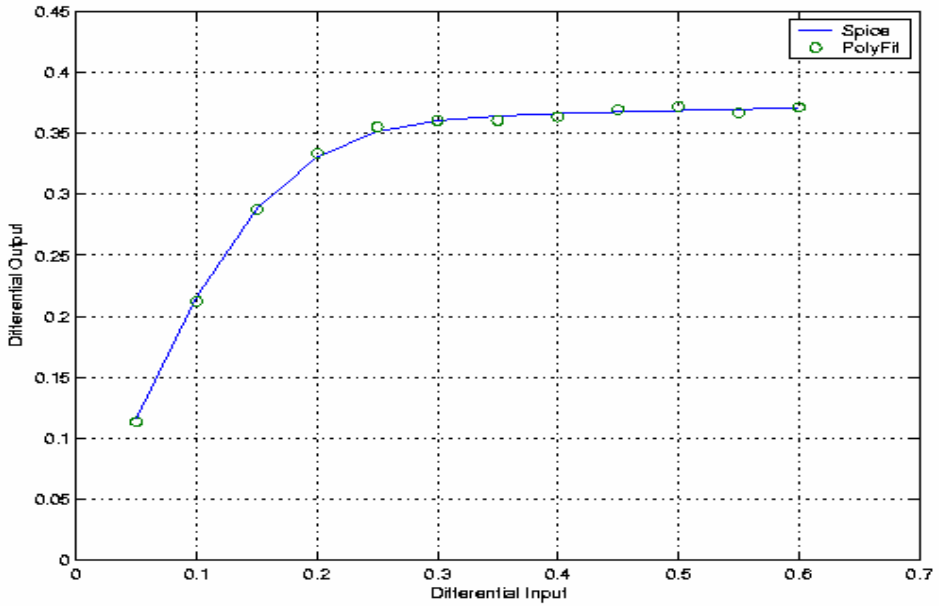


# IBISv4.1 (VHDL-AMS) Receiver building block



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# AMS call from within IBIS

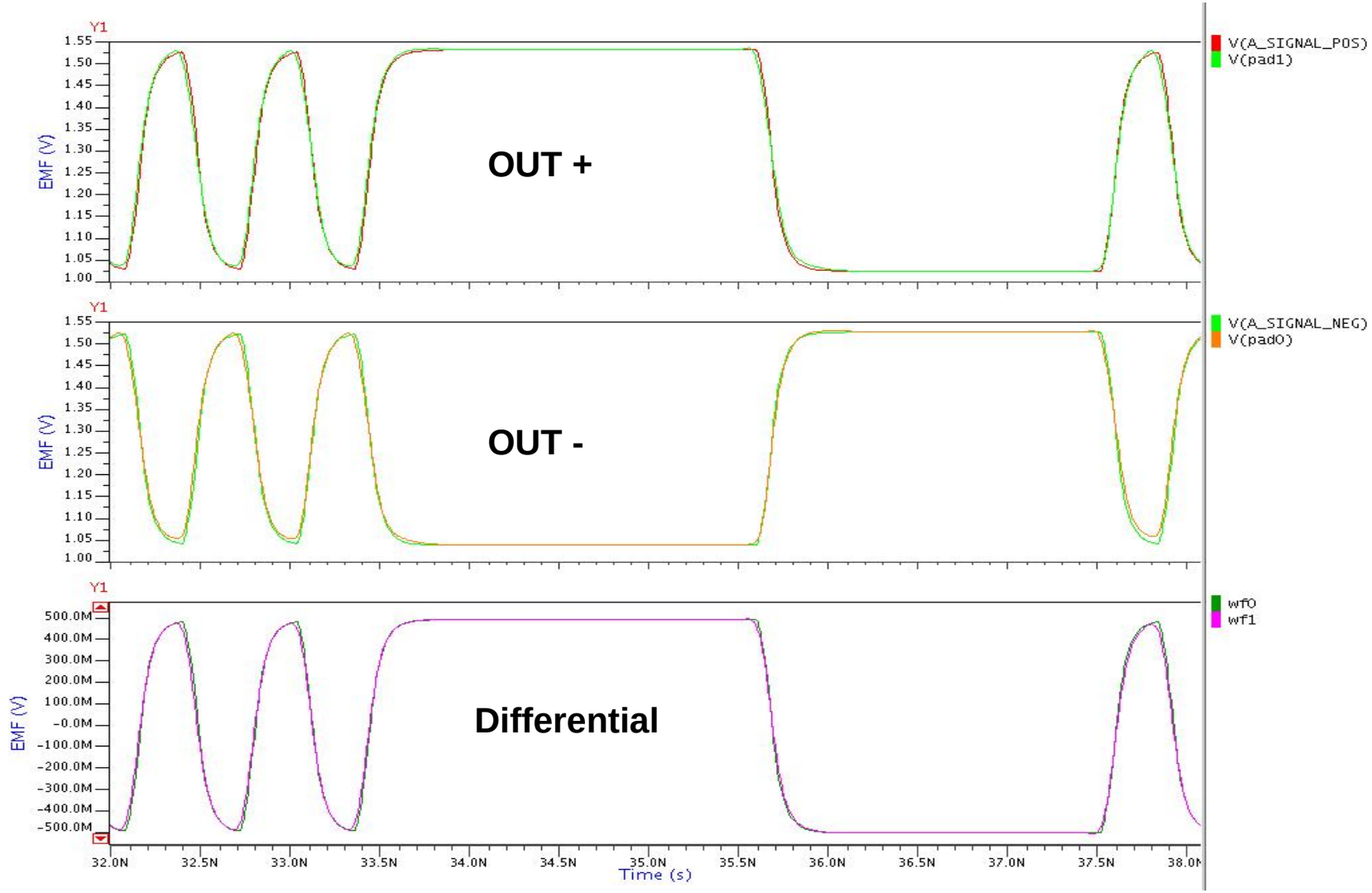


```
[Circuit Call] ICEM2
port_map  vdd_ic    21
port_map  vss_ic    22
[End Circuit Call]
|
|
[External Circuit]  ICEM2
Language  VHDL-AMS
|
| Corner  corner_name  file_name  subckt_name
Corner    Typ    icem_core2.vhd icem_typ2
Corner    Min    icem_core2.vhd icem_min2
Corner    Max    icem_core3.vhd icem_max2

Ports  vdd_ic vss_ic
|
[End External Circuit]
```

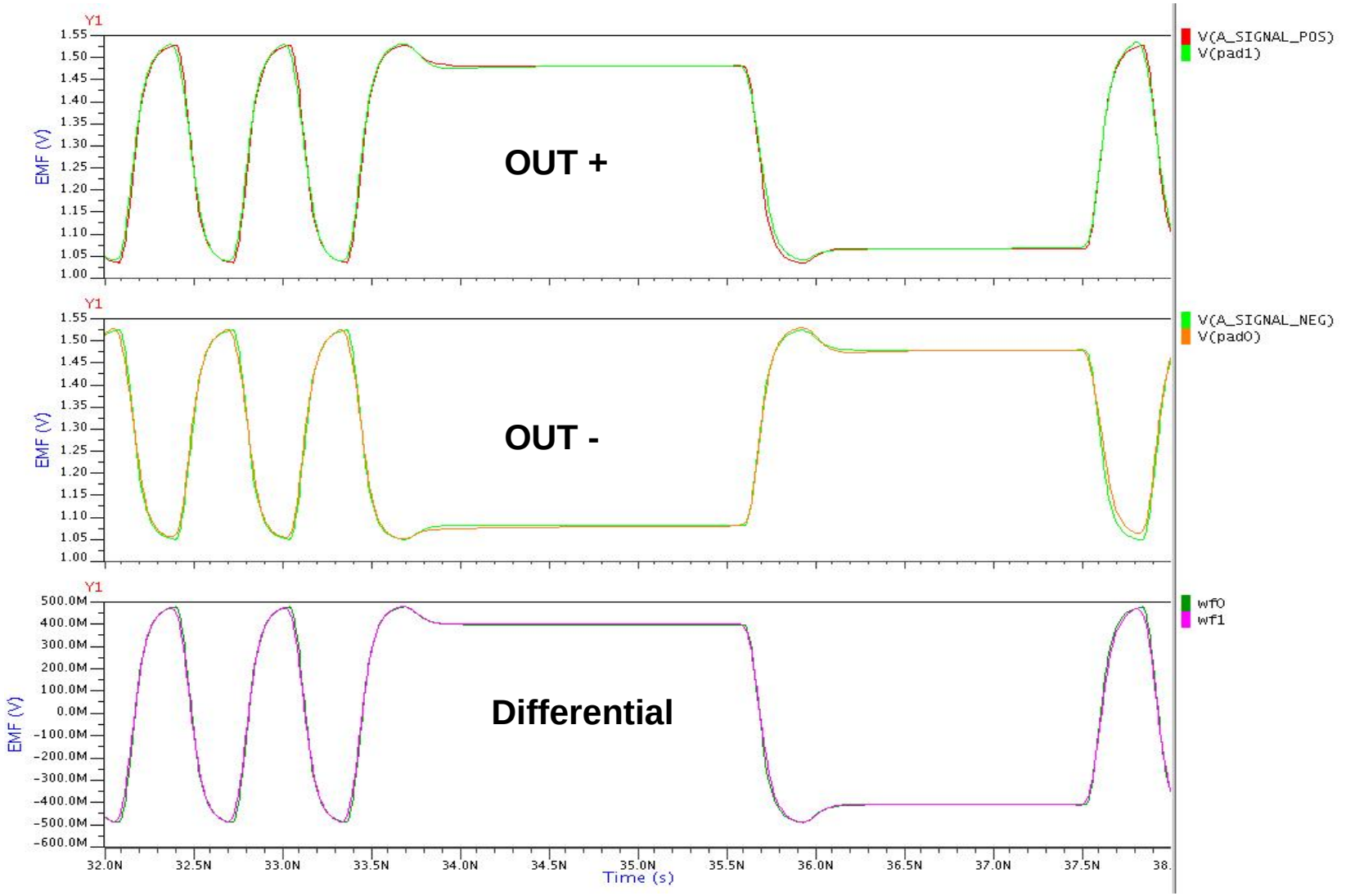
# Pre-emphasis level 0 – HSPICE vs AMS





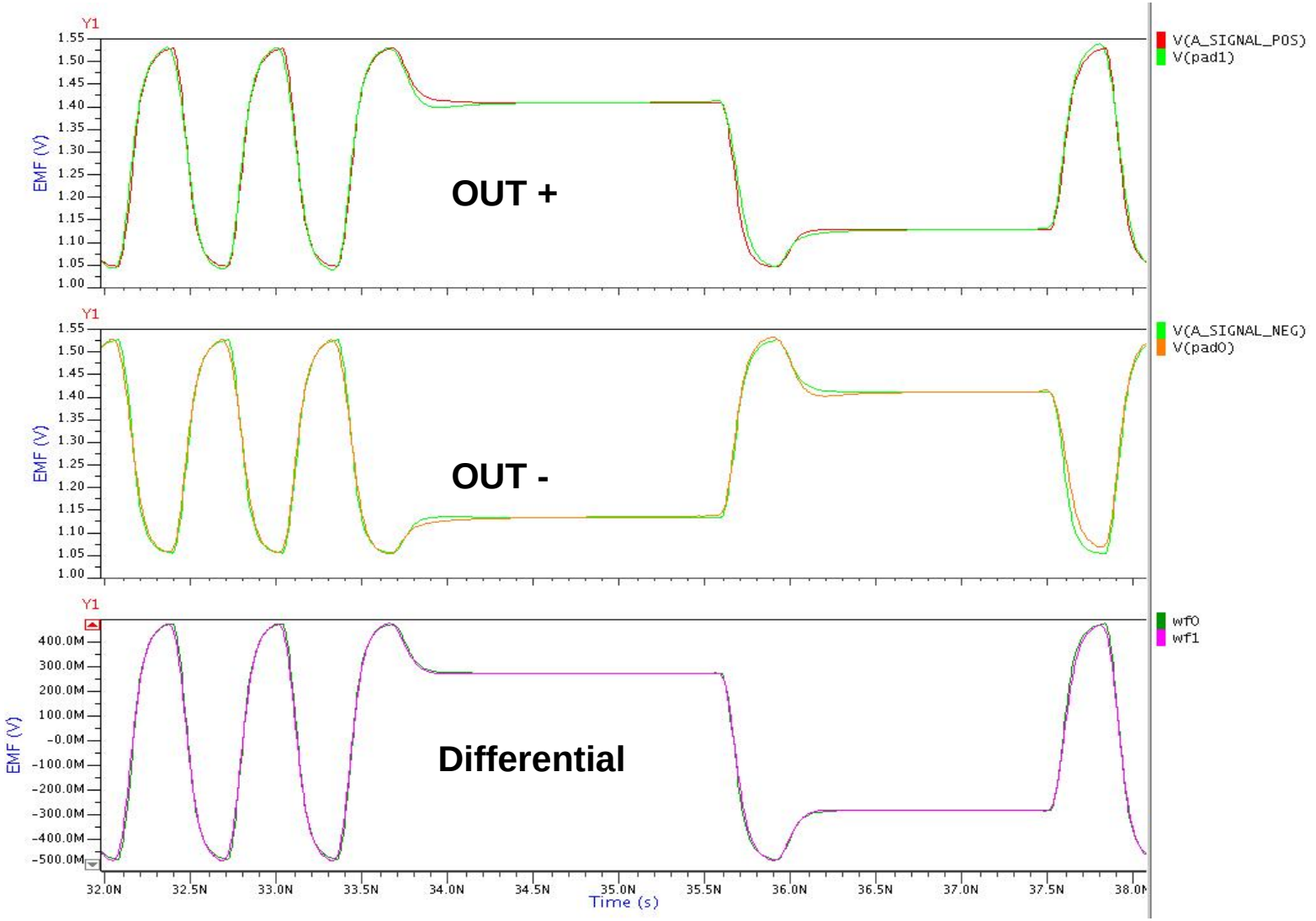
# Pre-emphasis level 3 – HSPICE vs AMS





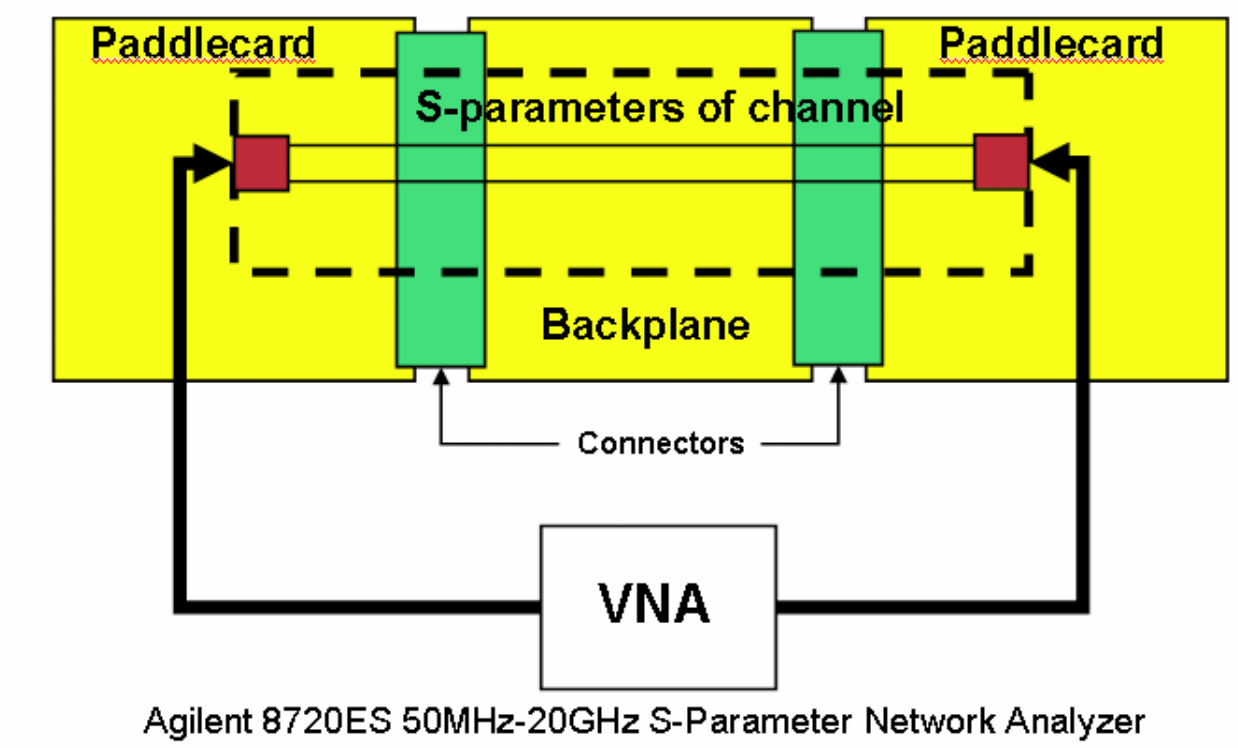
# Pre-emphasis level 7 – HSPICE vs AMS





# Measurement setup



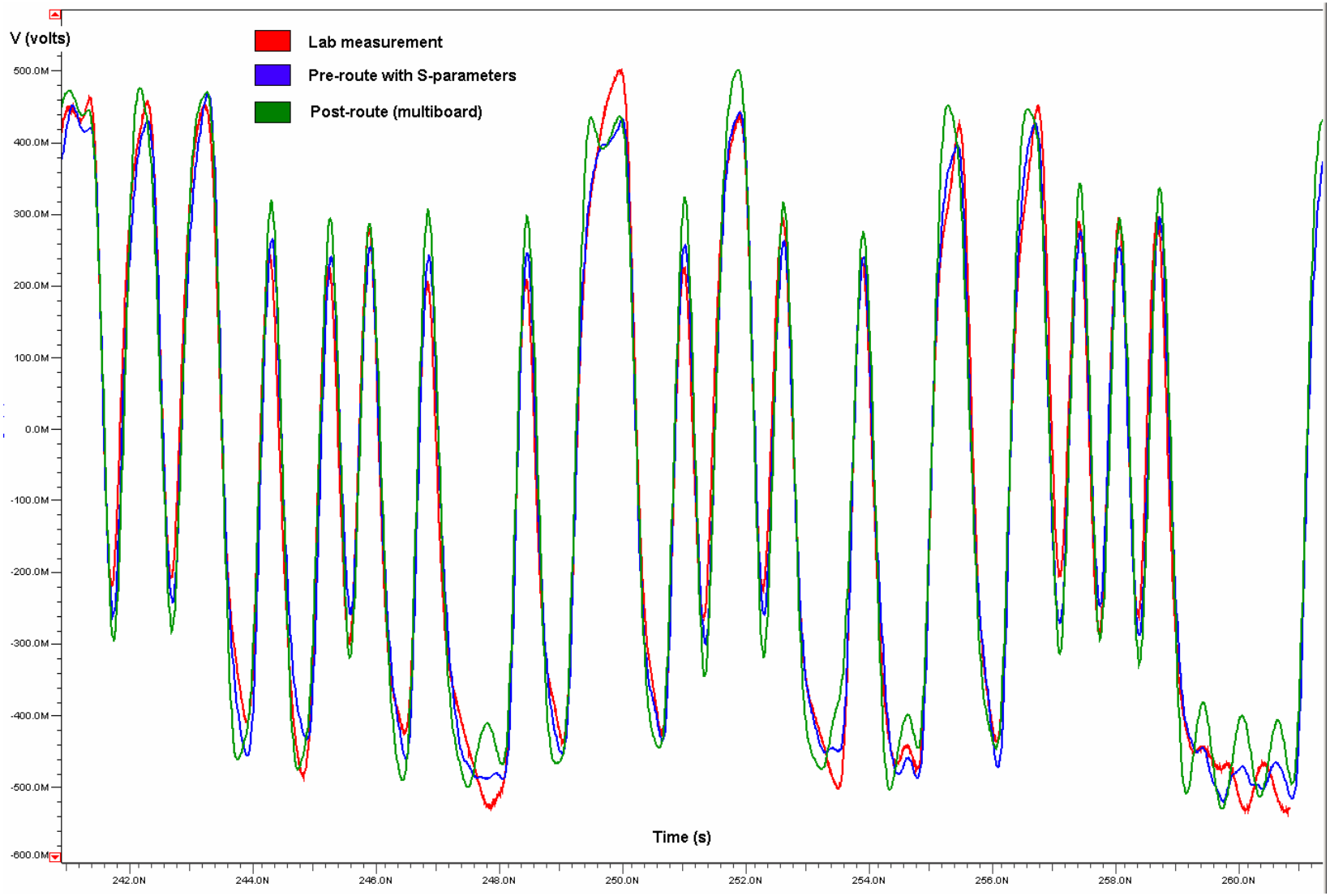



Agilent 8720ES 50MHz-20GHz S-Parameter Network Analyzer

- **Silicon measurement in Lab using VNA**
- **Post layout simulation using ICX**

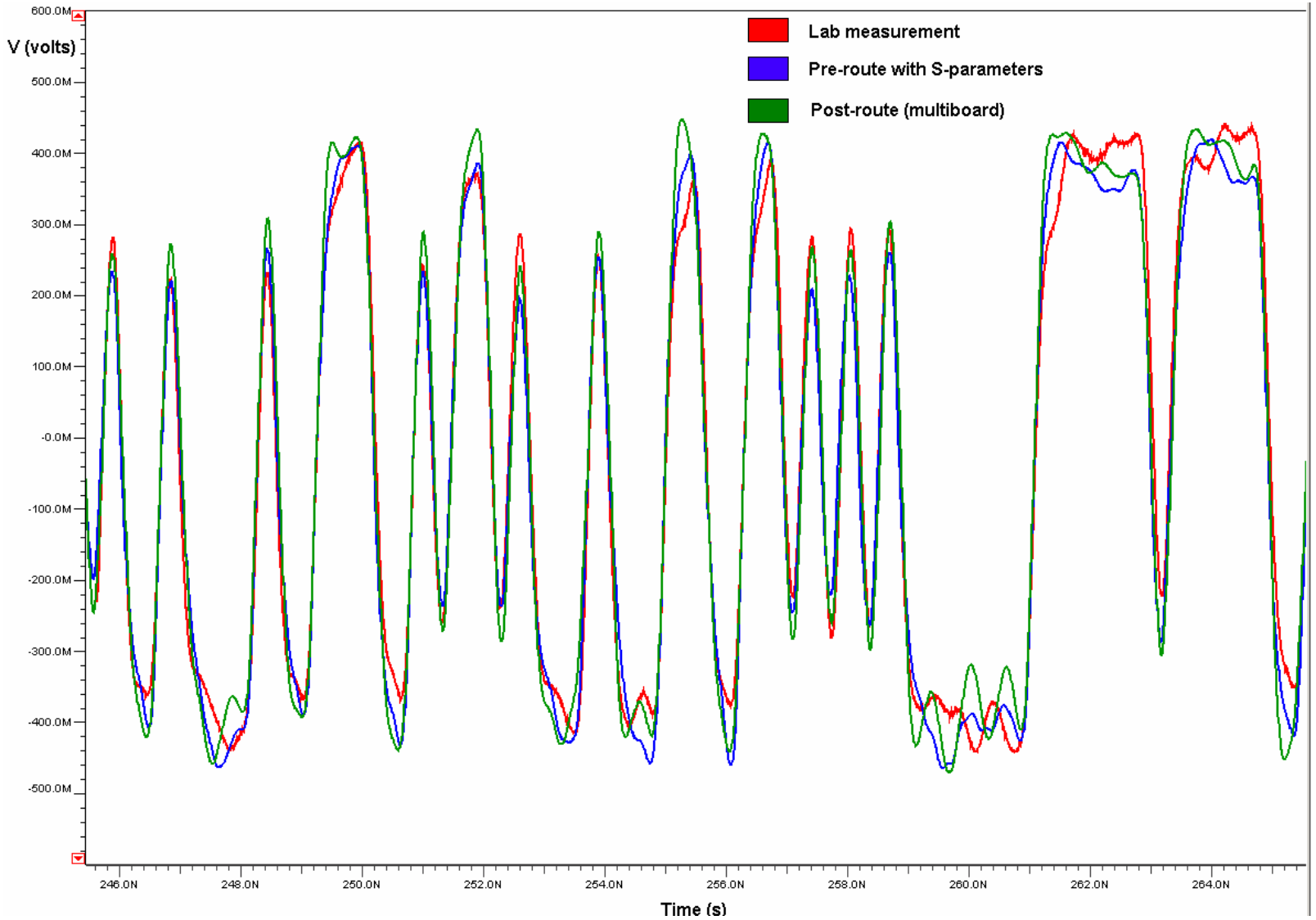
# Correlation with PE = 0





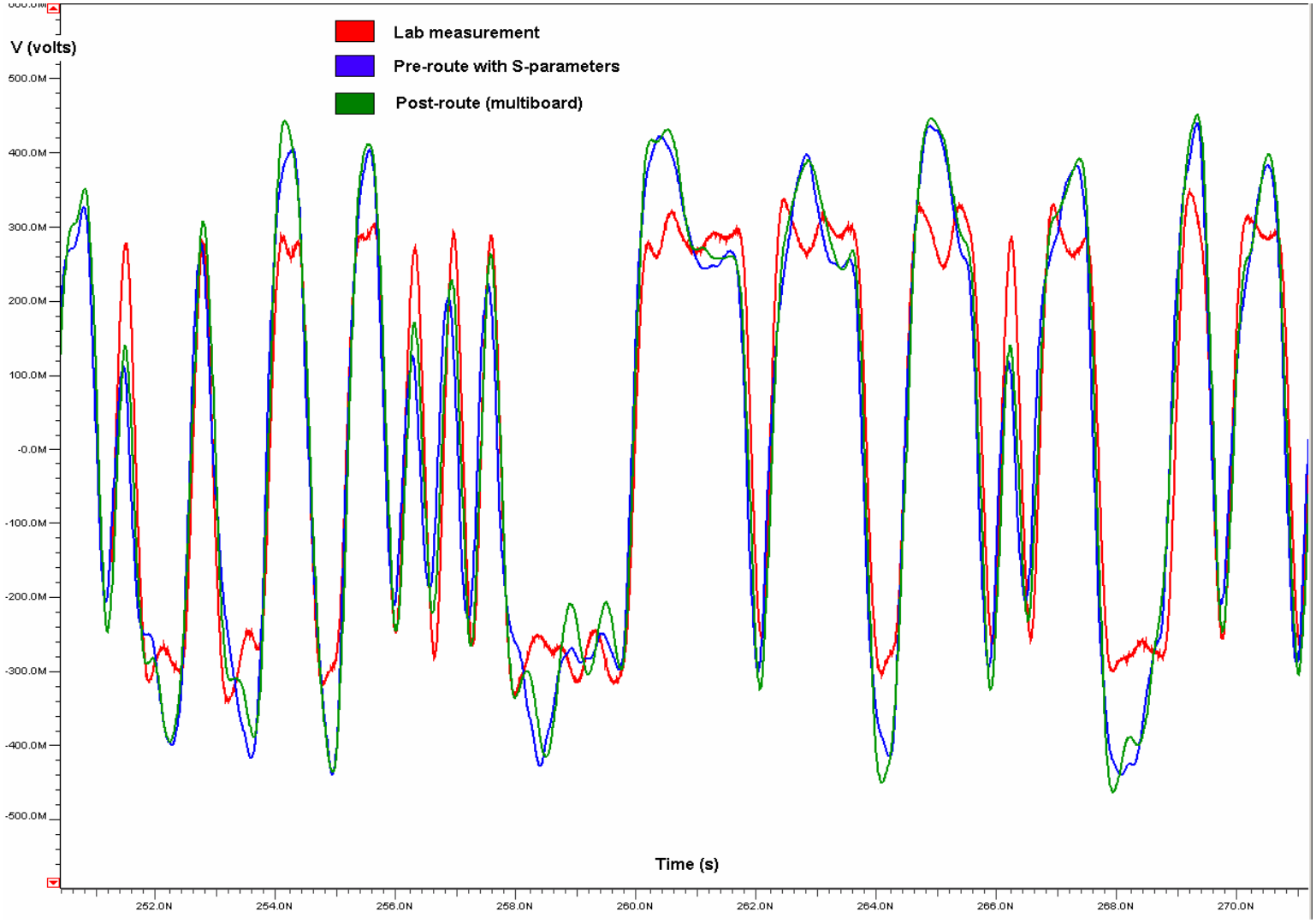
# Correlation with PE = 3





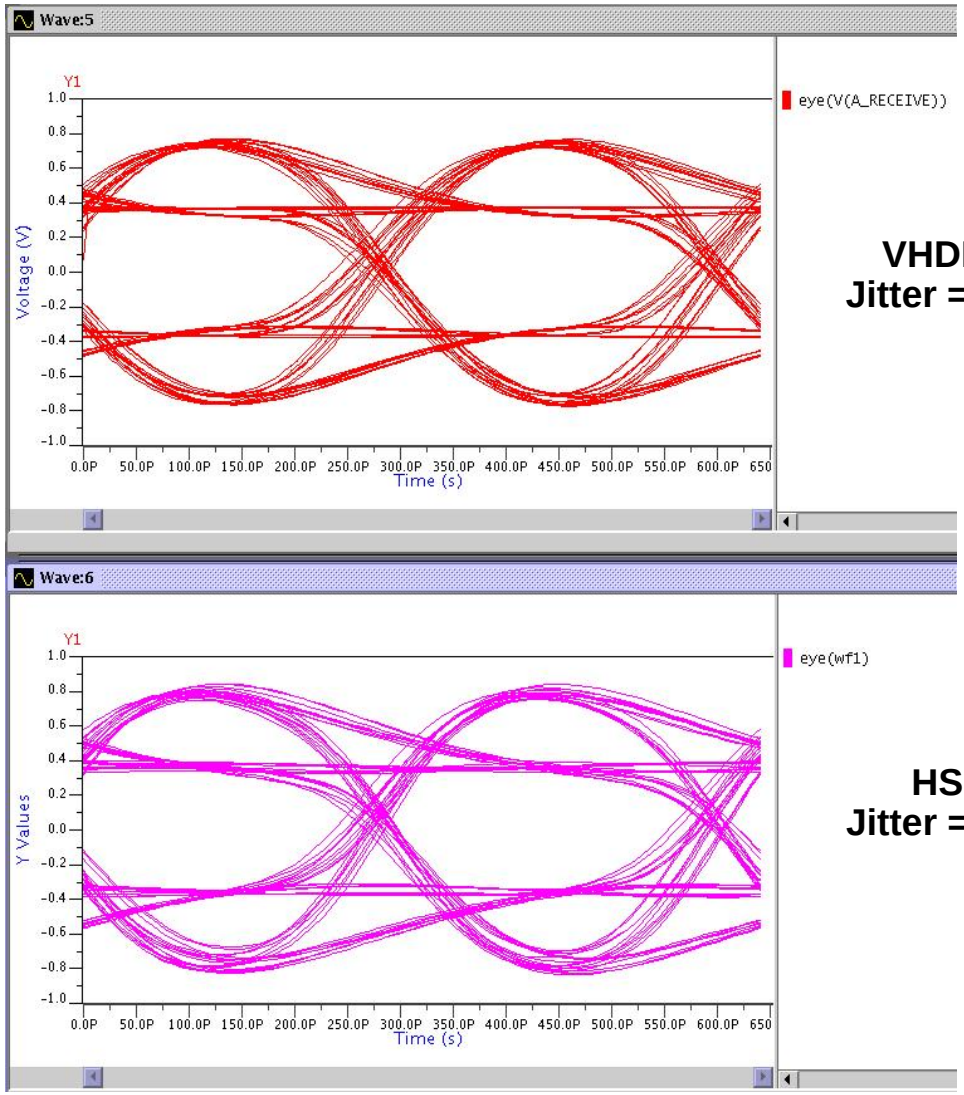
# Correlation with PE = 7





# Eye pattern correlation with PE = 0



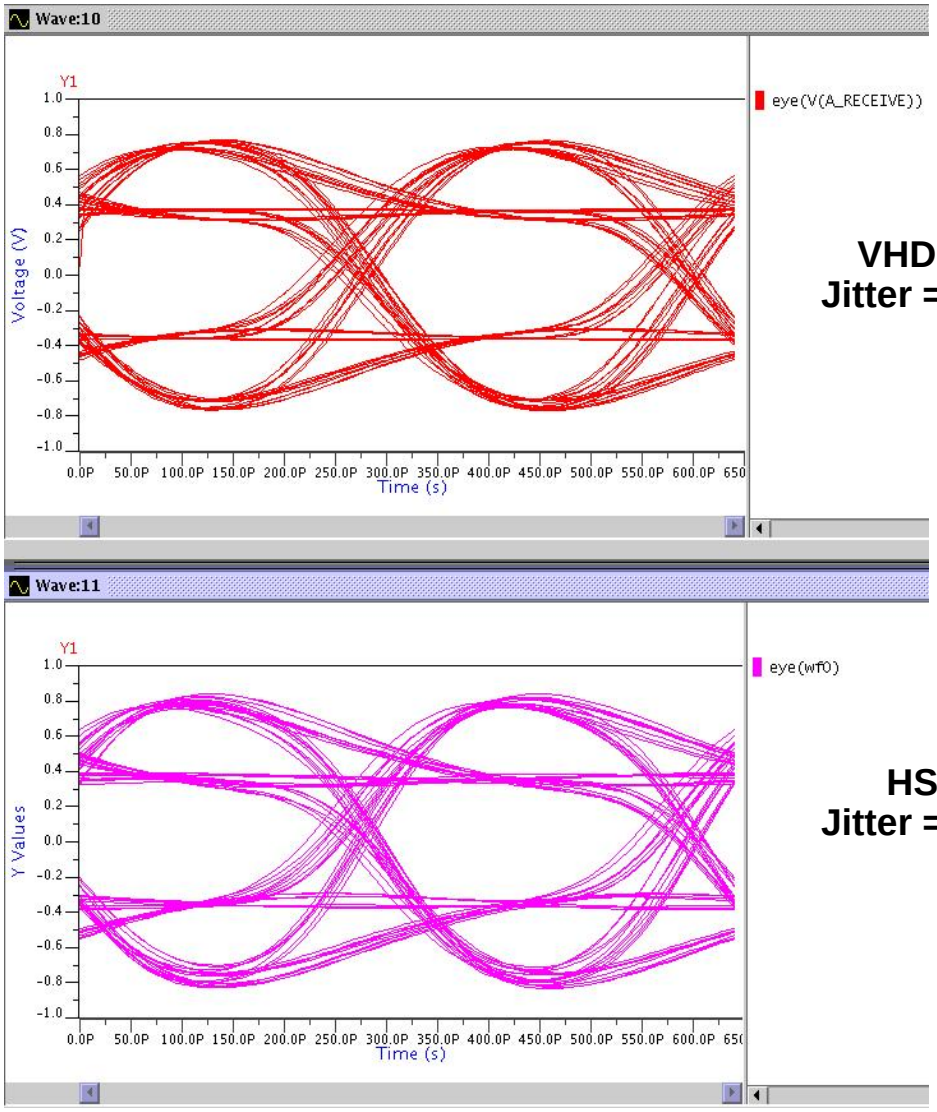



**VHDL-AMS**
**Jitter = 60.27ps**

**HSPICE**
**Jitter = 61.08ps**

# Eye pattern correlation with PE = 3



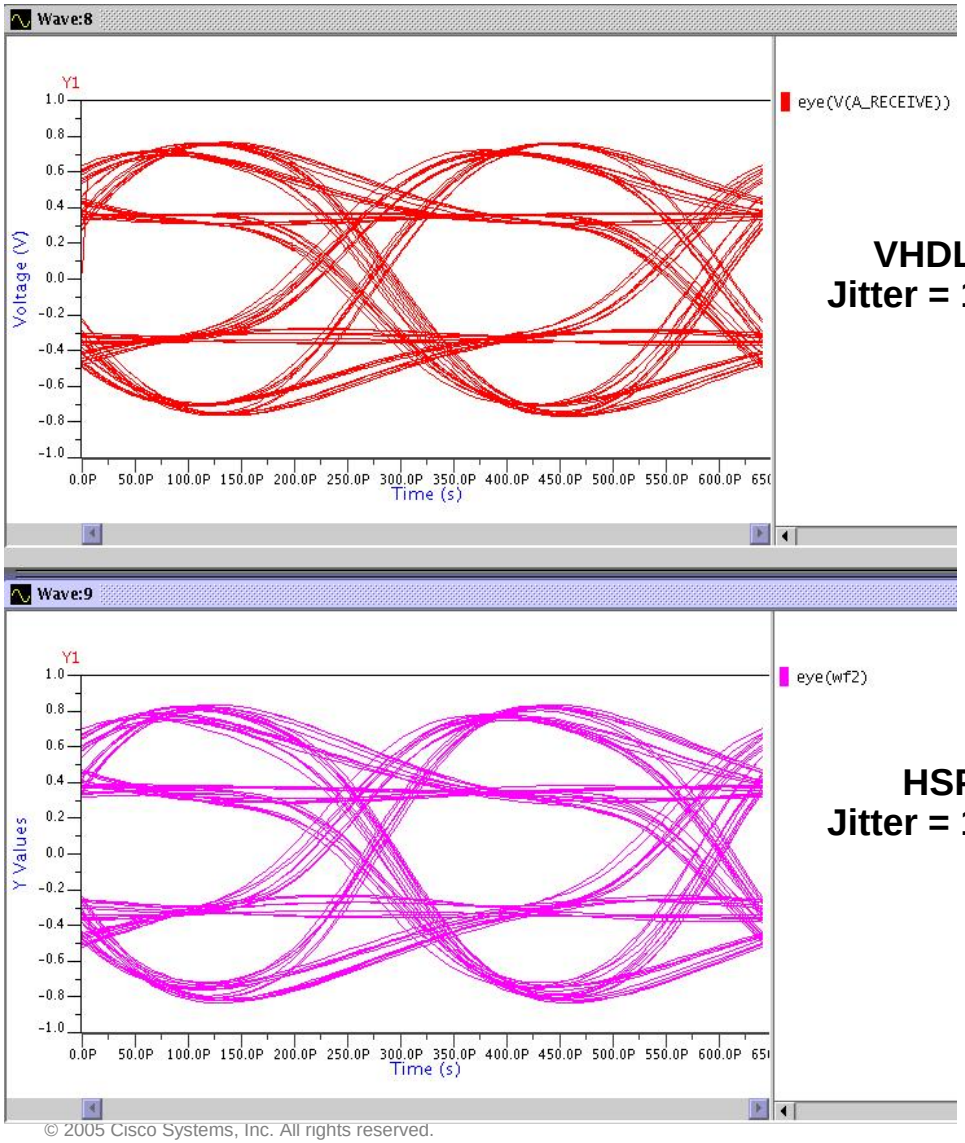



**VHDL-AMS**
**Jitter = 77.83ps**

**HSPICE**
**Jitter = 76.60ps**

# Eye pattern correlation with PE = 7



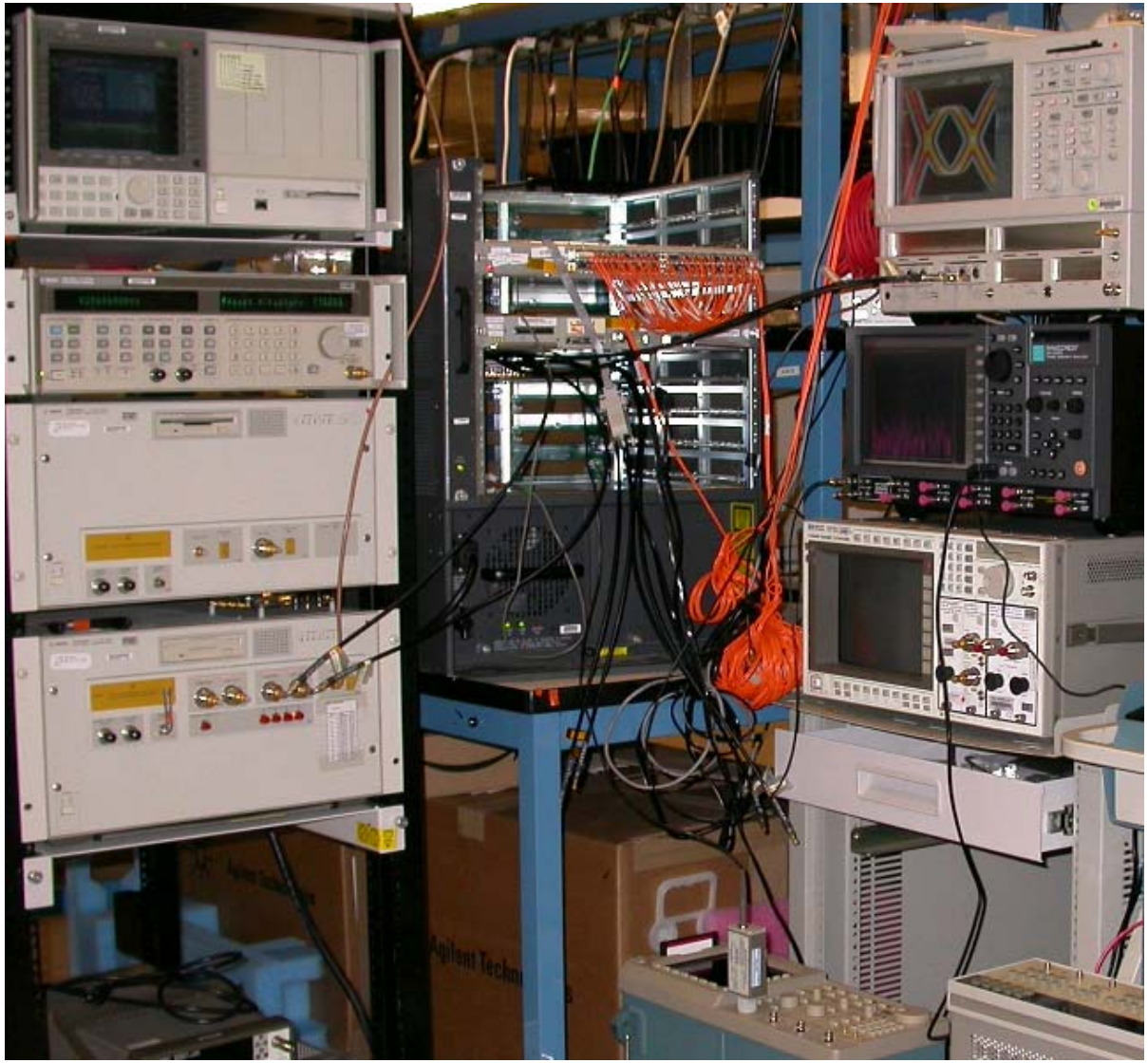



**VHDL-AMS**
**Jitter = 108.34ps**

**HSPICE**
**Jitter = 108.85ps**

# Lab setup used for Measurements





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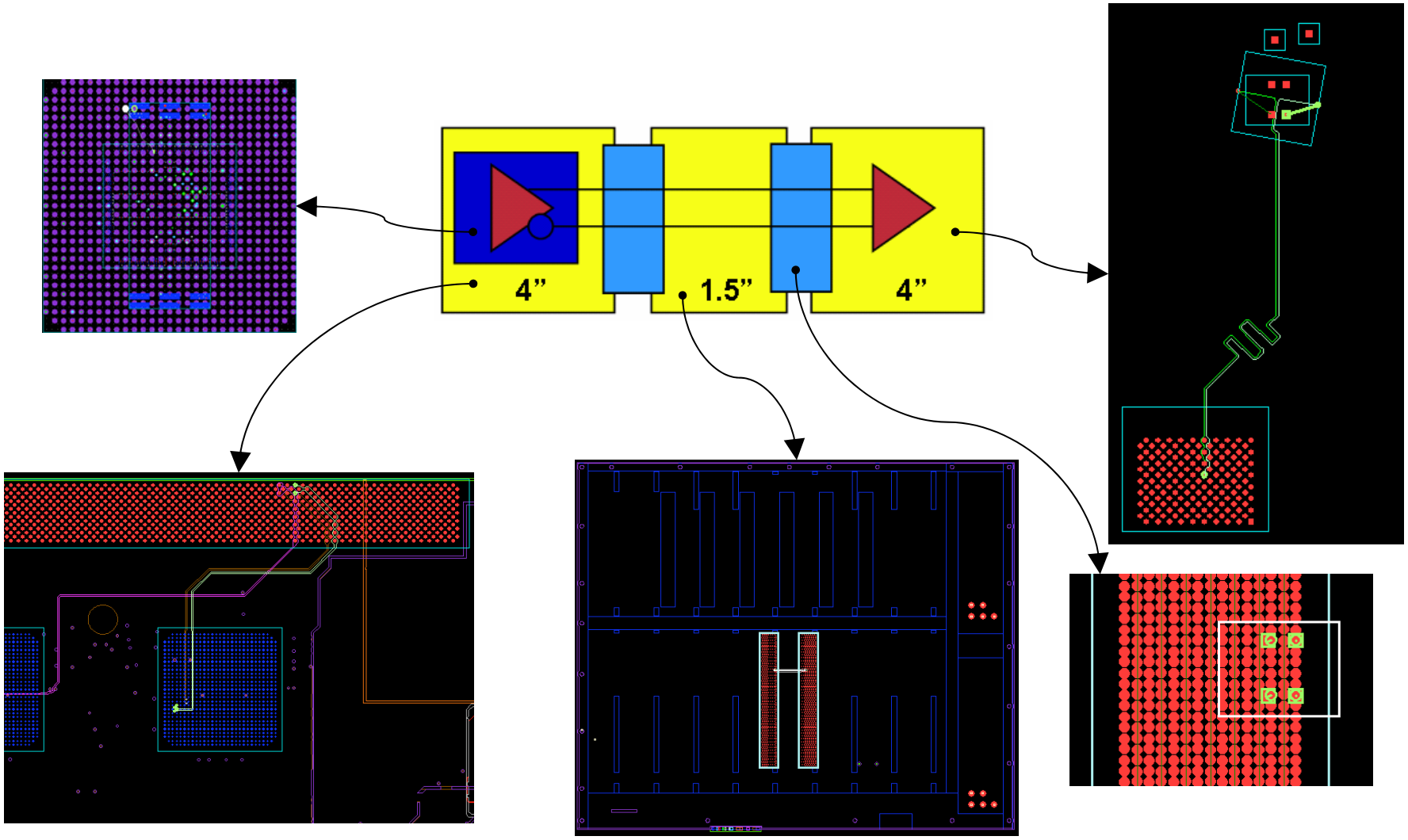
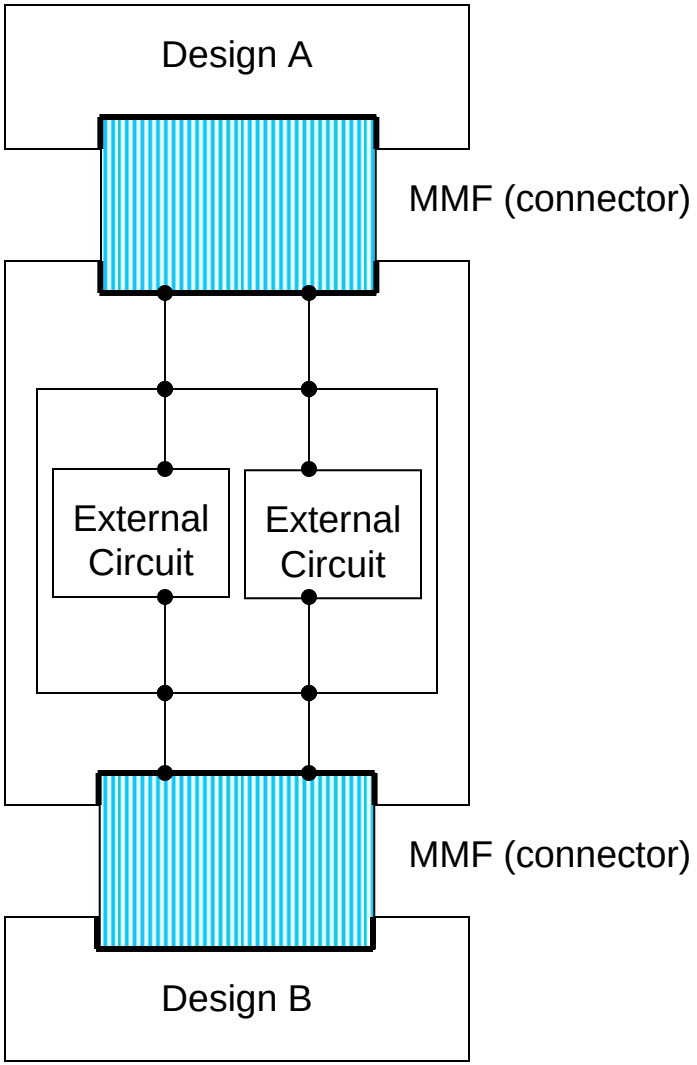
# Multi-board Verification with ISMB





# Connector Model

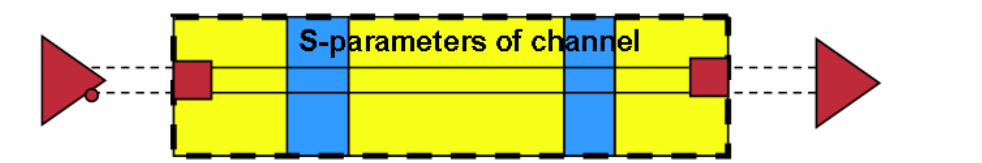





```
[File name]     spara_pluto_con_4port.ibs
[Notes]         calls a SPICE subcircuit that instantiates an S-parameter
                set of a connector.
|
|*******************************************************************************
|
[Component]     SConn_pluto_4port

[Pin]  signal_name   model_name    R_pin  L_pin  C_pin
1      dcp           NC            NA     NA     NA
2      dcn           NC            NA     NA     NA
15     bpn           NC            NA     NA     NA
16     bpp           NC            NA     NA     NA
|
|*******************************************************************************
|
[Diff Pin] inv_pin vdiff tdelay_typ tdelay_min tdelay_max
   1       2       0          0
   16      15      0          0
|
[Series Pin Mapping] pin_2    model_name      function_table_group
1 16  R_1G_ohm
2 15  R_1G_ohm
|
[circuit call] hsd5ab
port_map A1 1
port_map B1 2
port_map A2 16
port_map B2 15
[end circuit call]

[external circuit] hsd5ab
language  HSPICE
corner typ PLUTOCON.cir PLUTOCONN
ports A1 B1 A2 B2
[end external circuit]
|
|*******************************************************************************
|
[Model]         R_1G_ohm
Model_type      Series
Polarity        Non-Inverting
|                       typ             min             max
C_comp                  0               0               0

|
[R series]              10000000000 10000000000 10000000000


[End]
```

# Benchmark






- IBIS v4.1/VHDL-AMS and
- Hspice driver models

Probe model with
"fast settling" capacitor

**Preroute Simulation of 300ns (960 bits)**

- **IBIS v4.1/VHDL-AMS Driver/ S-parameter Channel/ probe model with "fast cap" simulated for 29 seconds (average of 5 simulation runs)**
- **HSpice Driver/ S-parameter Channel/ probe model with "fast cap" simulated for 7981 seconds (average of four simulation runs)**
- **275x Performance IBIS v4.1/VHDL-AMS versus HSpice**

**Platform: IBM Thinkpad with Pentium 4 @ 2 GHz – 1 GB RAM**
**Win XP, ICX Ver 3.4.01 Hspice Ver W-2004.09**

# Conclusions



- **IBISv4.1(VHDL-AMS) can solve complex modeling of multi-gigabit SerDes.**
- **275x faster than HSPICE**
- **Ability for EDA tools to simulate multi-board configurations without any run-time penalty (such as SPICE) and with excellent correlation.**

# What's next



- **There are many complex features that need to be modeled:**
  - **DFE (Decision Feedback Equalizer)**
  - **FFE (Forward Feedback Eq) – Multi-tap**
  - **CDR (Clock Data Recovery)**
  - **Higher Datarate and correlations**
  - **Target BER testing**
  - **Compliance to specifications**

# References



- **IBIS website:** http://www.eigroup.org/IBIS/Default.htm
- **IBISv4.1 spec:**

  http://eda.org/pub/ibis/ver4.1/
- **VHDL-AMS website:** http://www.eda.org/vhdl-ams
- **Mentor website:** http://www.mentor.com