IBIS in Applications

- Modeling Complex IO with IBIS

IBIS-JEITA Joint Meeting
March 24, 2005, Tokyo, Japan
Lance Wang

Outlines

- Device Models in EDA Tools
- New Challenges and New Studies
- An Applicable Solution - Macromodeling
- An Industrial Macromodeling Example

Outlines

- Device Models in EDA Tools
  - –Transistor Level Models
  - –Behavioral Models
  - –How EDA tools use Behavioral Models
- New Challenges and New Data
- An Applicable Solution – Macromodeling
- An Industrial Macromodeling Example

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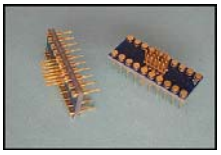
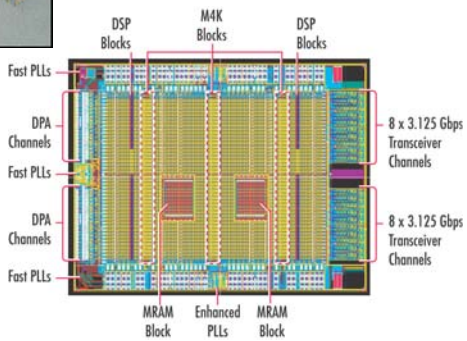
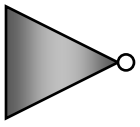
Device Models







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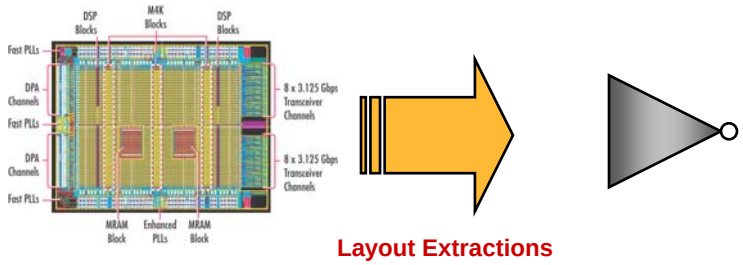
Spice Transistor Level Models



Layout Extractions

-Very Complicated
-A lots of unusable stuff
-Too slow in the simulations

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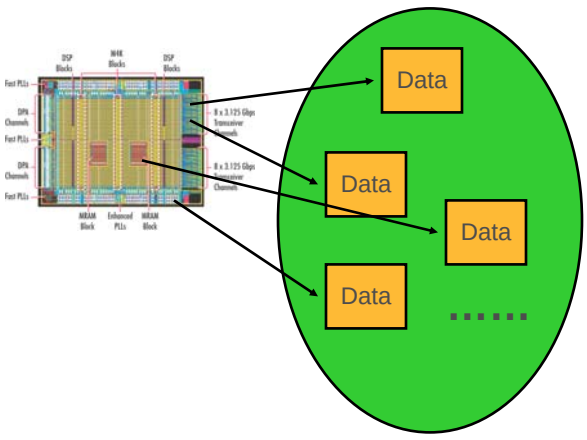
Behavioral Models



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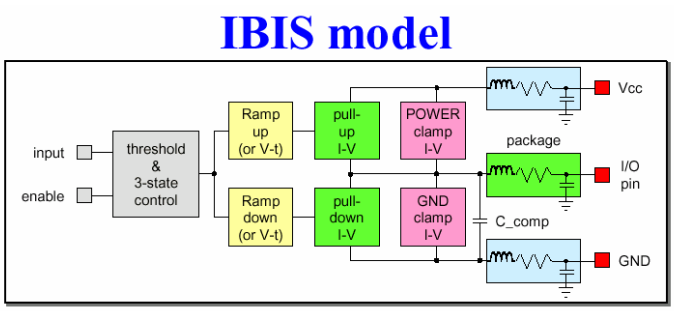
Behavioral Model



Block diagram of CMOS buffer

A basic IBIS model consists of:

four I-V curves: - pullup & POWER clamp
- pulldown & GND clamp

two ramps: - dV/dt_rise
- dV/dt_fall

die capacitance: - C_comp

packaging: - RLC values

for each buffer on a chip

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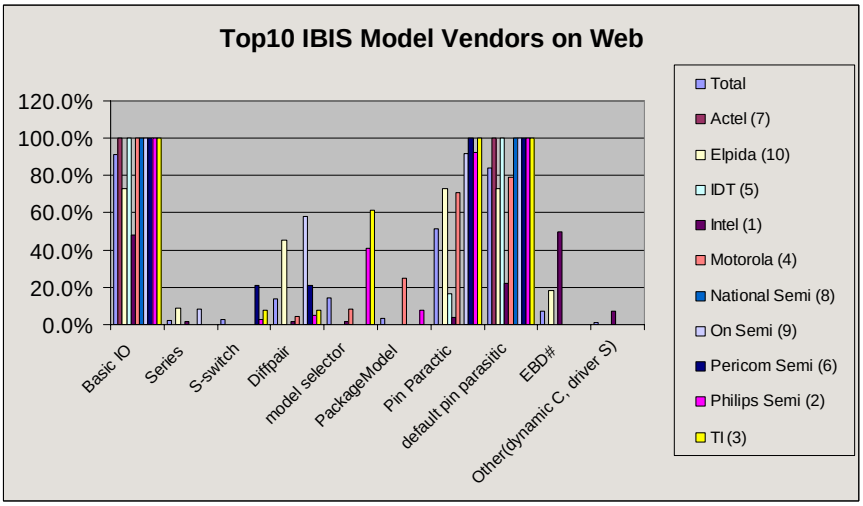
IBIS Model Vendors



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IBIS in EDA Tools

- Major EDA Simulators are supporting IBIS now
  - Cadence
  - Mentor
  - Synopsys
  - Zuken
  - Agilent

SPICE Simulators are taking IBIS now !!!

And many, many more ……

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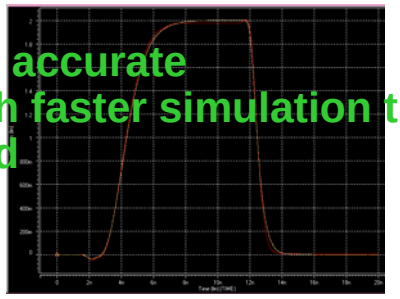
IBIS in EDA Tools

- Behavioral data in Spice simulators

  I(pad) = Ipd(V(pad)-V(gnd))*Wd(t) + Icd(V(pad)-V(gnd_c))

  + Ipu(V(pad)-V(pwr))*Wu(t) + Icu(V(pad)-V(pwr_c))

- Results are accurate
- Much, much faster simulation time
- IP Protected



HSpice Transistor Model vs. IBIS Model

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Support Advance IBIS Features

- Driver Schedule
- Series / Series Switch (FET)
- Submodel (Dynamic Clamps, Bus Hold …)
- Differential Pair
- EBD (Board Models)
- ICM (Interconnect Models)
- More ……

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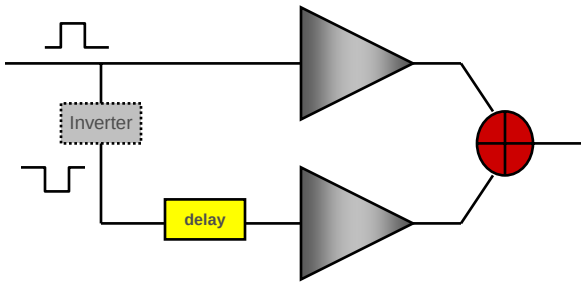
IBIS Implementation - Driver Schedule

[Driver Schedule]

Model_name	Rise_on_dly	Rise_off_dly	Fall_on_dly	Fall_off_dly
driver1	0.0ns	NA	0.0ns	NA
driver2	NA	0.666ns	NA	0.666ns



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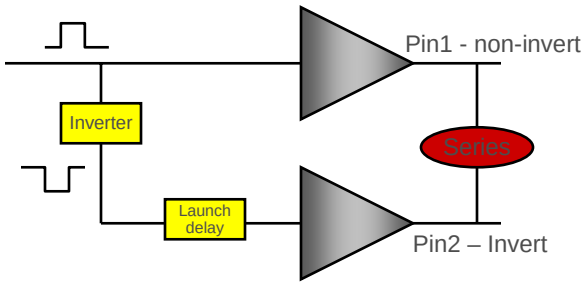
IBIS Implementation
- Differential Pair Driver

[Diff Pin]	inv_pin	vdiff	tdelay ……
1	2	0	1ns

[Series Pin Mapping]	pin_2	model_name ……
1	2	Series1



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Outlines

- Device Models in EDA Tools
- New Challenges and New Data
  - –Complex-IO Devices
  - –New Data from Survey
- An Applicable Solution – Macromodeling
- An Industrial Macromodeling Example

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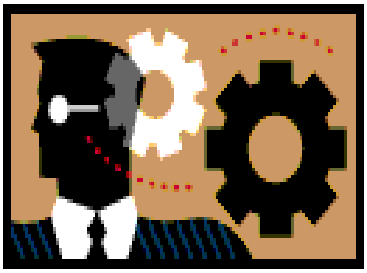
Then …… New Challenges



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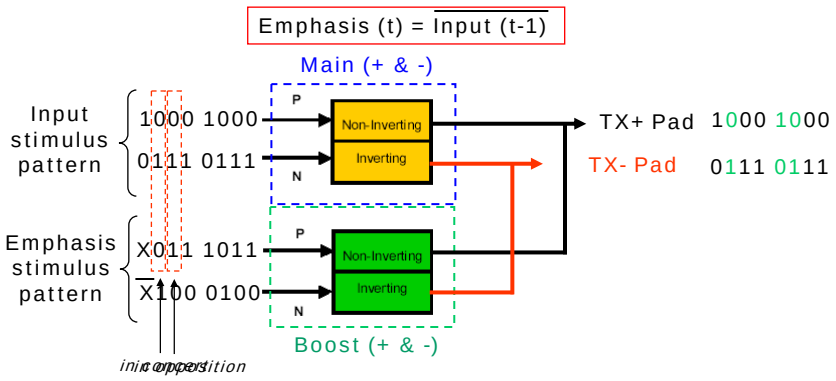
Complex-IO Devices

Pre-emphasis/De-emphasis



Picture from Michael Mirmak's presentation in DesignCon East IBIS Summit 2004

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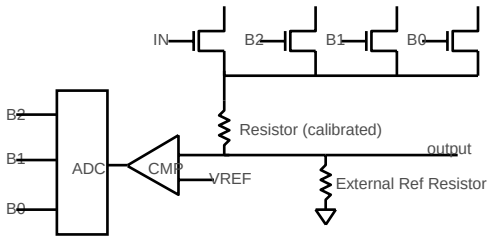
Complex-IO Devices

Self calibrating driver

(Calibrating Output Impedance only)
(For DDR2, when controller in a read cycle, the receiver is terminate)
(50 ohms. The resistor also requires to calibrate at run-time)



Note:
1) PMOS side is not being shown here.

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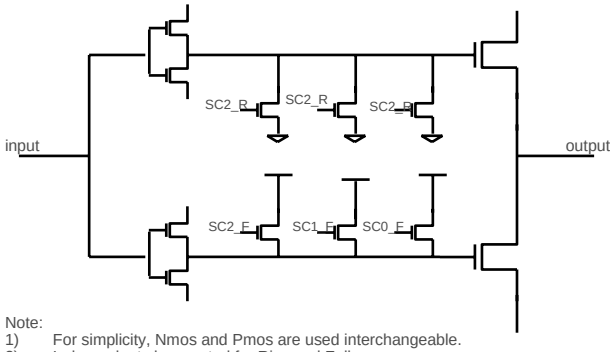
Complex-IO Devices

Driver with Slew Rate Control



Note:
1) For simplicity, Nmos and Pmos are used interchangeable.
2) Independent slew control for Rise and Fall.

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Complex-IO Devices

And More to Come … …

As Always for Technologies!!!

Where is IBIS?

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The Original "Box"

- 1st PCI Chipset (33 MHz)

IBIS

- 1st Pentium uP (66 MHz)

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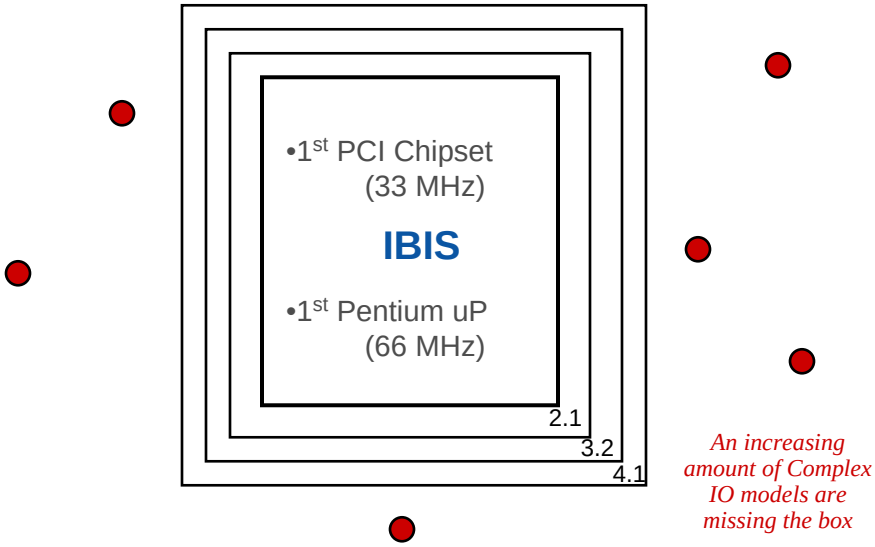
…and the “Box” did grow



An increasing amount of Complex IO models are missing the box

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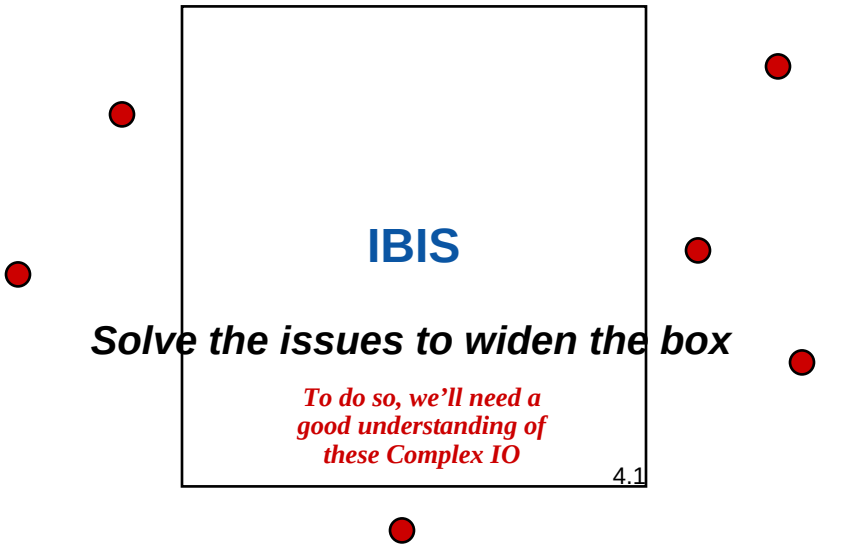
Our Mission



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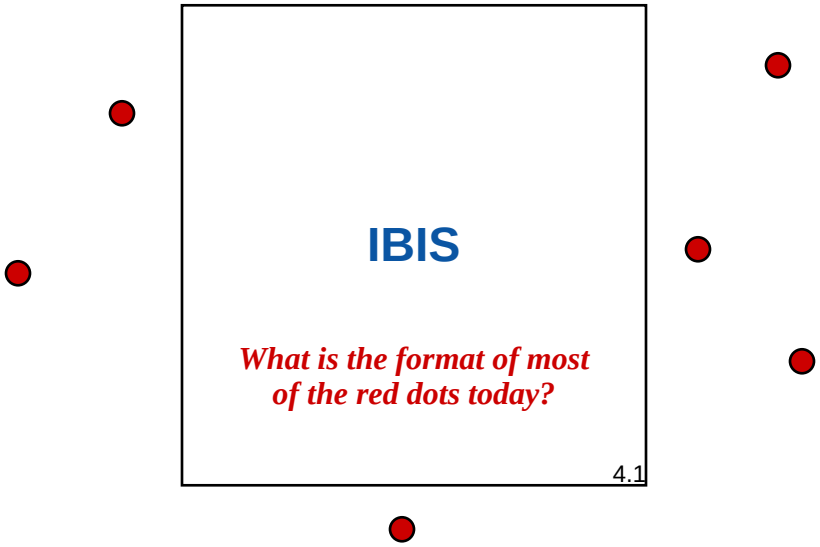
The Current Situation



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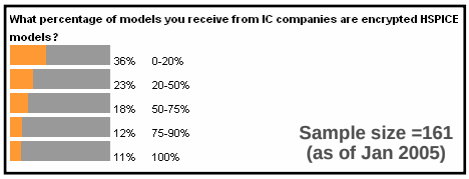
- All are involved with Complex IO
  - Majority were not CDS users
- Good re-introduction to the issues
- The issues are many
  - and the solutions weren't clear
- Will use this data to propose solutions
- Most want "industry standard solution"
  - but don't know how to get there
- So who will lead?

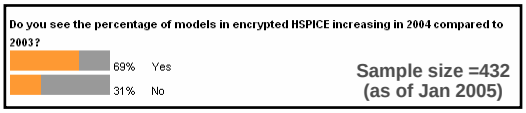
High-Speed PCB Web Surveys

- 64% say that more than 20% of the models they receive are Hspice



http://www.pcbhighspeed.com/discuss/user/non-frames/surveyresults.asp?surveyid=62

- 69% say that this percentage increased in 2004 over 2003



http://www.pcbhighspeed.com/discuss/user/non-frames/surveyresults.asp?surveyid=63

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HSpice Related Interview Questions

- "Do you want to see [External Model] HSpice?" - all "yes"
  - Half qualified this as a non-optimal short-term solution

This is actually already happening

- "Do you see HSpice as a long-term solution?" - all "no"
  - Unanimous reason: "it's too slow"

- As such, also unanimous in need to return to behavioral

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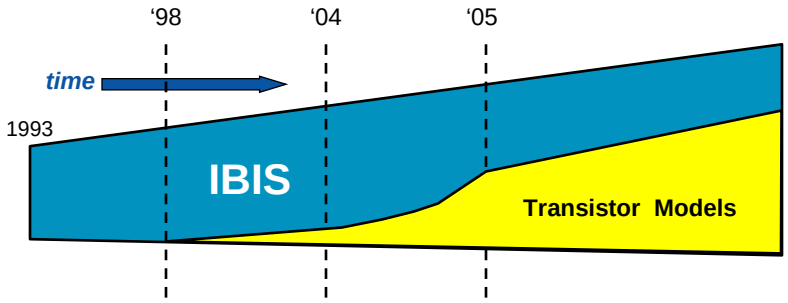
What has Happened



- IBIS enjoyed 5 years as THE digital IO model format
- Higher frequencies brought new issues and more skeptics
- Gigabit serial links brought rapid transistor model increase in 2004

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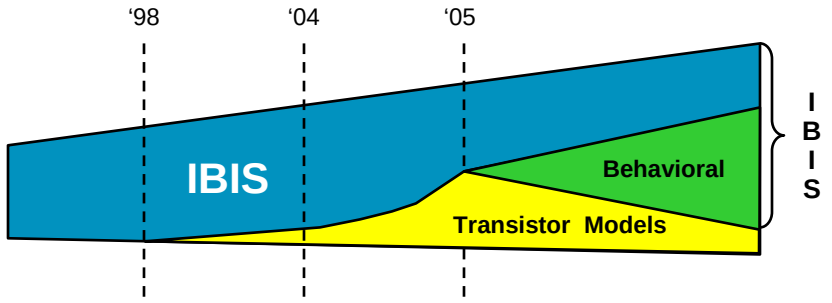
What Must Happen



- Enable faster behavioral solutions

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Features of Behavioral Solution

1. Fast
2. Protects IP
3. Template based
4. Works in many tools
5. Have links to IC design

What behavioral options exist?

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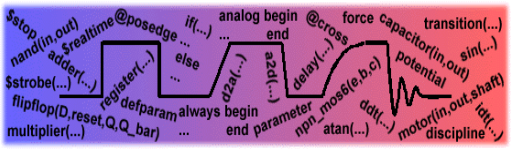
AMS Models – the Positives

- Most interviewed at this point are unfamiliar with AMS
  - When asked if they think AMS can be a good solution:

    3 said “yes”, 3 were hopeful, and 4 were unsure, 1 said no
- The experts list the following positives
  - Standards with documented specs
  - Mathematical freedom
  - Conditionals
  - File IO
  - Flexible language



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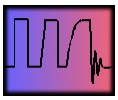
AMS Models – Issues to Solve



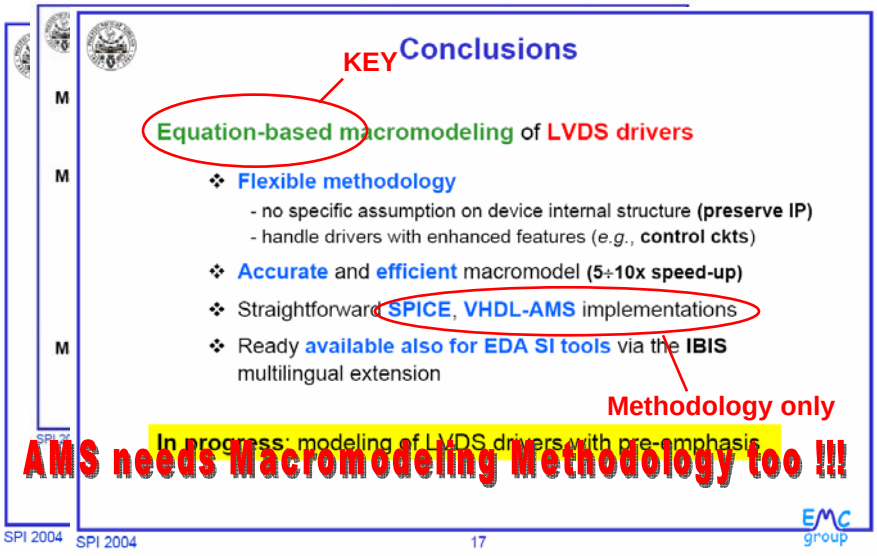
- Unfamiliar in SI world, learning curve exists
  - Must seed with templates / training
- Spec nuances/implementations (as with IBIS)
- Not naturally occurring in IO design
  - This is why transistor-level models get used
- IP protection
  - 3 would encrypt, 2 might, 4 are unsure, 2 would not

Any other solutions?

Outlines

- Device Models in EDA Tools
- New Challenges and New Data
- An Applicable Solution – Macromodeling
  - What is Macromodeling and Why
  - Our Experiences
- An Industrial Macromodeling Example

What is MacroModeling and Why?



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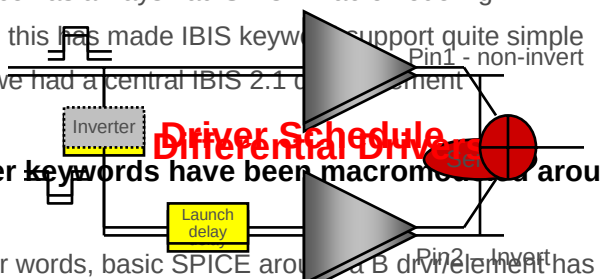
What Our Experience has Shown

- Spice Macromodeling is everywhere
- Cadence has always had SPICE macromodeling
  - And this has made IBIS keyword support quite simple
- Once we had a central IBIS 2.1 [illegible]ment



All later keywords have been macromodel around it

- In other words, basic SPICE around a B driver/element has handled everything IBIS has added for the last 10+ years
- Template is another **KEY** for Complex-IO Modeling

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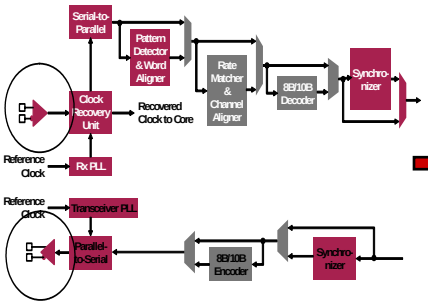
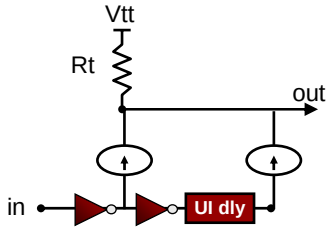
Macromodel from architecture templates

- Most modern devices are based on known DSP circuit architectures



Known circuit architecture

Match template parameters to Layout model to get an accurate macromodel



Macromodel template with parameters

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Behavioral SPICE Solutions

- 2.5 Gbps PCIe SerDes Chipset
  - http://www.cadence.com/company/newsroom/press_releases/pr.aspx?xml=090804_intel
- 1.5 Gbps S-ATA SerDes
  - http://www.designcon.com/conference/7_tc3.htm
- Differential pass-thru receiver
  - http://www.vhdl.org/pub/ibis/summits/jan00/telian.zip
- Adjustable FPGA SerDes
  - http://www.altera.com/corporate/news_room/releases/releases_archive/2004/products/nr-cadence_design_kit.html
- Front-side bus driver, impedance control, SSN, & gate choke effect
  - http://www.cadence.com/company/newsroom/press_releases/11_16_98_SQ_Intel_Merced_Processor.doc
- Others under NDA, mostly higher speed SerDes

The technique has been used for many "beyond IBIS" complex IO models

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SPICE Macromodeling

- Many tools and users have experience with it
- With template help, model makers are succeeding
- Academia is quite engaged in macromodeling research
  - http://domino.research.ibm.com/acas/w3www_acas.nsf/images/proposals_04.05/$FILE/madhavan.pdf
  - http://domino.research.ibm.com/acas/w3www_acas.nsf/images/projects_03.04/$FILE/canavero.pdf
  - http://www.spi.uni-hannover.de/2004/presentations/spi04_s08_p02_Stievano.pdf
  - http://www.ece.ncsu.edu/erl/html2/papers/paulf/2003/paulf_2003_10_varma.pdf … etc.

Outlines

- Device Models in EDA Tools
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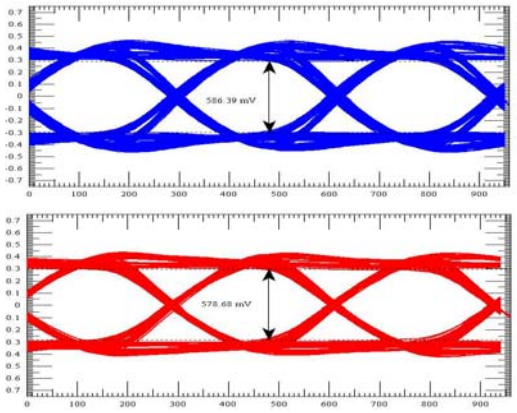
- An Industrial Macromodeling Examples

Industry example- Altera Stratix GX

"Altera successfully adapted the MacroModel templates to produce fast and accurate models of our multi-gigabit transceivers. Not only did the resulting model correlate well, it also simulates between 20 to 400 times faster than its transistor-level counterpart. And the model can be easily adjusted to match the behaviors of actual silicon measured in the lab."



Correlation: MacroModel vs TransistorModel

"Overall, the templates were simple to work with and very valuable amidst the challenges of multi-gigahertz design."

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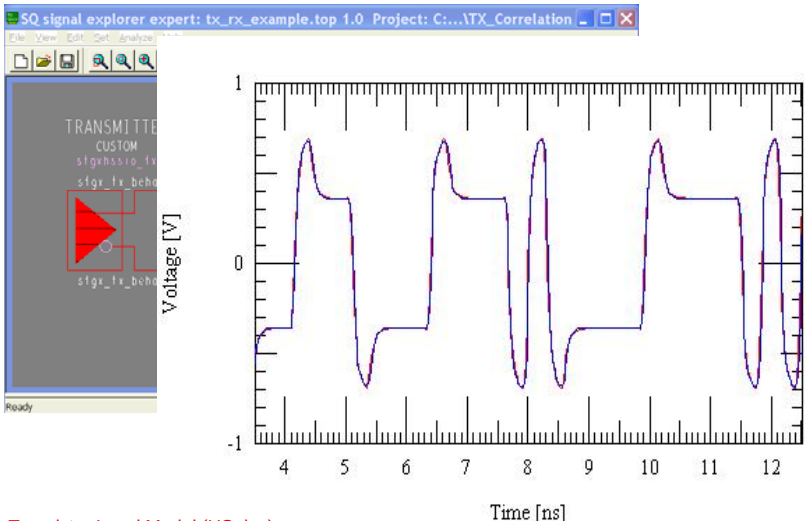
Correlation - Altera Stratix GX



- Transistor Level Model (HSpice)
- Spice Macromodel (Cadence DML)

Transmitter output at factor=5

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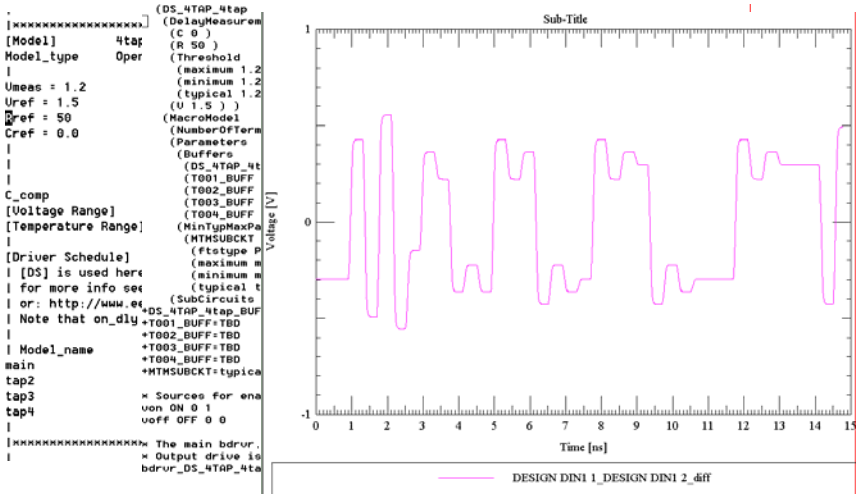
And, the latest news

- Driver Schedule in IBIS for 4 tap pre-emphasis buffer is working



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cadence

Thank You

謝謝

IBIS