





It is easy to get samples of the component that needs to be modeled unless the component is not in production yet. In most cases you do not need to sign a NDA to get samples or a datasheet.

With SPICE you frequently need to get a NDA signed which increases the time and cost of making a model. Lawyers do not do their work for free.

Many semiconductor vendors have proprietary SPICE simulators. Modeling a component which has a proprietary description means you will need a copy of the proprietary SPICE simulator.



Its easy to measure the DC characteristics to the level of accuracy required. Getting good AC bandwidth requires good fixturing, good probing and high bandwidth samplers.



Most IBIS features are described with either IV and VT tables or by taking the data right off the spec sheet. Dynamic clamps and Bus Hold require special setups and measurements. TT is easy to measure. We have not seen any demand for these features.



The bandwidth of the scope should be at least 5 times the bandwidth of the signals you model. Most parts these days have 200 to 500 psec transitions. This implies a scope bandwidth of at least 8.75 GHz.



This is one of Teraspeed's test setups. There are 5 power supplies, one scope with 20 GHz sampling heads and a 24 channel word generator. Also pictured is a hot/cold plate to vary the case temperature from 0 to 100C. There are a lot of other tools required such as probes, attenuators, etc.





Most outputs will source of sink between 100 and 500 ma. We have seen parts that can sink over 1 Amp. The supplies need to be able to both source or sink current to make these measurements.

Many of today's chips have 3 or more supply connections. A core supple, a I/O supply or two and maybe some bias supplies.





Like most things the more automation you can use the more productive you can be. Also properly designed tools will prevent errors form occurring. Many of the problems seen in IBIS models are just syntax issues. Automated tools will prevent those kinds of mistakes.

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Keeping the time correlation between waveforms is very important. The scope must be triggered off some external event, not the waveforms of interest.



Here is a complete set of VT curves for a part measured over process, temperature and voltage. The upper set of waveforms are with the 50 Ohm termination tied to Vcc and the lower set for the output terminated to ground. It is easy to see the change in prop delay in the component from the max to typ to minimum set of conditions.





These are the IV characteristics of the same component over process, temperature and voltage. The upper window shows the pull up characteristics, the middle the pulldown and the lower the input.



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This shows some of the screens in our database. All pin and specification data is stored in the database.

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Too may model makers neglect step two in the process. There are too many models that will not pass the IBIS parser.





Would a model that has voltage and temperature variation only, no process information give the SI engineer more useful information than a typical only model.