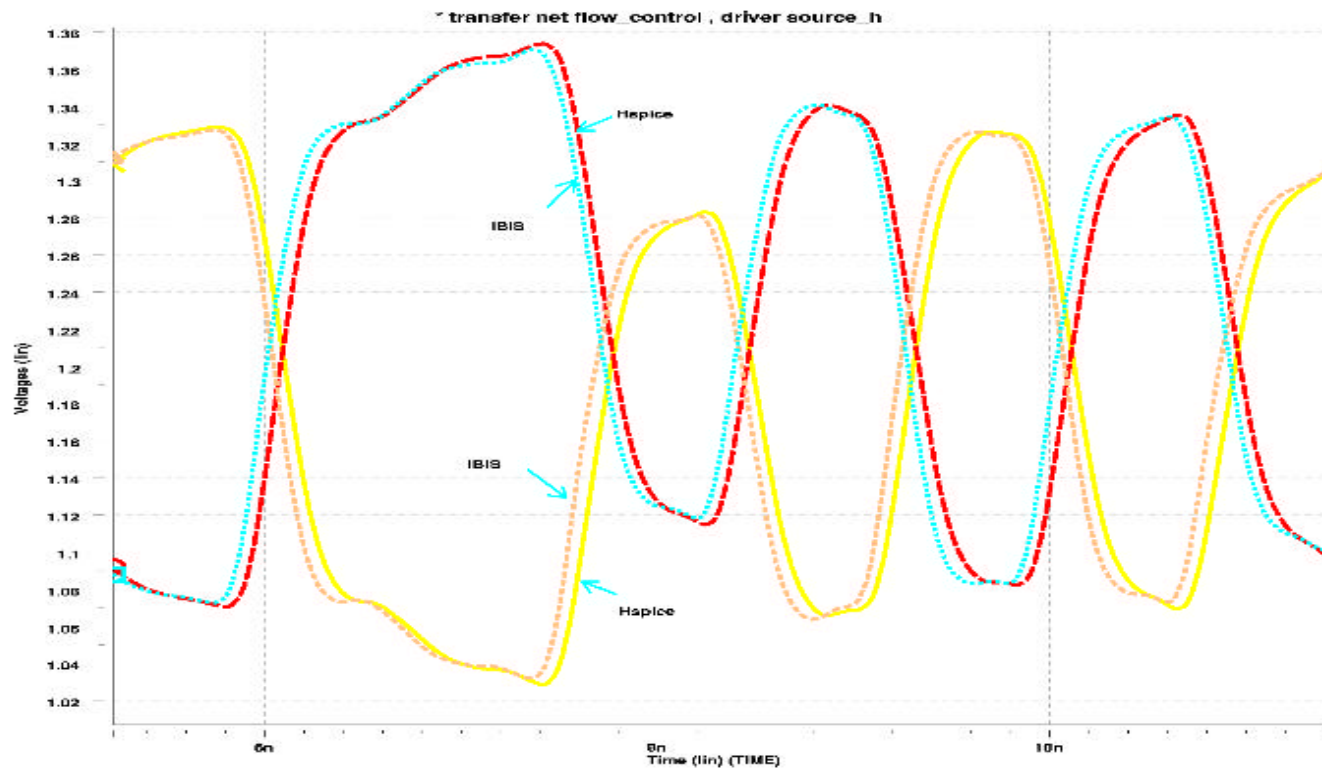




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SPICE versus IBIS

Accurate LVDS IBIS Model @ 1.25GHz



SPI4 interface: 1.25GHz, target pad, VDDQ=2.375

SPICE versus IBIS

- Why SPICE ?
- Why IBIS ?
- Why BOTH?

Why SPICE?

- Advantages
 - Industry Standard
 - Berkley SPICE is Free
 - HSPICE has widespread acceptance
 - Accurate
 - Transistor level models
 - Connectors, WLINE's – Lossy transmission lines
 - Rail collapse, ground bounce
 - Return path
 - If you can build it, you can model it
- Disadvantages
 - Performance can be slow
 - Inconsistent net list formats and cryptic spice syntax

Why IBIS?

- Advantages
 - Fast
 - Easy
 - Doesn't reveal proprietary information
 - Complete chip definition
 - Pin out
 - Cell Usage
 - AC and DC specifications
- Disadvantages
 - IBIS model quality is generally poor
 - Accuracy can be an issue
 - Practical Issues and Limitations
 - Connectors/package models
 - Intrinsic cell delay characteristics
 - Different results from different simulators (portability)
 - IBIS committee slow to respond

Need both SPICE and IBIS

- I'm not the only one who thinks so
 - Best of Both Worlds
 - **Mixed-signal HDLs put IBIS on steroids** (Glenn Perry [ee_design](#) 9/12/02)
 - Will Hobbs (Intel - Oct 98) said:
 - We Need to find a happy coexistence between structural and behavioral.
 - We need to keep pushing IBIS to meet emerging needs
 - Many others...
- If only we had it now (some of us do :-)

Conclusions

- High quality accurate IBIS models can be created
 - Hard work in most cases
 - Sometimes unachievable
 - Often, model has limitations
- We need SPICE and IBIS
 - Best of both worlds
- IBIS open forum must meet emerging needs

