Multi-Element C_comp Modeling

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IBIS Summit
PCB East 2004
October 4, 2004

Desktop Platforms GROUP

Agenda

- **Background**
  - Recall C_comp "Back Out" Experiments
  - Transient Matching
  - AC Differential- and Common-mode Behaviors
- **Creating a Better AC Model for C_comp**
  - Simulation Data in AC Domain
  - The Giacotto-Muranyi Model
  - Improvements on the G-M Model
  - Analytic vs. EDA Tool Solutions
  - Results
  - Applying G-M Models to the Differential Case
  - Next Steps

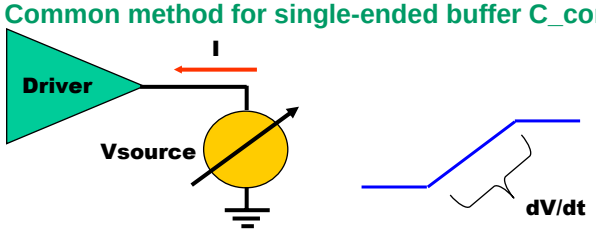
Note: many slides in this presentation are animated

Desktop Platforms GROUP

from April '04 Summit

How is C_comp data collected?

- Common method for single-ended buffer C_comp



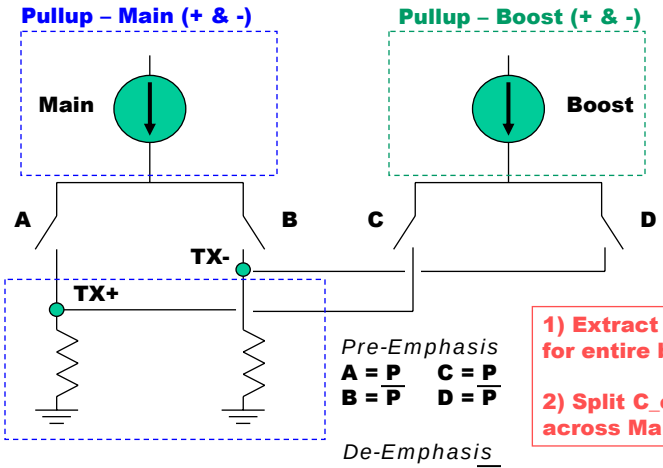
1. Use Vsource with known edge rate, dV/dt
2. Measure the input current
3. Calculate capacitance (may have to take an average)

$$I = C * \frac{dV}{dt} \quad \rightarrow \quad C = \frac{I}{(\frac{dV}{dt})}$$

What about for the differential case?
How about pre-emphasis (wired-or structures)?

from April '04 Summit

IBIS for SerDes Pre-Emphasis



Pre-Emphasis
A = P C = P
B = $\overline{P}$ D = $\overline{P}$

De-Emphasis
A = P C = $\overline{P}$
B = $\overline{P}$ D = P

Ground Clamps
Main + & -

1) Extract C_comp for entire buffer

2) Split C_comp across Main, Boost

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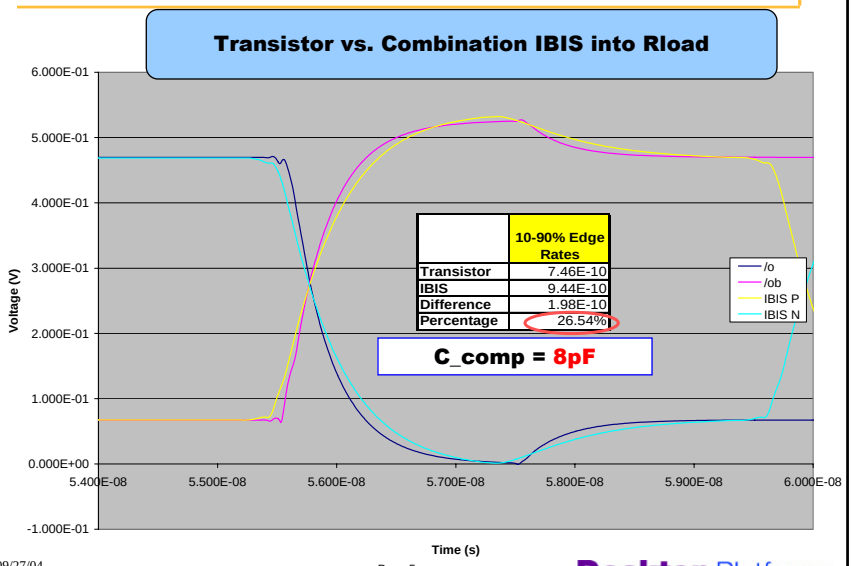
Results of First Attempt

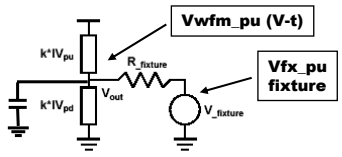


	10-90% Edge Rates
Transistor	7.46E-10
IBIS	9.44E-10
Difference	1.98E-10
Percentage	26.54%

from April '04 Summit

Proposed Fix

- Method 2: Adjust all V-t curves for the total C_comp value before using the models for simulation
  - *Each V-t curve reflects total C_comp load*
  - *Adjust each curve (Main, Boost) for total C_comp*
  - *Set IBIS C_comp for Main, Boost to 0 pF*
  - *Add external cap equal to original total C_comp*



Current through fixture is function of current through pullup AND through die cap

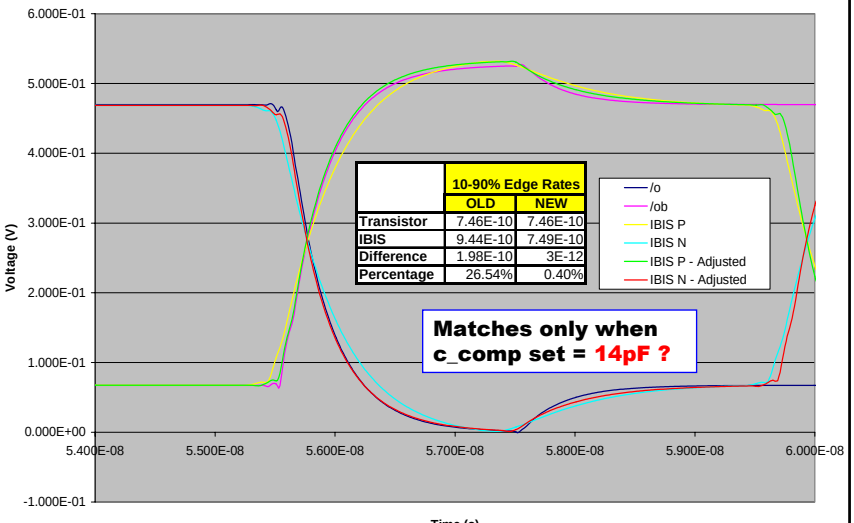
```
Ifx1 := ((Vwfm_pu(index) - Vfx_pu) / Rfx_pu) + C_comp * dVwfm_pu(index);
Ifx2 := ((Vfx_pd - Vwfm_pd(index)) / Rfx_pd) - C_comp * dVwfm_pd(index);
```

C_comp compensation

images and equations from A. Muranyi

from April '04 Summit

Results of Using New Method



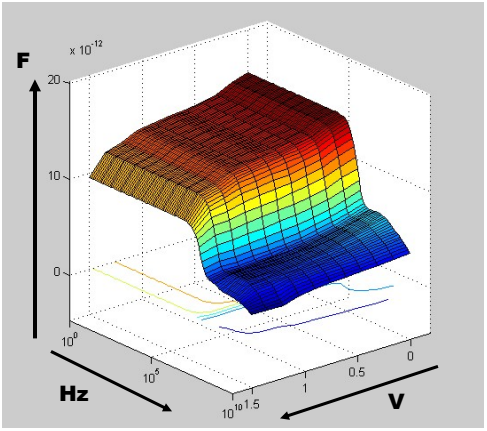
	10-90% Edge Rates	
	OLD	NEW
Transistor	7.46E-10	7.46E-10
IBIS	9.44E-10	7.49E-10
Difference	1.98E-10	3E-12
Percentage	26.54%	0.40%

Matches only when c_comp set = 14pF ?

from April '04 Summit

A Further Complication

- Transistor model capacitance behaviors are not simple
  - Capacitance varies with frequency and bias V
  - Frequency-based measurement result is *not* a constant



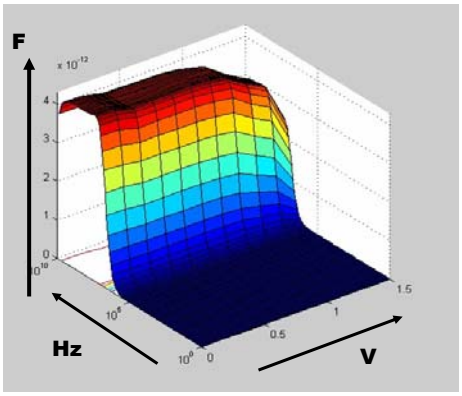
Recall A. Muranyi's analyses:
"Details on True Differential Buffer Characterization Revisited"
October, 2003

Single-ended capacitance of our "8 pF" buffer vs. V & F

from April '04 Summit

A Further Complication

- Differential view of transistor model capacitance
  - Differential capacitance not included in adjusted model
  - Note that finding of femto-farad differential capacitances described in previous summits may not always apply!



Recall A. Muranyi's analyses:
"Details on True Differential Buffer Characterization Revisited"
October, 2003

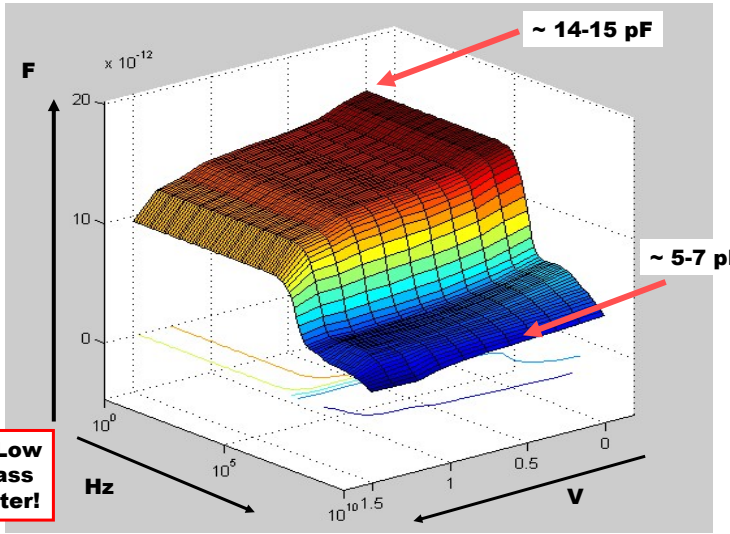
Differential capacitance of our "8 pF" buffer vs. V & F

Another New Approach

- First C_comp adjustment attempt made two assumptions
  - *Differential buffers can be "split" in two*
  - *Each can be modeled adequately with a single C_comp*
- Additional data calls at least one assumption into question
  - Single C_comp does not permit frequency dependence
  - A differential component appears at some frequencies
- Proposal: Stay in AC Domain for C_comp Measurement
  - Attempt to match AC behavior of simulation model
  - Once model correlates in frequency of interest, add data into IBIS model
    - *This may stretch IBIS 3.2/4.0 beyond available keywords*

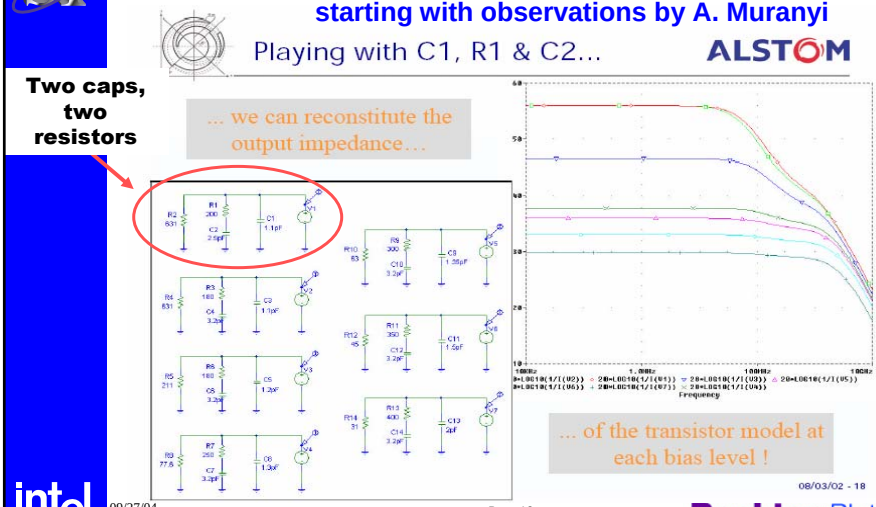
from April '04 Summit

Our Target Behavior



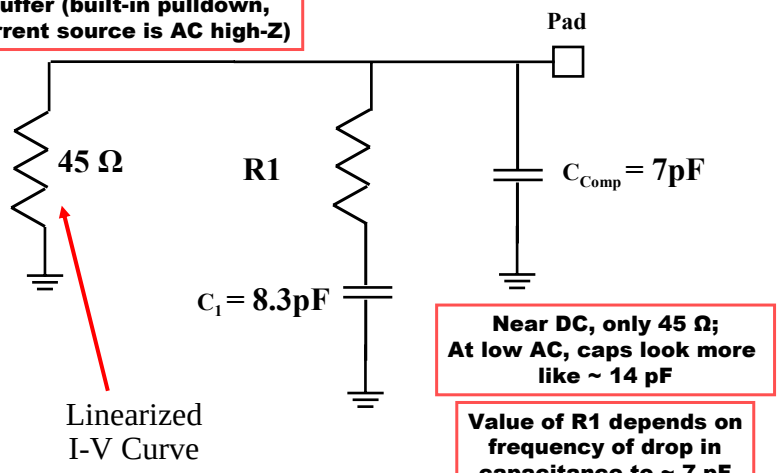
Recall L. Giacotto's Slides...

- 2002: Luca Giacotto presented twice on buffer impedance starting with observations by A. Muranyi



Original Giacotto-Muranyi C_comp Model

One side of our differential buffer (built-in pulldown, current source is AC high-Z)

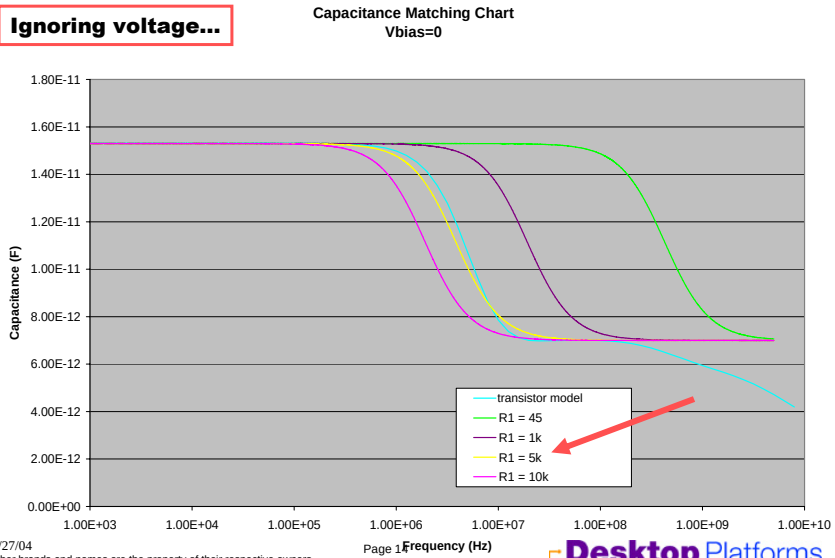


Near DC, only 45 Ω; At low AC, caps look more like ~ 14 pF

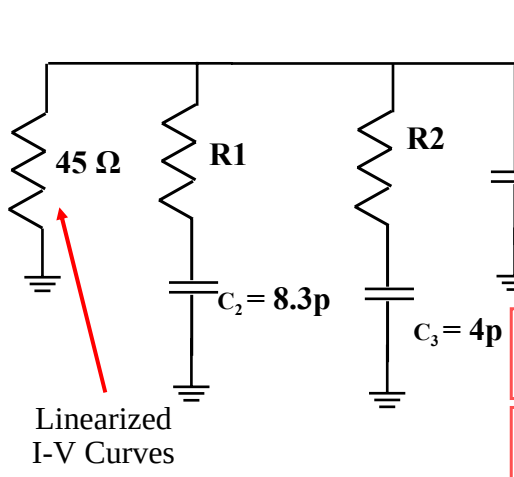
Value of R1 depends on frequency of drop in capacitance to ~ 7 pF

Model vs. AC Analysis of Buffer

Ignoring voltage...



Modified G-M Model

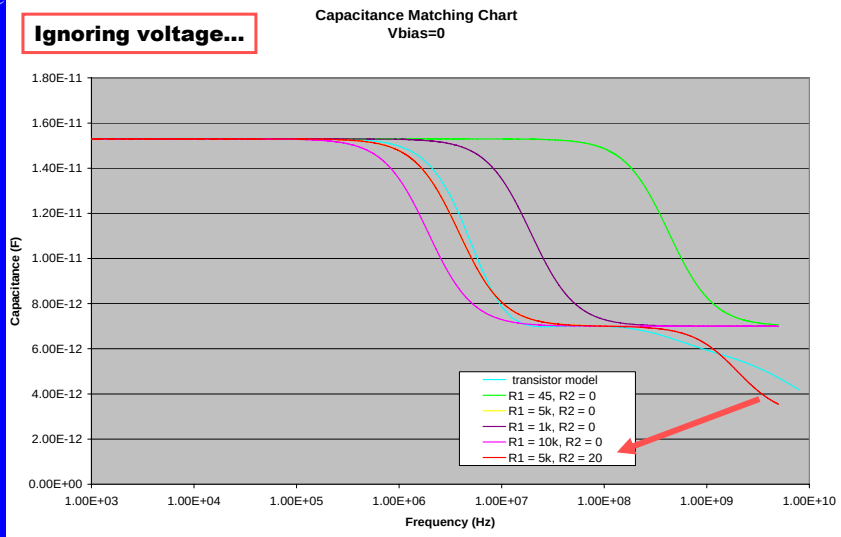


Near DC, only 45 Ω; At low AC, caps still add to ~ 14 pF

Adding new elements to cause new "break" in frequency

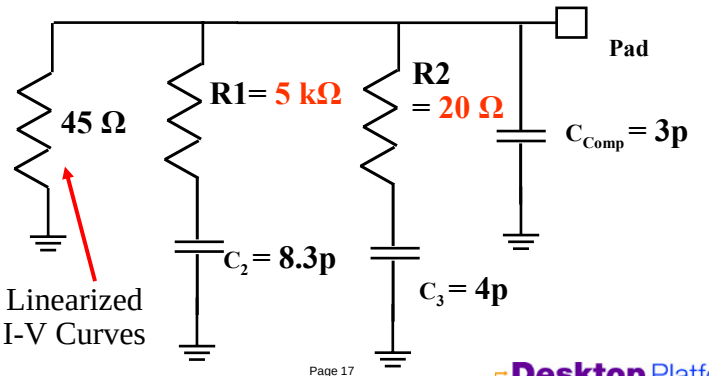
Modified Model AC Analysis

Ignoring voltage...



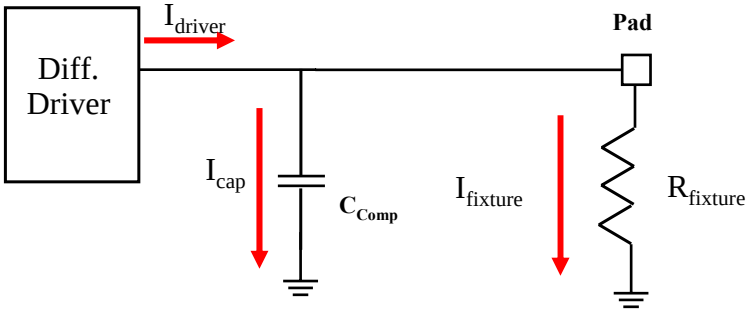
Model Assessment

- Model is a fair match up to ~ 2 GHz
- Problems arise
  - *A single C_comp value is no longer adequate*
  - *No IBIS keywords support this structure*
  - *Still need to "back out" these elements from V-t curves*



Original C_comp Adjustment

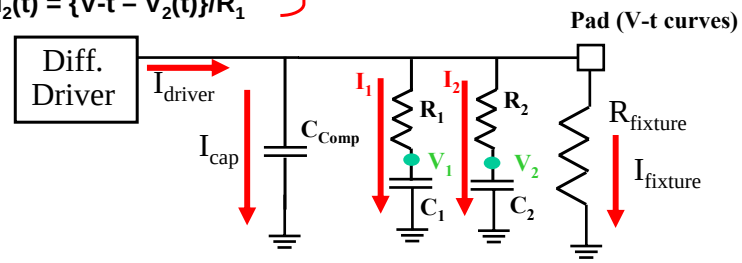
- $I_{driver}(t) = I_{cap}(t) + I_{fixture}(t)$
- I_{cap} = C_comp * dV/dt where dV/dt is instantaneous V-t slope
- $I_{fixture}$ = V-t/$R_{fixture}$, taken at every time point
- "Cap-less" V-t curve = $I_{driver}(t) * R_{fixture}$
  - Driver is pullup curve set with internal pulldowns
  - $V_{fixture}$ = 0, since there is no active, driving pulldown



Modified Approach

- $I_{driver}(t) = I_{cap}(t) + I_{fixture}(t) + I_1 + I_2$
- I_{cap} = C_comp * dV/dt where dV/dt is instant. slope of V-t
- $I_{fixture}$ = V-t/$R_{fixture}$, taken at every time point
- "Cap-less" V-t curve = $I_{driver}(t) * R_{fixture}$
- $I_1(t) = C_1 * dV_1/dt$
- $I_1(t) = \{V-t - V_1(t)\}/R_1$
- $I_2(t) = C_2 * dV_2/dt$
- $I_2(t) = \{V-t - V_2(t)\}/R_1$

But we don't know V or I!!!

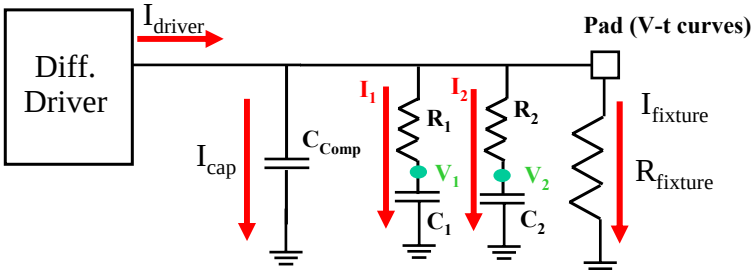


Modified Approach (2)

- Yes, we do know…
- RC charge equation is $V_1 = V_i + Ae^{-t/RC}$
  - see Horowitz and Hill, *The Art of Electronics*, Chapter 1
- For arbitrary V_i (t), this becomes

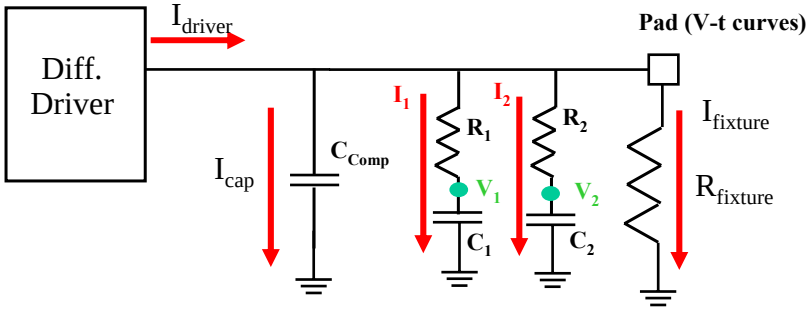
$$V(t) = \frac{1}{RC}\int_{-\infty}^{t} Vi(\tau)e^{-(t-\tau)/RC}d\tau$$

- If $I_1(t) = C_1 * dV_1/dt$…

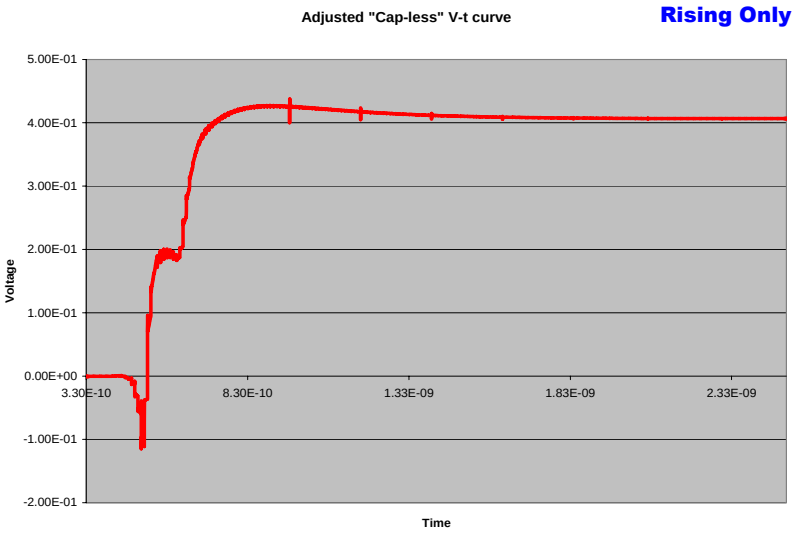


Modified Approach (3)

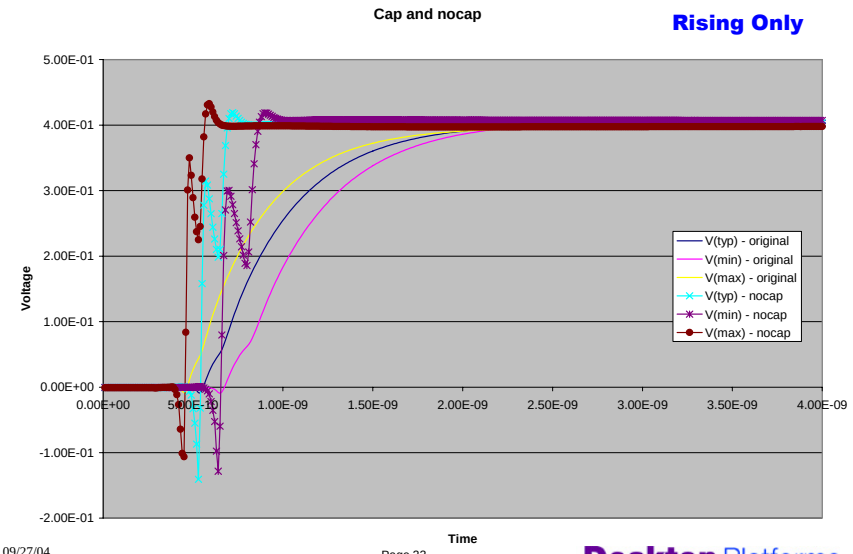
- Very tricky differential equation…
- Easier solution – use EDA tool to generate data!
  - Create netlist as shown
  - Drive PWL source with original V-t data set(s), at pad
  - CCCS into load = Rfixture provides "adjusted" V-t curves



New "Cap-less" Main V-t Table

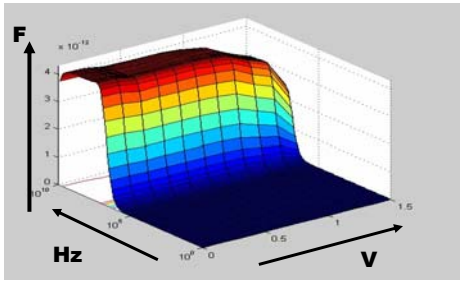


Original V-t and First Adjust…



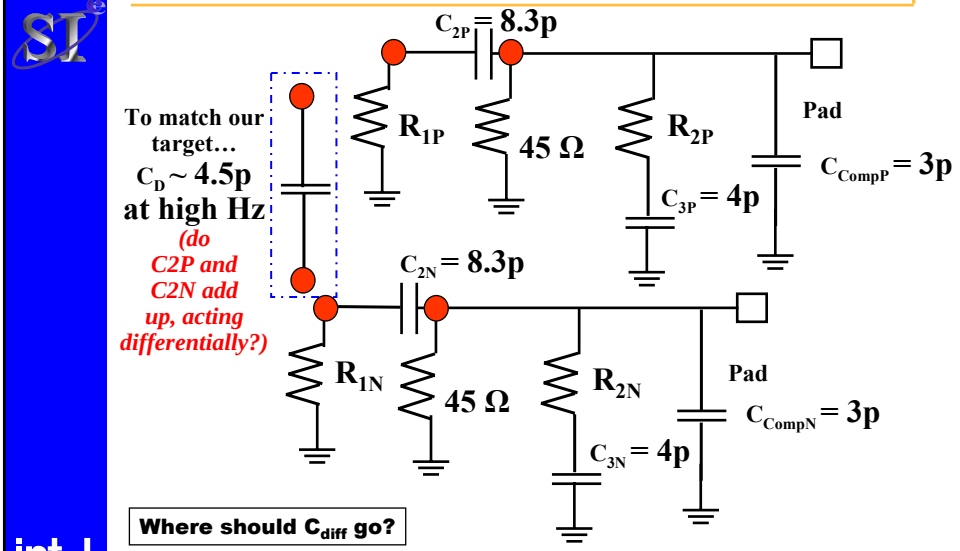
Assessment

- We can now adjust V-t curves for AC C_comp
  - *Enabling each portion of differential buffer…*
  - *Take a separate V-t curve (Main Only, Boost only)*
  - *Take AC domain frequency response for entire buffer*
    - ***Single-ended response only analyzed so far***
  - *Match AC domain with model & extract adjusted V-t curve*
- Can we repeat the process for differential behavior?



A High Pass Filter!

What about differential C_comp?



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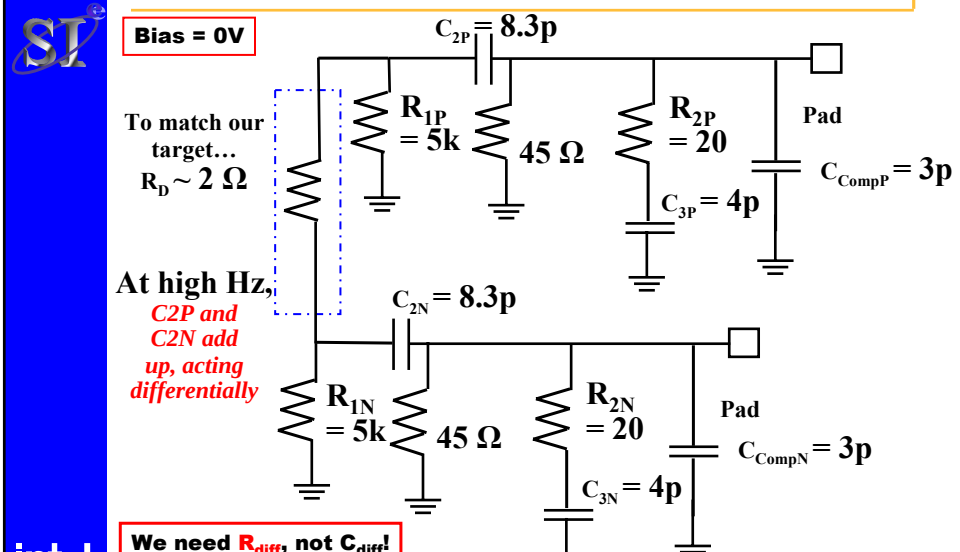
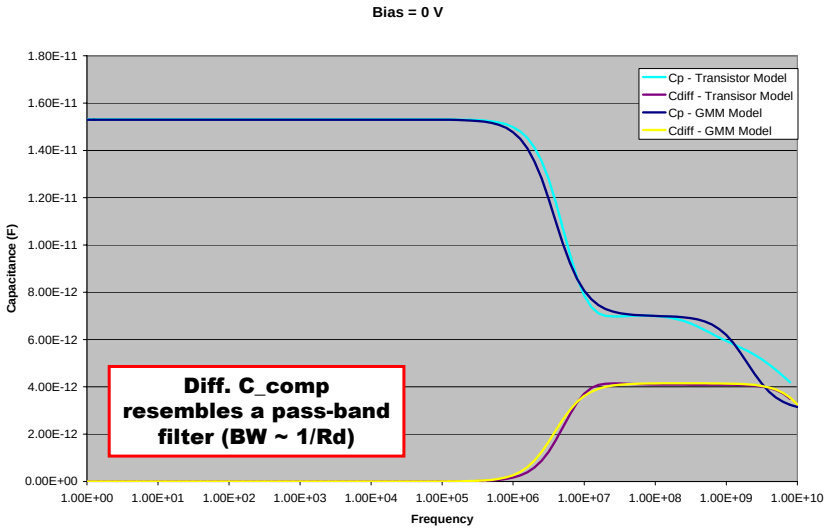
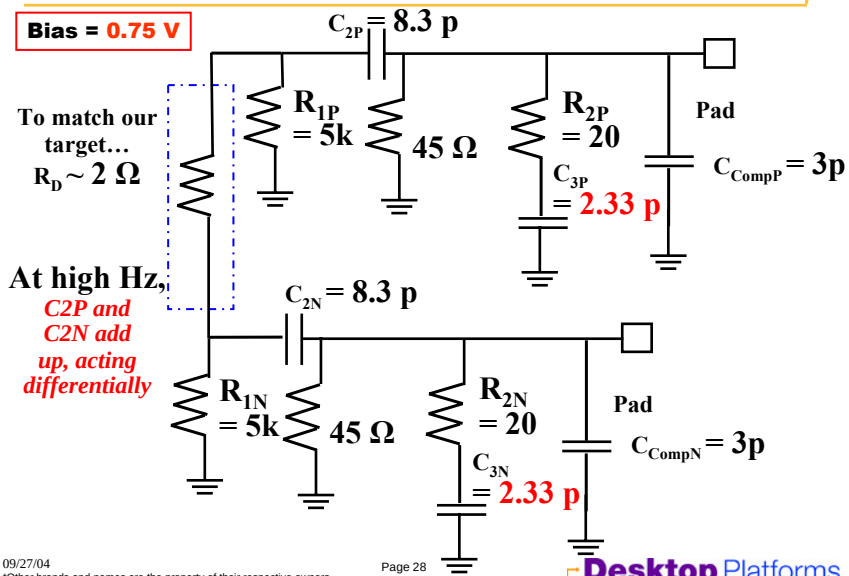


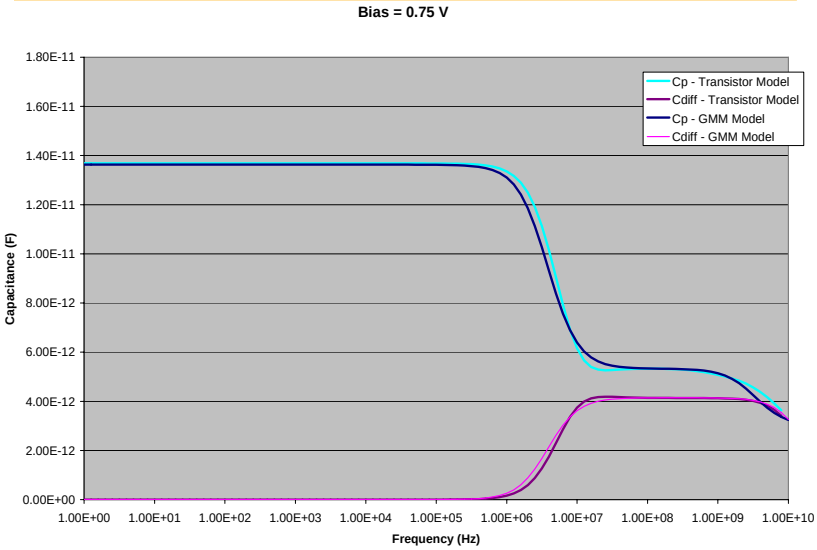
Differential C_comp (Bias = 0 V)



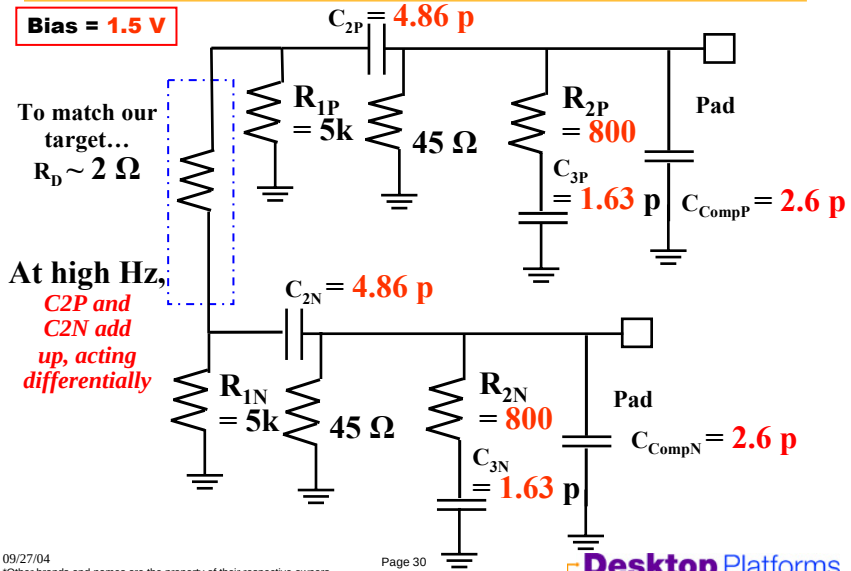
What about differential C_comp?



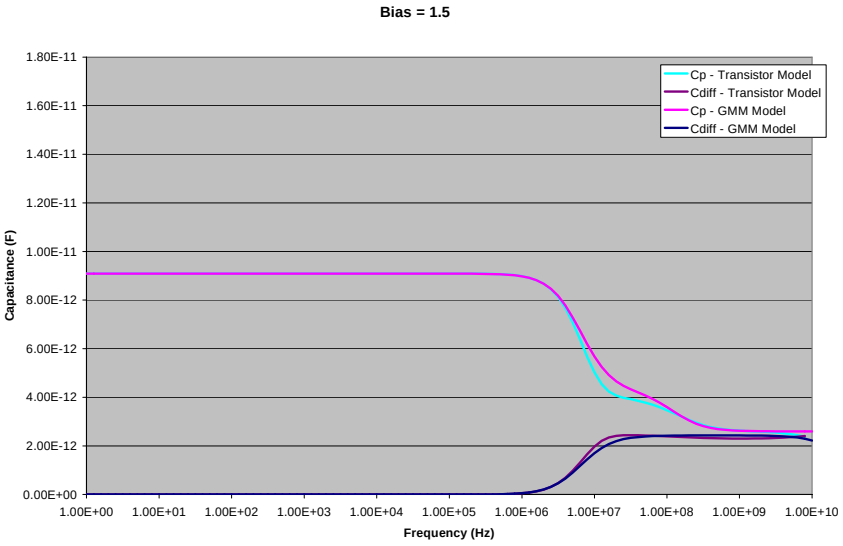
Diff. C_comp (Bias = 0.75 V)



What about differential C_comp?



Diff. C_comp (Bias = 1.5 V)



Summary and Next Steps

- A new method for adjusting V-t curves is shown
  - *Based on frequency-domain capacitance profile*
  - *Fit to a circuit expanded from Giacotto-Muranyi model*
  - *Covers both differential and single-ended AC behavior*
- Comments and Next Steps
  - *Method is untested in system simulation!*
    - EDA tool method (CCCS) does not generate clean V-t data
    - Local IBIS creation tools will choke on “noise” in V-t data
  - *Need analytic method of model value fit*
    - Values here determined using trial-and-error; fit isn’t great
    - Giacotto proposed pole-zero analysis
    - No luck in getting PZ to generate matching RC values
    - Will all models have the same RC model profile?
  - *Need to incorporate more voltage bias data*
  - *Need a recommendation for model bandwidth*

BACKUP

Single-ended C_comp – Alternate View