A Proposal for Developing S2IBISv3

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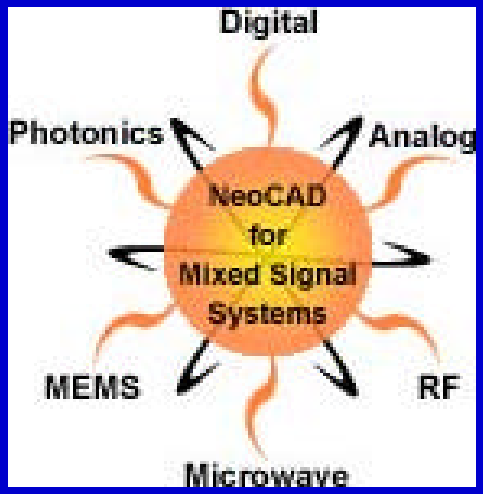
NC STATE UNIVERSITY

Automated Design Tools for Integrated Mixed Signal Microsystems (NeoCAD)



Outline

- Background
- DARPA Program “NeoCad”
  - Program Objectives
  - Program Approach
- Support for IBIS Community
  - Detailed Technical Approach
  - Future Planning Support
- Timeline and Feedback
- Conclusions

Background

- ARMM Group
  - Analog, RF and Mixed Mode
  - Strong industry connections and support
  - Large base of Federal Funding
- Proud of previous contributions to IBIS Community

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DARPA project … Big Picture

Implementation of advanced modeling and simulation abstractions, fast linear and nonlinear solvers, full-wave EM modeling for on-chip parasitics and integrated RF/microwave circuit design and modeling, digital and analog behavioral modeling, optoelectronic modeling and electrothermal modeling.

Plans and Team

DIGITAL BEHAVIORAL MODELING AND SSN MACROMODELING

Paul Franzon NC STATE UNIVERSITY

GLOBAL ENVIRONMENT NC STATE UNIVERSITY

Michael Steer, PI

PARASITIC EXTRACTION AND FULL WAVE MODELING OF INTERCONNECT

Andreas Cangellaris University of Illinois Urban Champaign

OPTOELECTRONIC MODELING

Mark Neifeld The University of Arizona

Impact: **A mixed-signal modeling capability that incorporates full-wave (EM) modeling of on-chip interconnects linked into a robust global simulation environment that provides a universal simulation environment for modeling.**

Development of physical device models and optoelectronic device models linked into global simulation environment.

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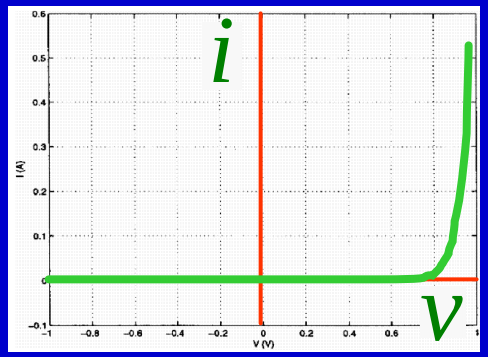
TRANSIM

Unique Feature:

Nonlinear devices models based on state variables:

- This provides great flexibility for the design of new models. All of the analyses are state-variable-based, including a time marching analysis (different integration methods available) and a unique wavelet transient analysis.
- The state variables can be chosen to achieve robust numerical characteristics.
- The calculation of derivatives are free of truncation errors at a small multiple of the run time required to evaluate the original function with little additional memory required. (ADOLC)

CONVENTIONAL DIODE MODEL



STRONG NONLINEARITY

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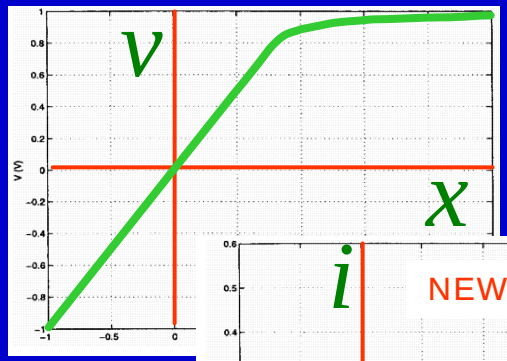
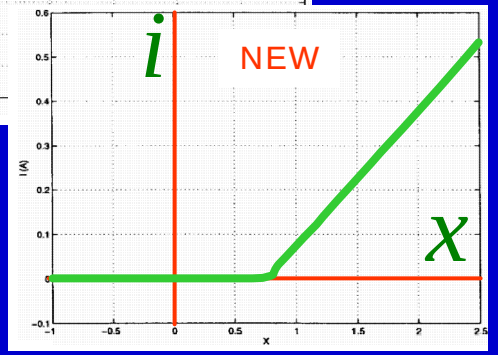


NEW

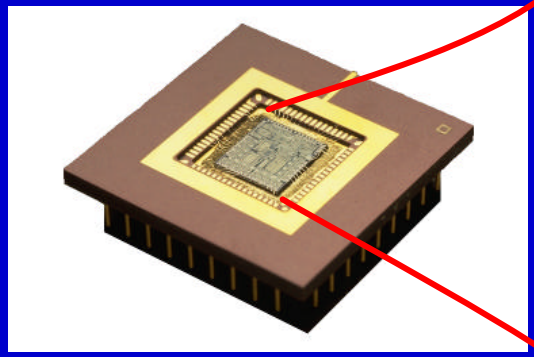
+

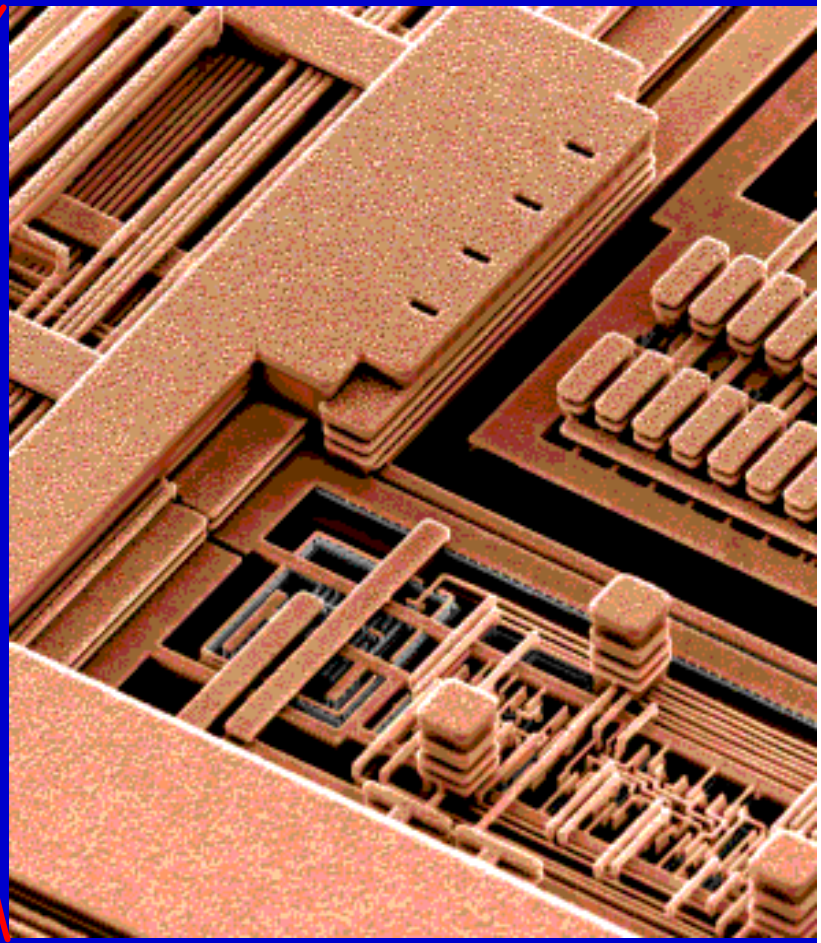


MODERATE NONLINEARITY

Parasitic and Interconnect Modeling

Mixed Signal Chips And Systems





Model using

(a) Capacitance Extraction ?

(b) + Inductance Extraction ?

(c) Transmission Lines ?

(d) Full-Wave (full EM Modeling) ✓

Technical Approach

PARASITIC EXTRACTION AND FULL WAVE MODELING OF INTERCONNECT

Approach and Issues:

Full-wave interconnect parasitic extraction.

Global surface impedance models capturing frequency-dependent field penetration inside conductors of arbitrary cross section.

Closed-form Green's functions for the rapid calculation of interactions between electric charges and currents in multi-layered, lossy dielectrics. Planar, layered dielectrics need not be discretized.

Adaptive integral method (AIM)-based solvers, for the rapid iterative solution of interconnections in multi-layered substrates.

Unique Features:

Accurate capture of the broadband nature of the electromagnetic interactions, and thus account for all frequency dependencies in the interconnect medium that impact signal distortion, noise generation and coupling.

Technical Approach

ON-CHIP DIGITAL BEHAVIORAL MODELING AND SSN MACROMODELING

Approach and Issues

Macromodeling tool for automatic accurate reduced-order SSN modeling of on-chip digital structures from full circuit description.

Unique Features

A macromodel production tool (similar to Spice2IBIS); Complete SSN macromodel conversion tool.

Extracts of Requirements of S2IBIS3 Issued by IBIS sub-committee

Outline

- Scope of the Project
- General Requirements
- Specific Requirements
- Documentation
- Acceptance Criteria

Scope of S2IBIS3 Project

Generate a user-friendly IBISv3.2 compliant SPICE-to-IBIS translator runs on multiple OS platforms and be easily up-gradable to meet the requirements of future IBIS standards

OS Platform Independence

- Should support LINUX, AIX, HP, Windows 2000 among other platforms using a single Makefile

  (Code will be developed in the gnu environment. The same makefile can be used on 26 known operating systems with no code changes.)
- We will use C++, for coding and JAVA for graphics.
- Should be portable (Though it is mentioned that LEX/YACC should be avoided, We will use FLEX/BISON and achieve portability through GNU environment and Cygwin in MS Windows.)

Hooks to other SPICE Engines

- Testing S2IBIS3 on BerkeleySPICE2G.6, SPICE3 and HSPICE
- Should have hooks to SPICE2G.6, SPICE3 and commercial SPICE simulators through configuration files
- Use of SpiTranGUI (JAVA based freeware from Cadence) and possible incorporation into S2IBIS3

Other Features

- Graphical viewer to plot VI and VT tables
  (We plan to do it in JAVA)
- Parser Integration for automatic validation of the output IBIS files
- Project Manager for file and library maintenance

Specific Requirements

- Flexibility to extrapolate VI data
- Flexibility to define the sweep range for VI tables
- Rectification of clamp problem in S2IBIS2
- Option of Ramping up Vdd (rather than single step)
- Implementation of .OPTIONS feature supported by SPICE compatible simulators for non-convergence issues

…Requirements

- Debug through GUI control
- [Iterate] feature in S2IBIS2 to be carried over
- User selectable Voltage step, Time step, Sweep speed support
- User selectable number of data points, decimal accuracy
- Choice of choosing between the TYP, MIN and MAX instead of all process corners

Features

- Correction algorithm to avoid double counting for buffers with on-die termination
- Cross-checking VT curves against VI curve-load line intersection and subsequent correction
- Guardbanding feature for VI and VT curves
- Intelligent pin list to avoid repetition of equivalent models

Documentation

- README File with Contents of the package and Installation instructions
- User guide with Contents, Algorithms and Tutorials
- Code explanation with Flow chart of the project

NCSU Goals

- GNU Public License
- C++ (Platform Independent using GNU, Cygwin)
- Class Structure to support Digital and Analog Macromodeling -IBIS is a subset
- Applicable to Board level modeling and modeling of segments of Mixed Signal Chips

Programming Technology

S2IBIS 2	S2IBIS 3
•No Graphics	• Graphics in JAVA
•Originally not portable	•Portable through GNU environment(Cygwin in MSWindows)
•C Data Structures	•C++ Classes
•LEX/YACC Input/Output	•LEX/YACC Input/Output

Research Agenda

- Support for IBIS-X (IBIS-X + 1?)
  - Provide SSN macromodelling
  - Investigate 3-D models
  - Test accuracy against full-fidelity simulations and measurements

Validation

- Against Spice
- Against Measurement
- Industrial Collaborators

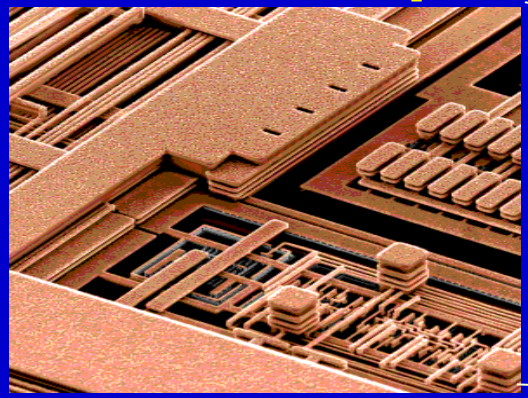
Conclusion

- 3-year DARPA effort
  - Full fidelity modeling
  - Digital macromodeling
  - Strong Industrial Emphasis
- Deliver Spice2Ibis3
- Investigate issues for IBIS-X (+1?)

Backup Slides

- …

Chip Macromodeling



IBIS INTERFACE

BEHAVIORAL MODEL

Full Chip Model

IBIS INTERFACE

BEHAVIORAL MODEL

IBIS

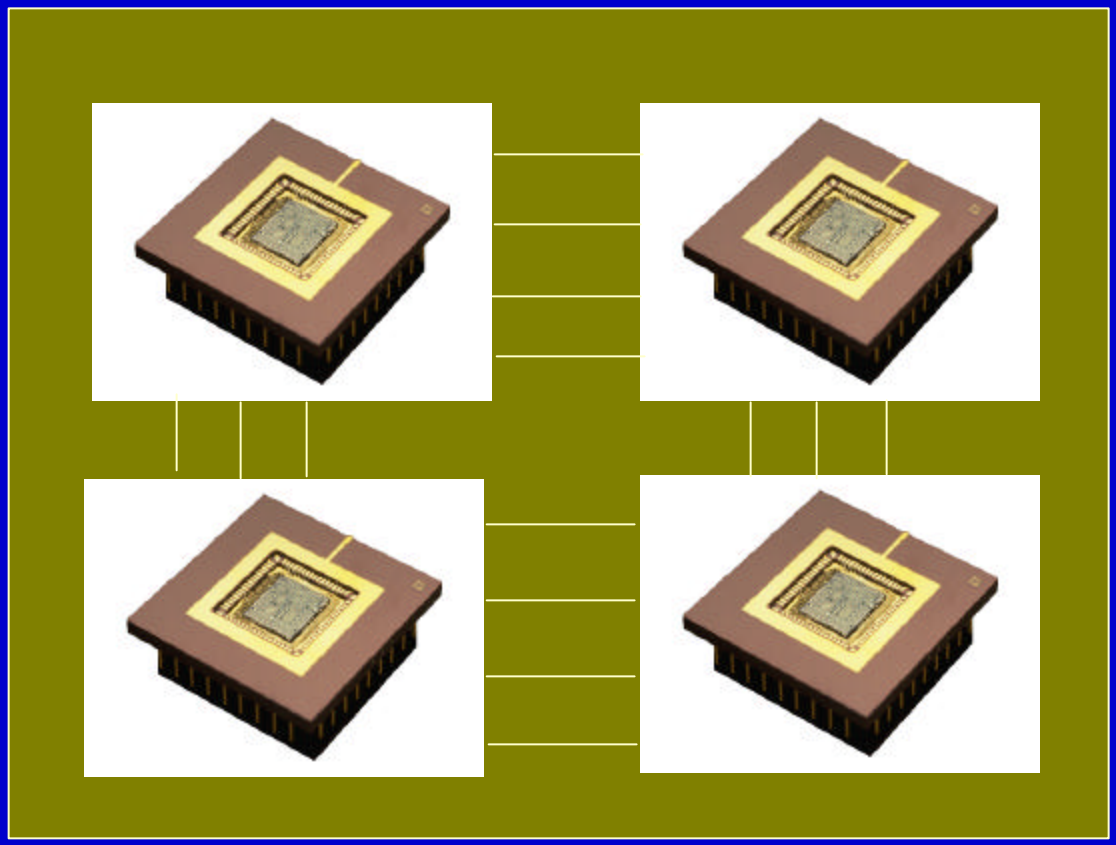
BEHAVIORAL MODEL

IBIS

BEHAVIORAL MODEL

CIRCUIT

IC'S On a PCB



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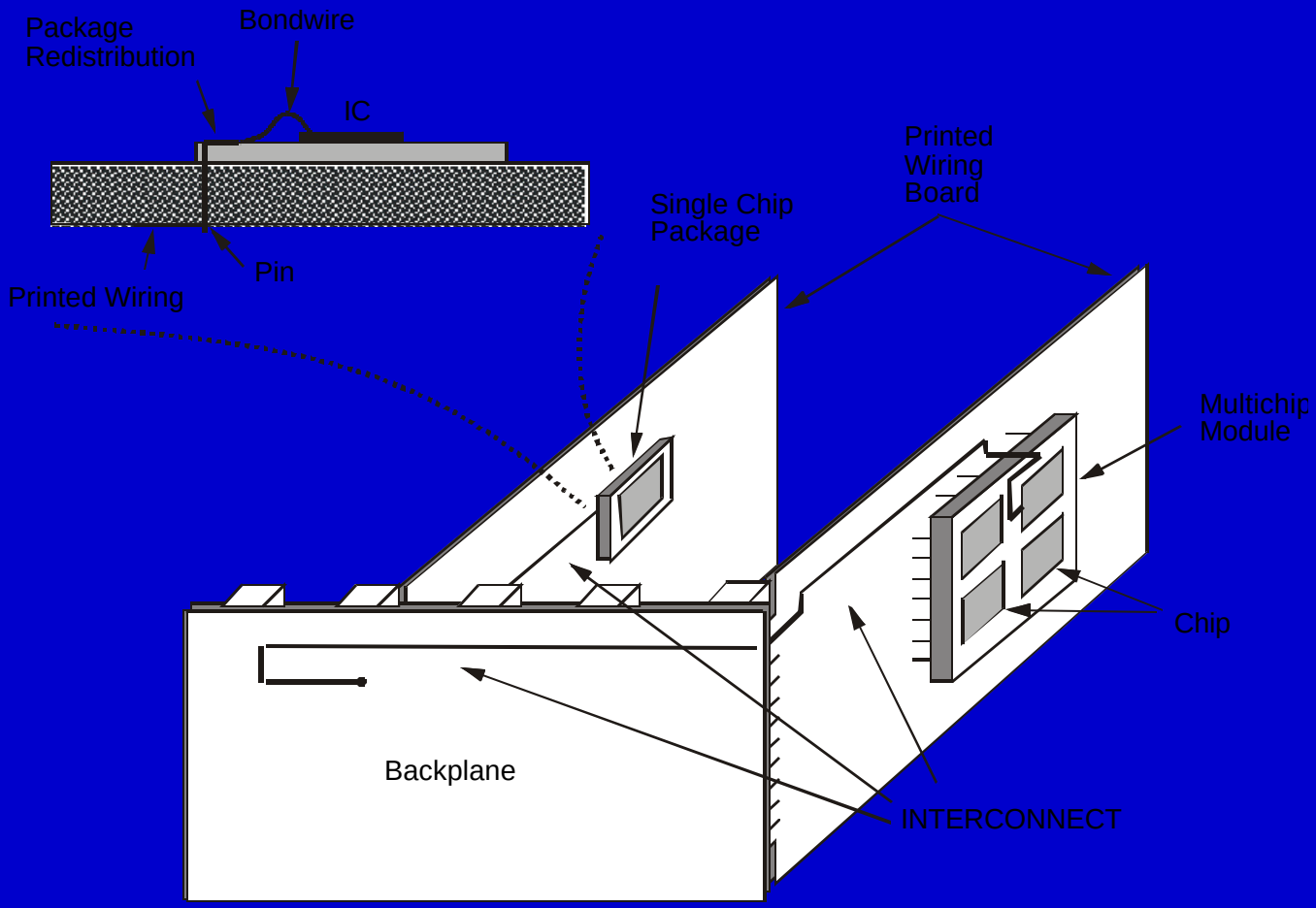
Package
Redistribution
Bondwire
IC
Pin
Printed Wiring
Single Chip
Package
Printed
Wiring
Board
Multichip
Module
Chip
Backplane
INTERCONNECT

gate (poly)
OUT (metal1)
NMOS
IN (metal1)
PMOS
nWell
VDD (metal1)
GND (metal1)

Board Level Modeling

- Development of a Digital Macromodeling technology to enable ICs to be incorporated in a PCB
- Signal Integrity should be taken care of as well
- Capture of SSN and Substrate noise