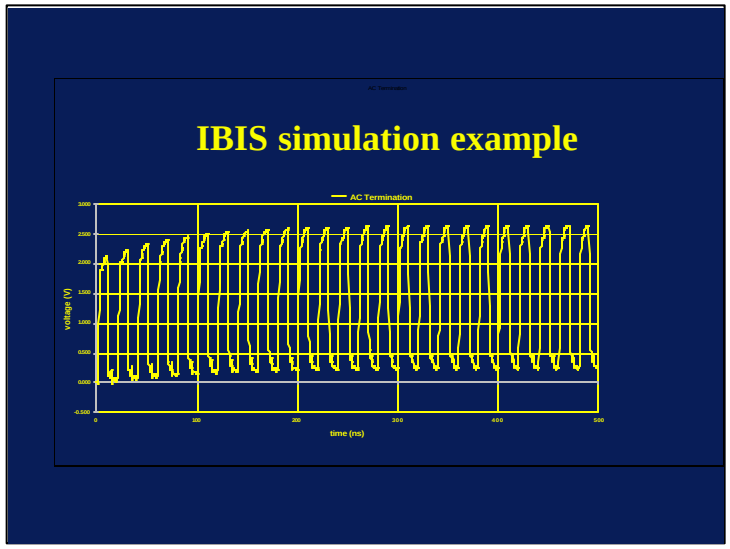
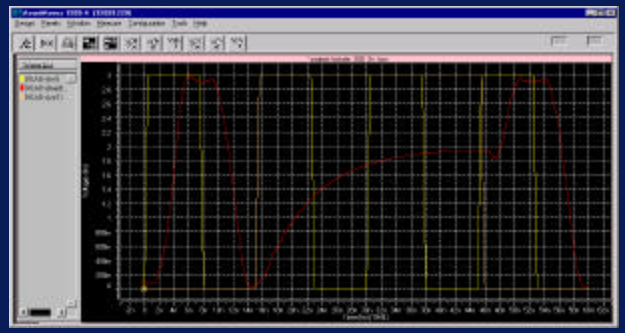
Anyone See this before ? In my brief time today I will give you my recent experiences as an IBIS user. This in sharp contrast to being a MODEL building, verifier and user. For those who don't know me I worked for a number of years as DEC ..err.. Compaq, err or is it now HP, and was the IBIS Open forum Primary contact. I contributed to the the IBIS accuracy Specification and time developing and verifying ACCURATE behavioral IBIS models. Now I find myself a consumer or "user" of models. Being at a startup, resources are tight and everything needs to be done fast but correctly. I am the SI group. This is also in sharp contrast to being a member of a team at a big company building, and verifying and using your own models. This presentation is intended to be interactive and provoke some discussion. Please Jump in at anytime. I wanted to start by briefly touching on the SPICE vs. IBIS issues which constantly comes up on the web reflectors.



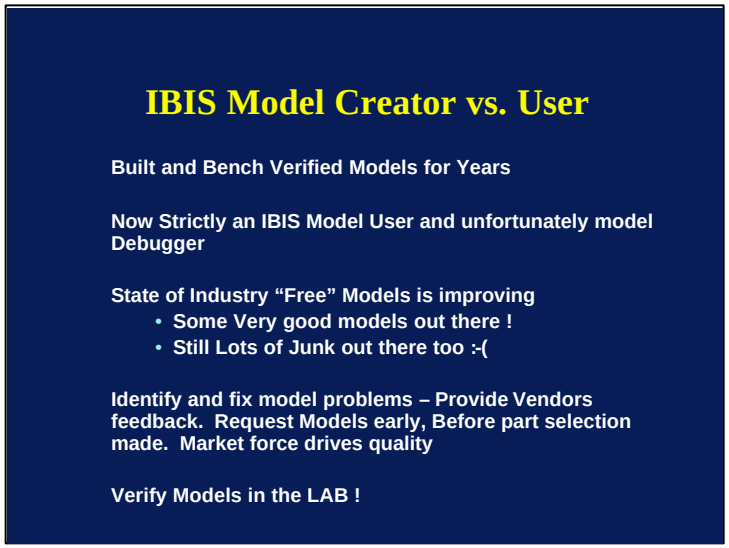
Here is a simple IBIS simulation example of a network utilizing AC termination. It is a point to point clock network with a driver, load and .01uf/50 ohm AC termination in the middle of the network. I have plotted the waveform at the input to the receiver (the load). This is an example of a case were the run time of an IBIS simulation is a big advantage over spice.I was able to quickly examine various termination values and quickly converge on a solution. I then bench tested the solution in the lab.

SPICE simulation example

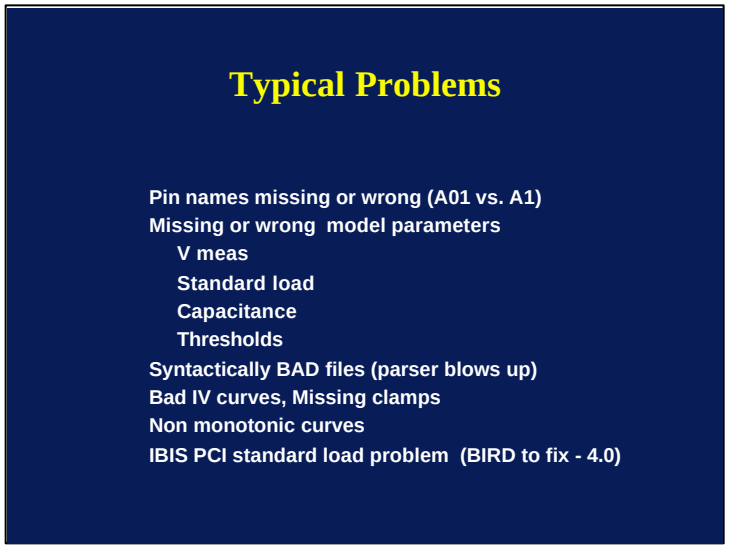


Here is a simulation that is difficult to perform using IBIS. It is a multi-drop bi-directional network with stiff DC termination. The simulation waveforms shows the input waveform, tri-state enable and the output. After the first cycle I tri-stated the output. These simulation results show that the bus is left in an illegal state which could potentially cause problems on the bus.

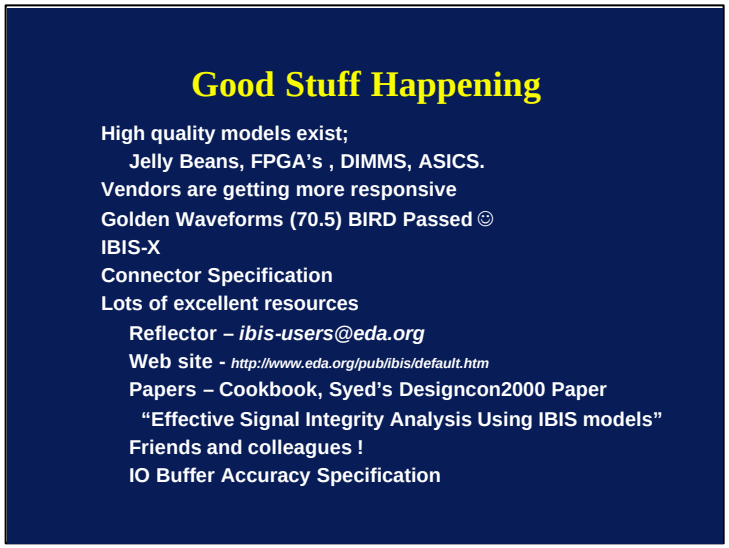
These examples would presented to illustrate why it is important to use Both IBIS and SPICE. Each has its respective advantages and disadvantages.



I can remember sitting on a panel at designcon98 were we discussed the problems with IBIS models today. After a few long winded exchanges on the merits of bench verification of models, it was clear that a lot of people were having trouble just getting models, or that they wouldn't even pass basic Golden Parser syntax checks. I will never Forget Bob Ross's classic statement of ONLY about 10 % of the models out there being good. I think vendors web sites have improved significantly. Bob do you have any estimates on % of good models out there now ☺. Today you can even buy bench verified models from some 3rd parties. There is a few things we can all do to help continue the improvement and availability of models; 1. Request a model when you Component engineer request samples and data sheets. Let them know that model creation is part of doing business.2. Feedback any and all problems to the model creator. Don't just fix the problem. Let the vendors know you're using the model and you expect quality. I don't know if the percentages have changed much, but there are a lot of good models. It takes due diligence to find and verify them..



This is not an all inclusive list, but just intended to be a short list of problems I stumble across every day. Just getting “IBIS models” is sometimes a challenge. Recently I have asked for IBIS models and received Verilog models. Another day I asked for SPICE models, went through a huge delay, NDA all sorts of rigmarole and finally received an IBIS model that did not work.. I was told, there was an update and received the same model, with only the date changed. A few very common problems are pin numbers begin wrong, or missing, missing Vmeas data. Some problems are relatively easy to fix, although sometimes time consuming. Syntax problems is an example. Other problems are much more difficult, like BAD IV curves, missing clamps. It is up to all of us to work with the semiconductor vendors and model creators to improve the quality. I use to focus on bench verifying models to insure accuracy. I realize there is another hole realm of problems out there. But all is not bleak .



Even though there are lots of problems, there are a lot of people working on solutions.

Golden waveform BIRD is an attempt to facilitate documenting the the long hard IBIS accuracy specification path we traveled. All of the other activities are also excellent ways to move forward. The Semiconductor vendors are listening. They are attempting to create better models and it shows. There are a ton of excellent resources. And being an SI island I need help too. Some of the best resources are the colleagues sitting around the room . I have found everyone to be extremely cooperative and have tried to do my best to help too. The Models are getting better But still USER beware ! Thank you for your attention.