Power/Gnd Simulation Using IBIS Models and Pin Mapping Issues

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Outline

- Motivation – automated Power/Gnd simulation
- Example of Power/Gnd simulation and effect of decaps
- Examples of package pin layouts
- How pin mapping helps automation
- Suggestion for IBIS models to improve automation

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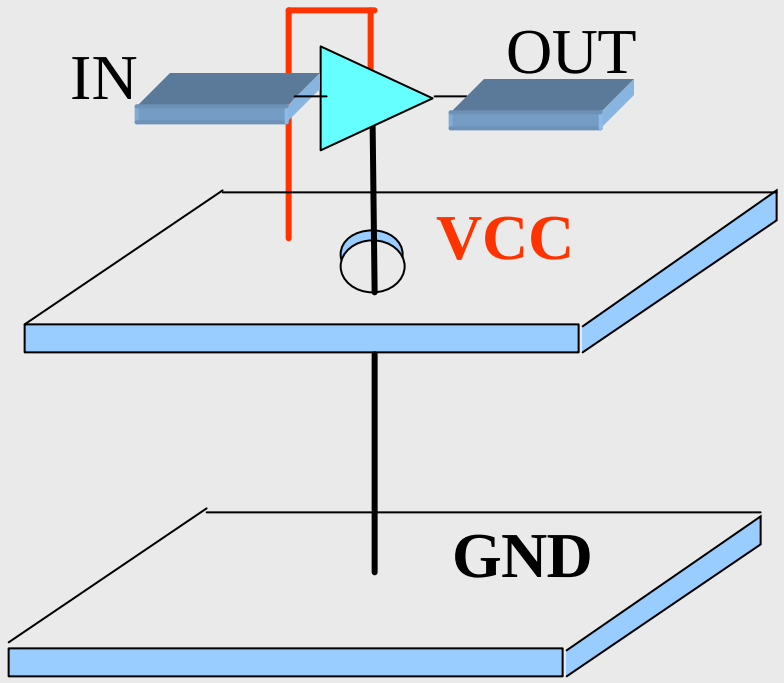
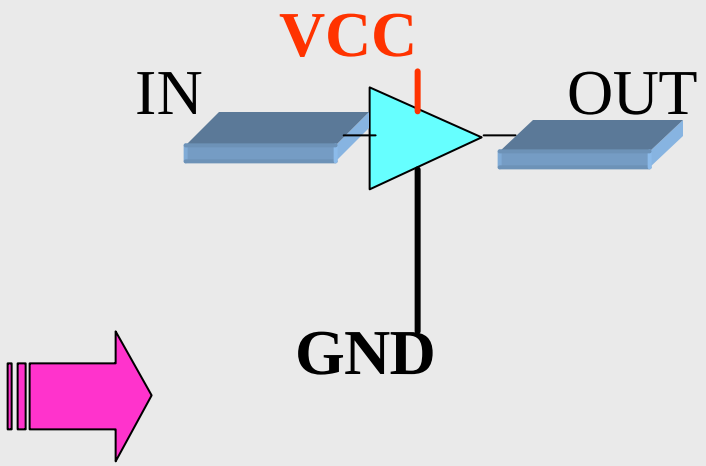
Simulation Assuming Ideal Power/Gnd Planes





There is no need to know which GND and VCC pins of package drivers and receivers are connected to

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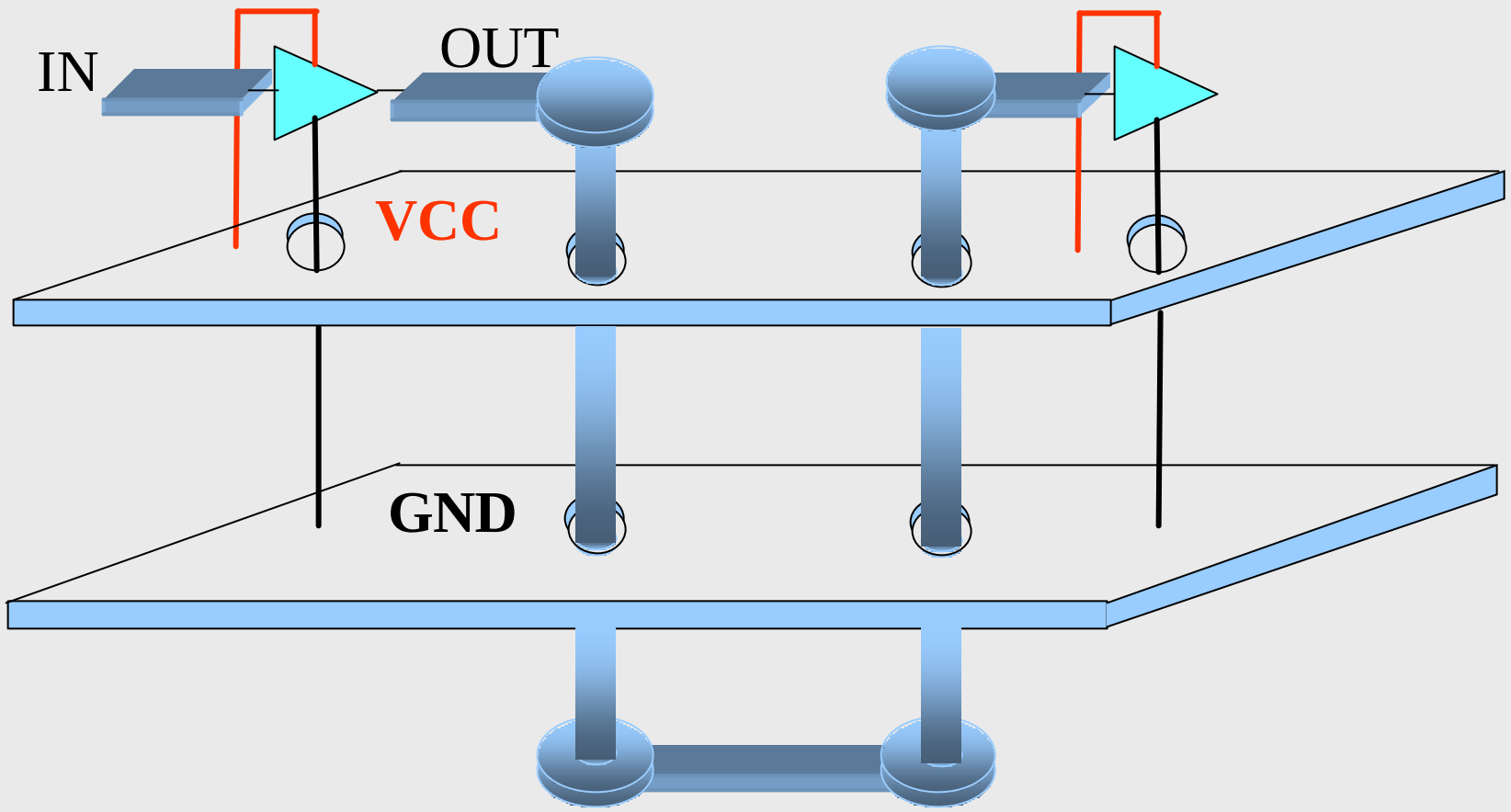
Time Domain Simulation with Power/Gnd Structure in Place



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Difference between Conventional SI Solution and Solution that takes Power/Gnd Fluctuations into Account

Conventional SI does ***circuit + transmission line + pin RLC simulation*** assuming ideal ground and power planes

Advance SI/PI solution does a combined ***circuit + transmission line + (pin RLC) + nonideal ground and power plane simulation***.

Can take care of

- Power ground noise i.e. SSN or Delta-I or ground bounce
- Effects of vias and return path discontinuity can be modeled
- Effect of decoupling caps can be considered
- Edge radiation from boards due to SSN can be calculated

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Use of IBIS Models in PWR/GND Analysis

In conventional SI simulation, directly simulating IBIS models eliminates the process of making models separately. Same can be true of PWR/GND analysis or Power Integrity

Two approaches to model pwr/gnd

Separately model pwr/gnd (maybe in frequency domain) and later do time domain simulation. Less automated, smaller structures and difficult to interface to layout

At Sigrity, we do a combined circuit/transmission line/power/gnd simulation with IBIS models in time domain. This can be directly done from layout, especially if IBIS models are available.

For this pin mapping (absent in most IBIS files) is imperative.

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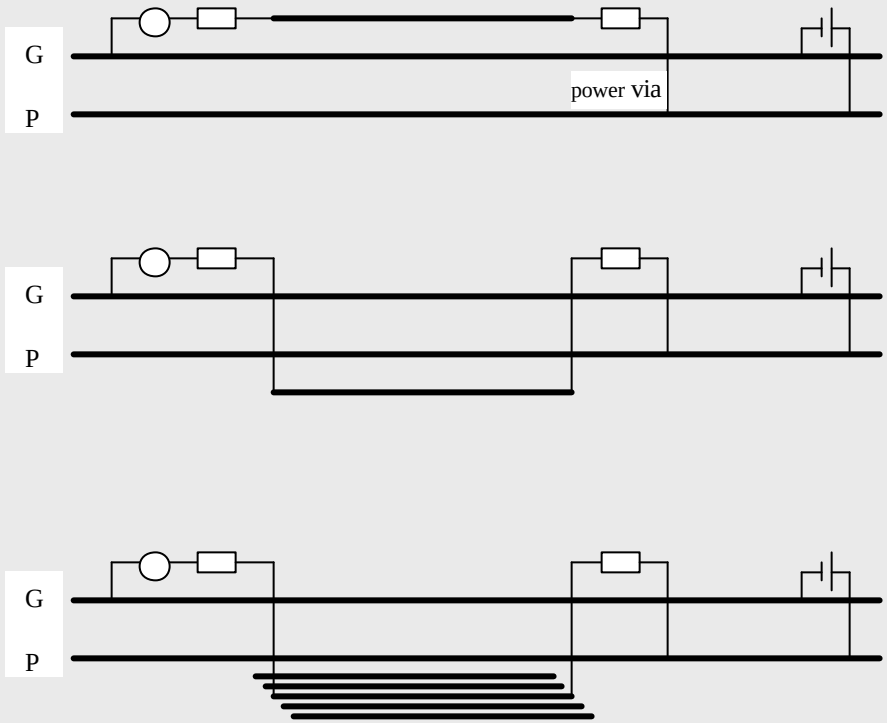
Return Path Discontinuities and Simultaneous Switching Output (SSO)



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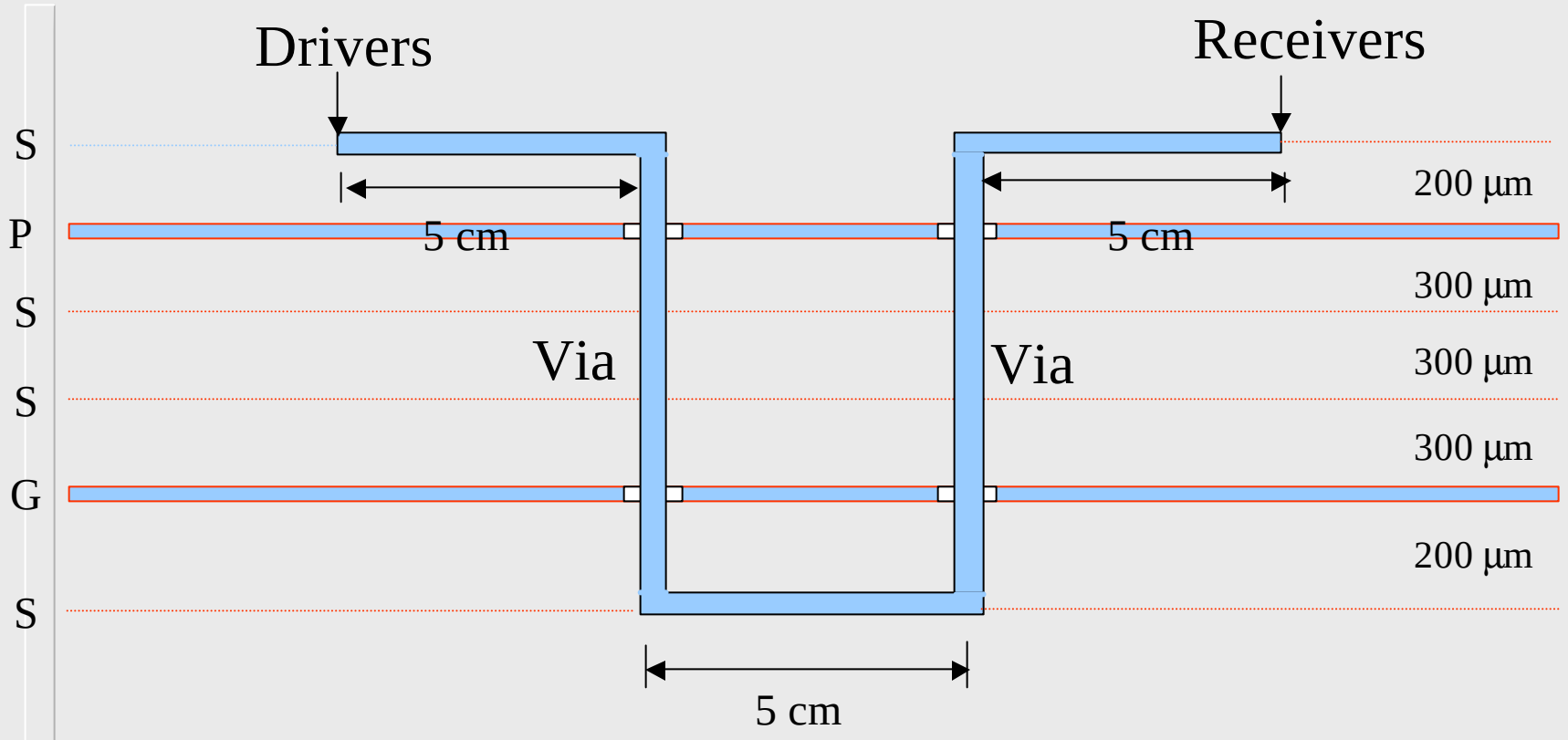
Effects of Signal Return Path Discontinuity – Layer Geometry



Trace width = 200µm; Trace thickness=35.6µm; Trace separation = 4 mm;
Series matching resistance= 55 Ω;
Drivers and Receivers are IBIS models from part 74LVC125A

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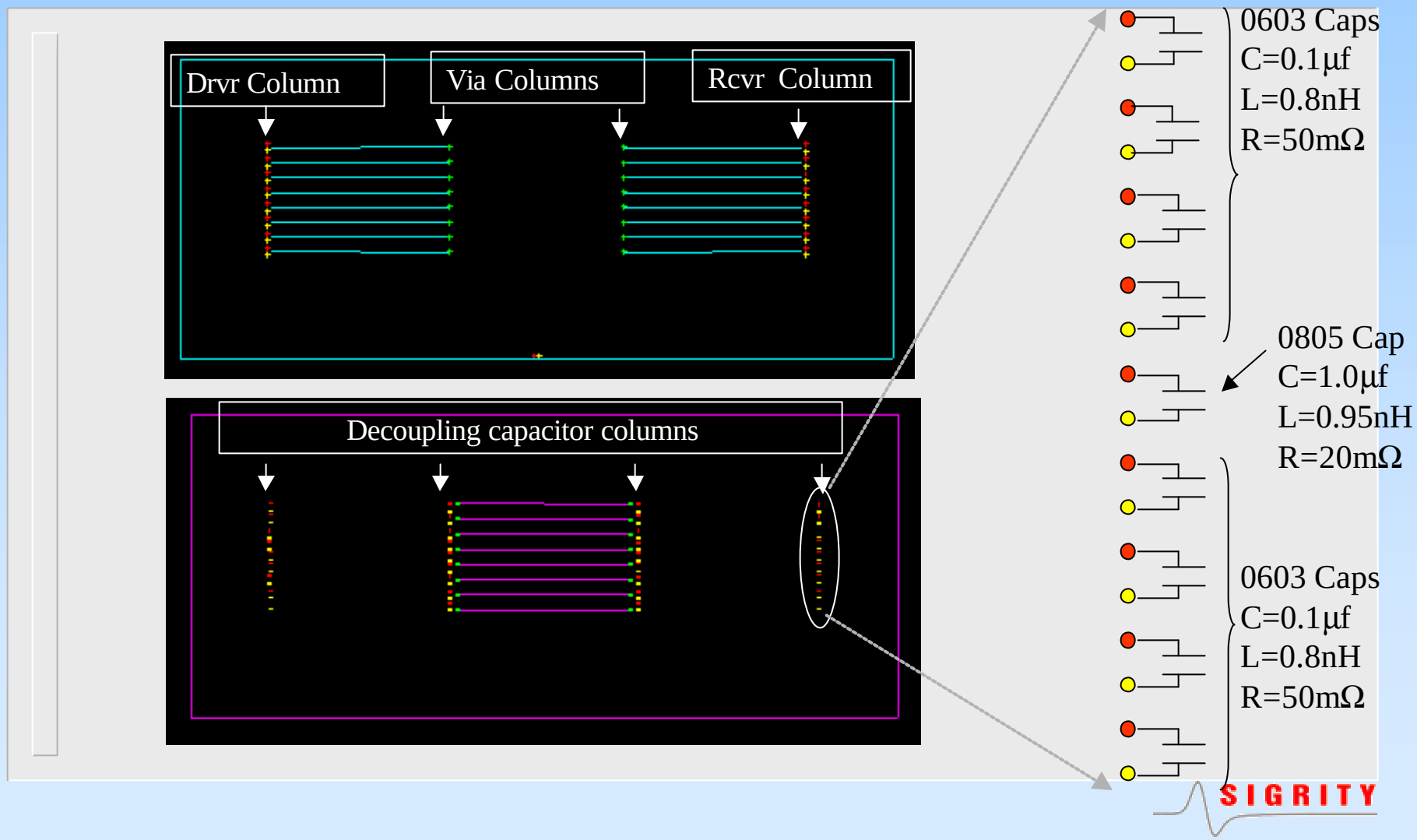
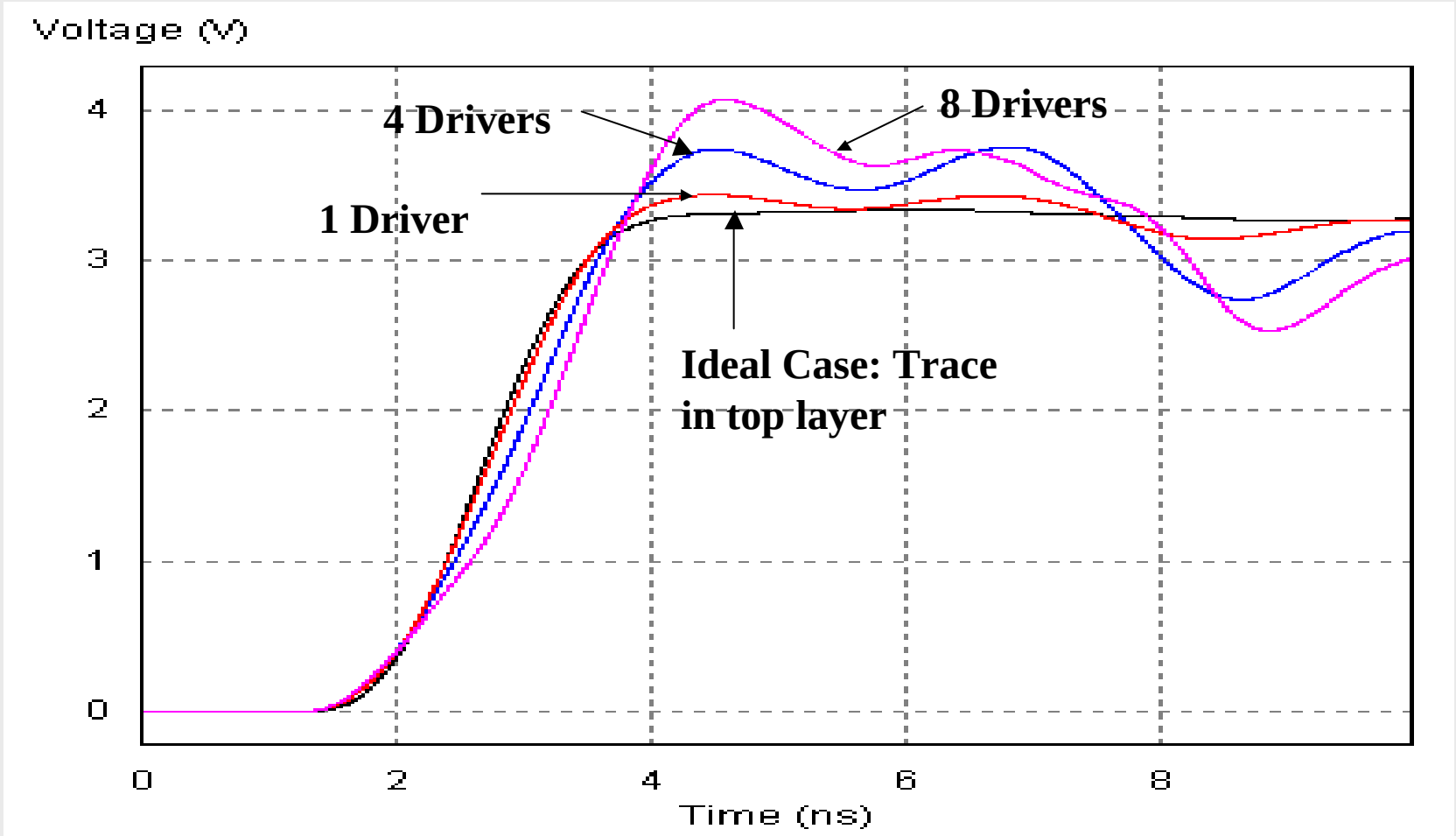
Top and Bottom Layers of the Board



Voltage Waveforms at One Receiver As the Number of Simultaneous Switched Drivers Varies

(no decoupling caps used)



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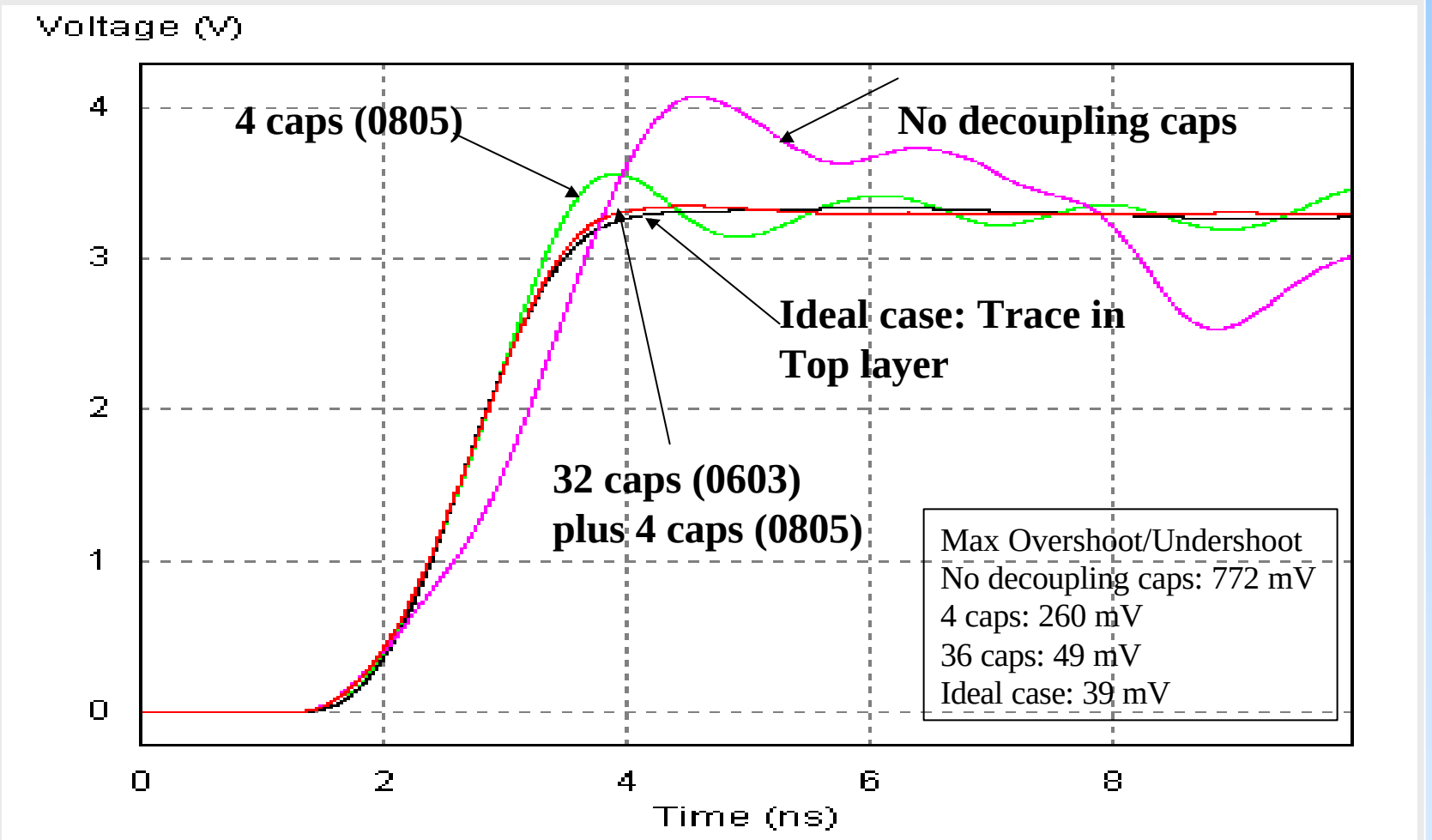
Effect of Decoupling Caps on Receiver Voltage with 8 Drivers Switching Simultaneously



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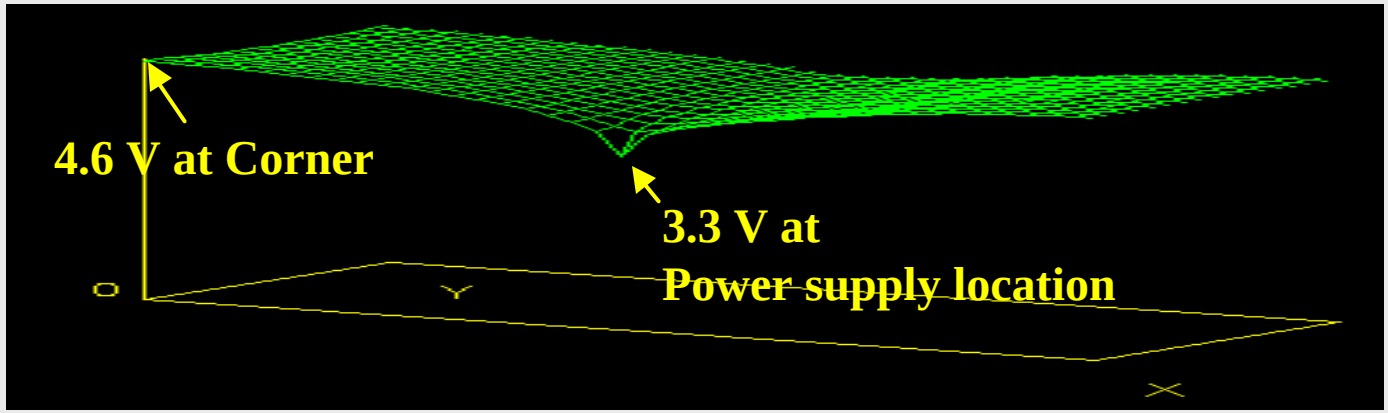
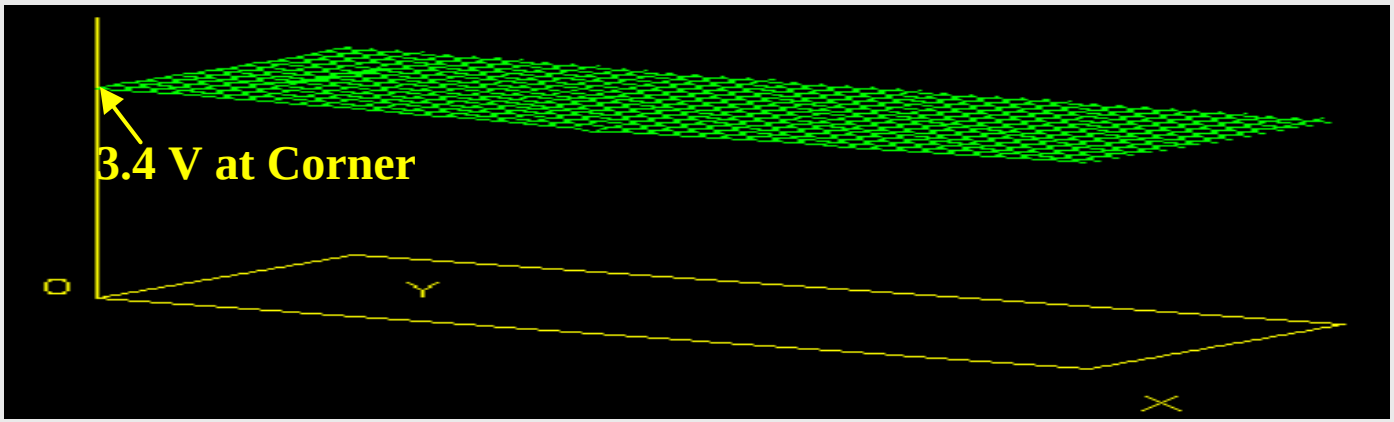
Power/Gnd Voltage Historical Peak Surface Plot with and Without Decaps



No Caps



With Caps

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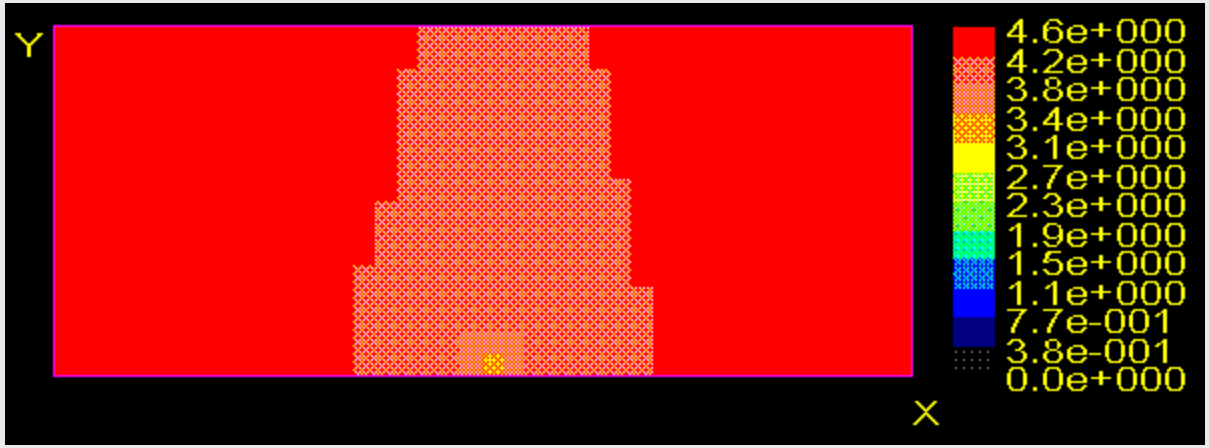
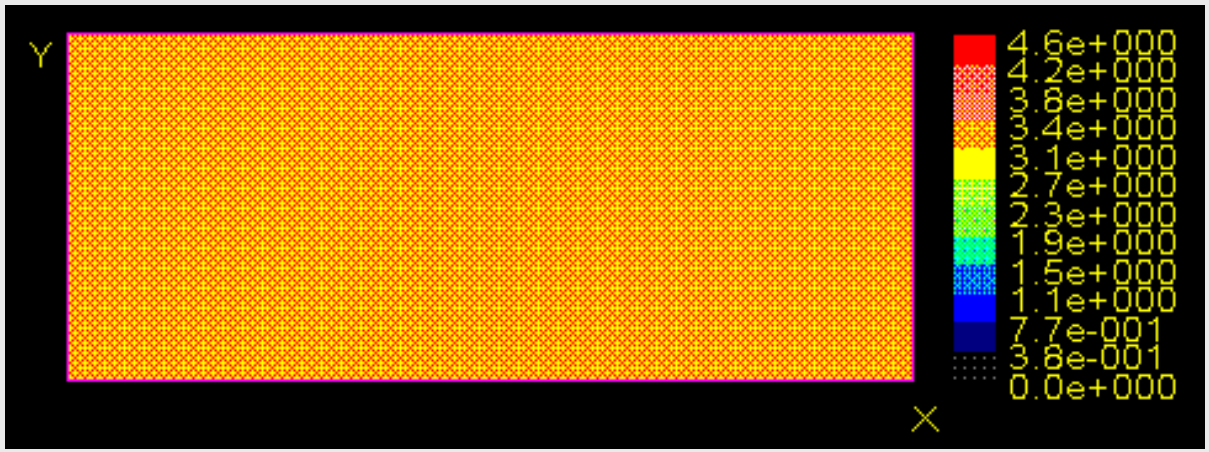
Power/Gnd Voltage Historical Peak Color Intensity Plot with and Without Decaps



No Caps



With Caps

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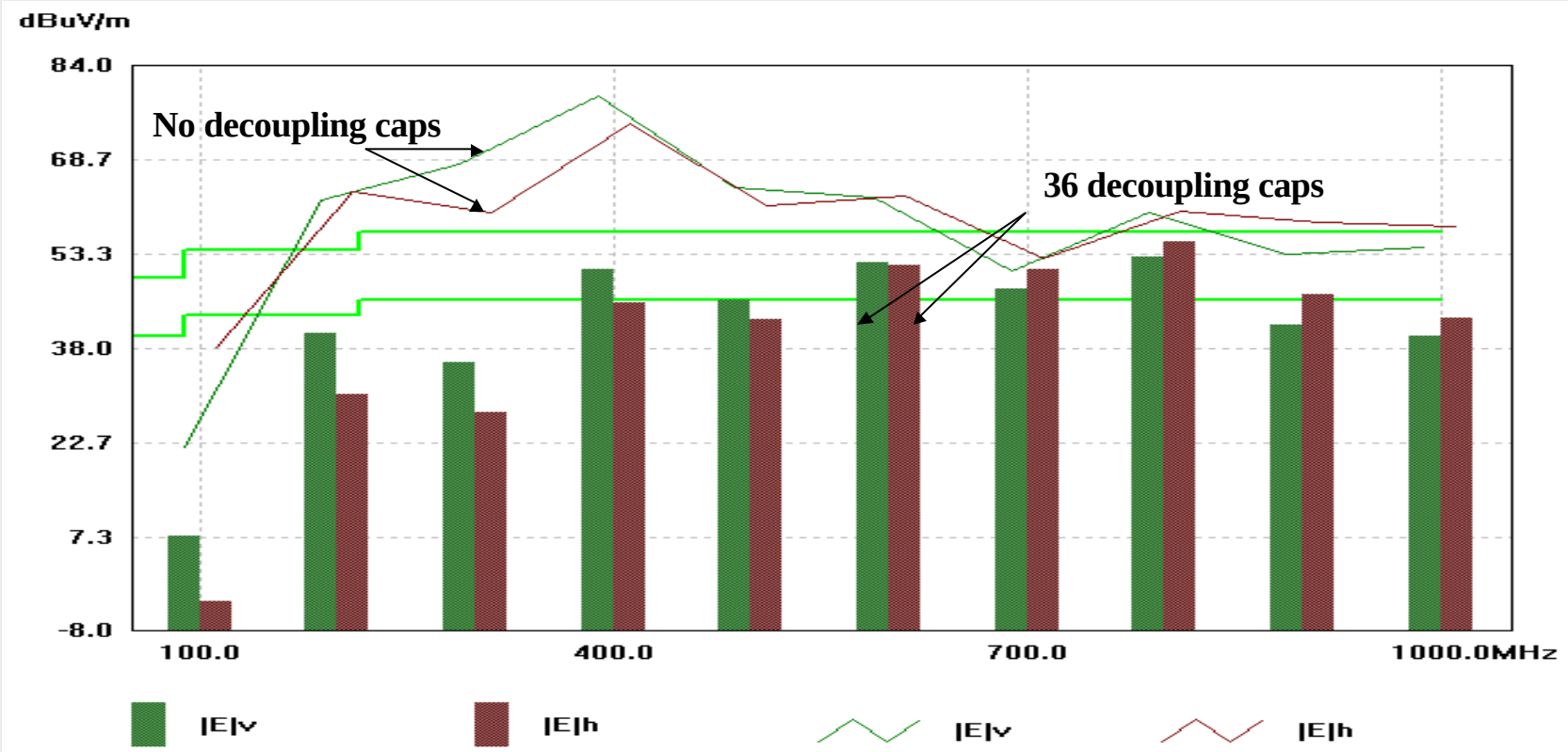
Effect of Decoupling Caps on Edge Radiation



Edge radiation was calculated corresponding to waveforms in the previous slides. The higher power-ground noise without decoupling caps leads to much higher edge radiation. This was measured at a horizontal distance of 3m and a vertical distance of 3m from the board

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Situations where Pin Mapping Essential

- Many power and ground pins in one IC
- More than one power supply – say 3.3V and 2.5V
- Separate power pins for Core and I/O parts of IC
- Pullup and power clamp may go to different power pins or pulldown and gnd clamp may go to different pins
- Separate analog and digital ground pins

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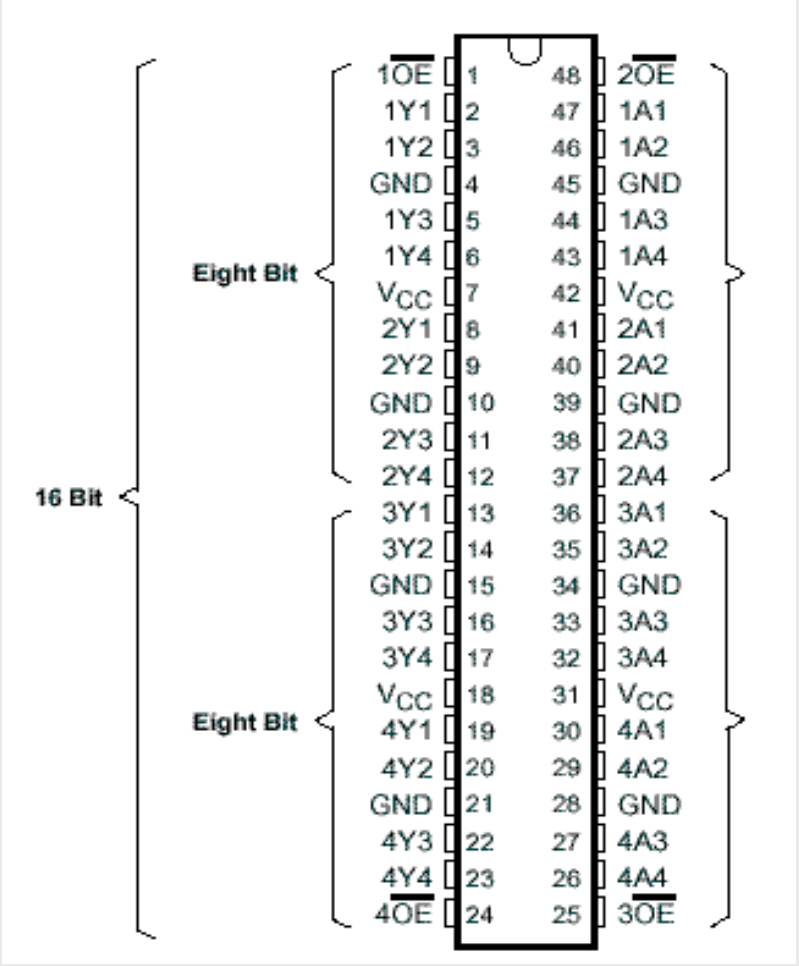
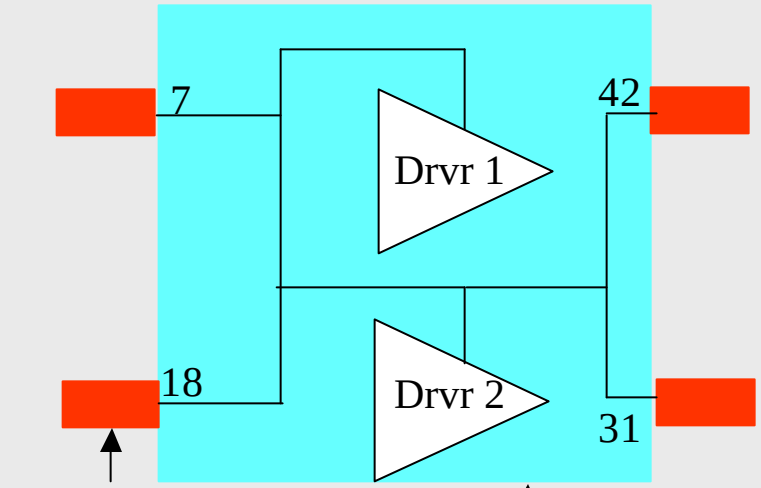
Pin Configuration ABT244



Many VCC and GND pins. Probably all VCC connected
together inside IC. Same for Gnd. If we are simulating drivers on this IC,we connect their VCC to all VCC pads of this package on the PCB.

But this is an assumption



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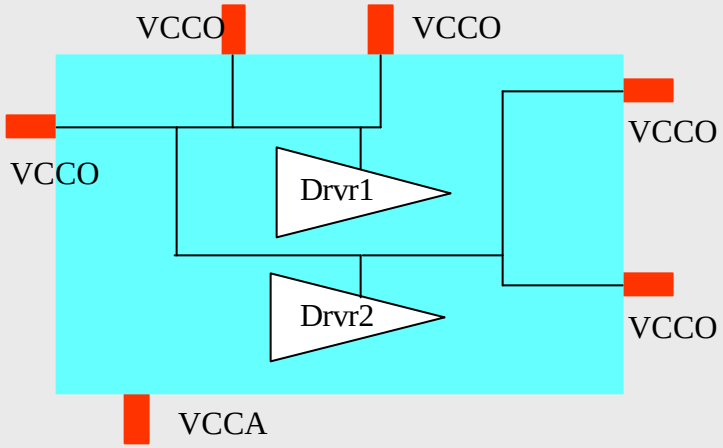
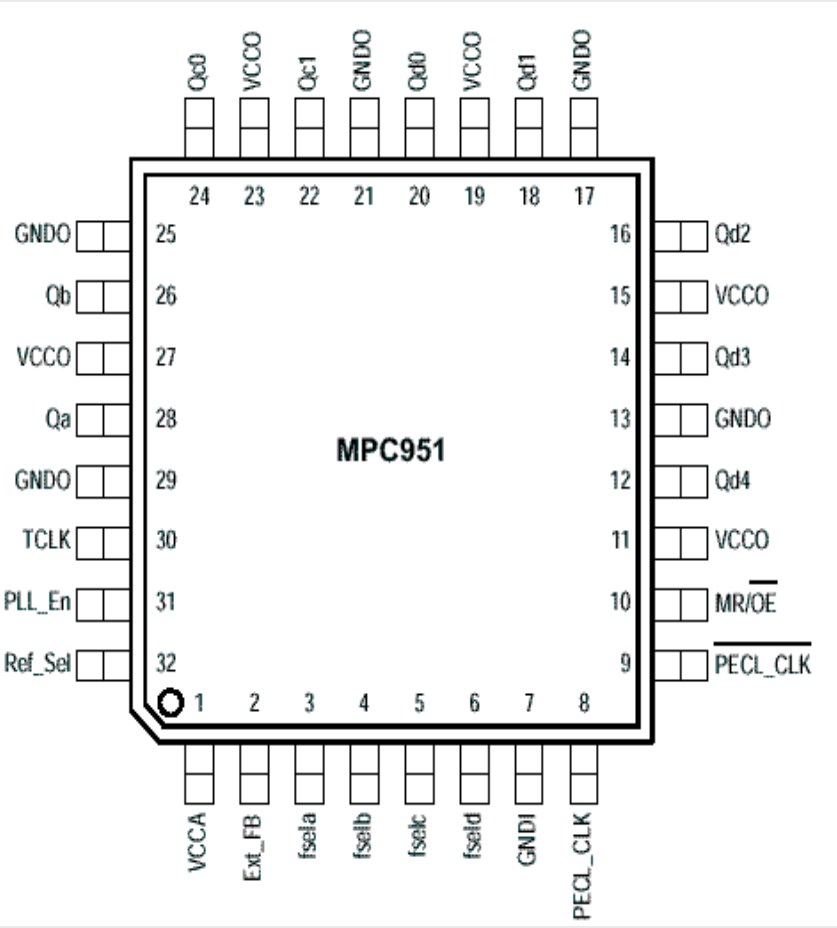
Pin Configuration for MPC951

There are separate analog and digital GND and VCC pins. They are probably not joined together inside the IC. So the VCC for the buffers must come from VCCO and not VCCA. It is even possible that different drivers get their VCC from different VCCO pins. This information needs to be given in the pin mapping in order to do POWER/GND simulations.





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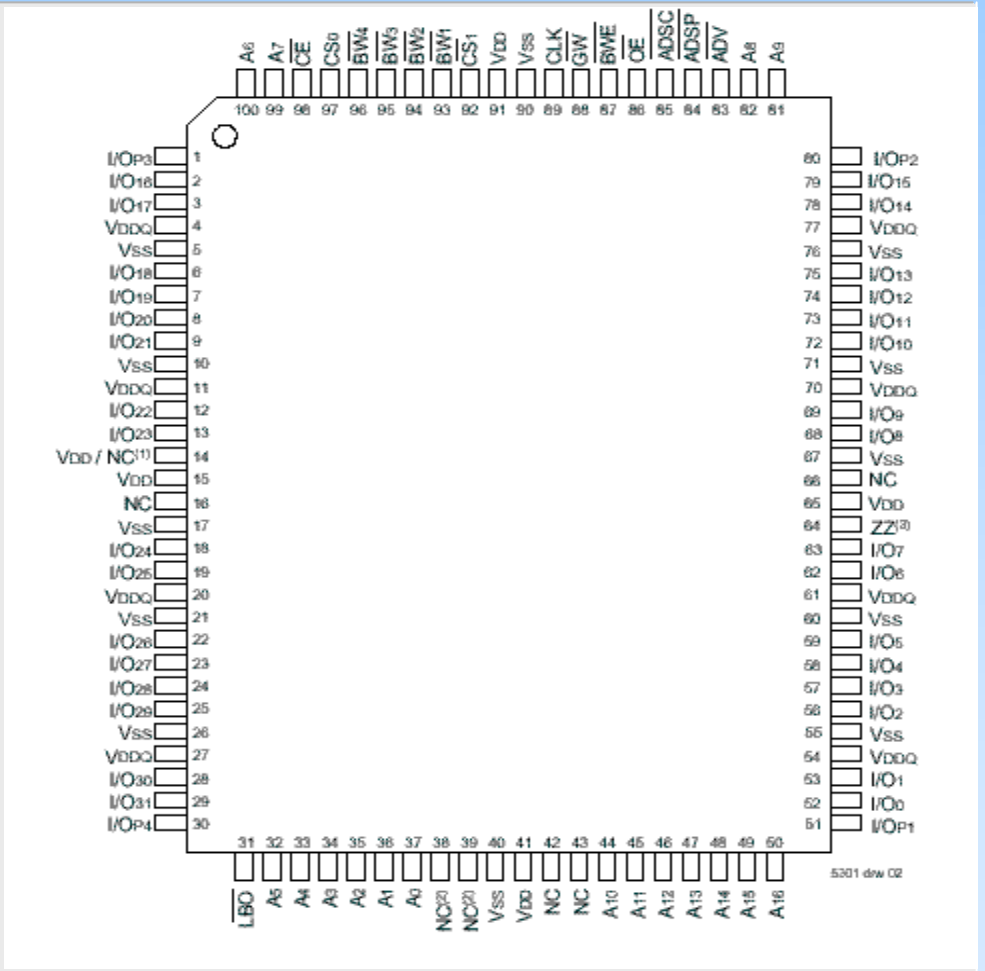
Pin Configuration for IDT71V35761

Separate VDD and VDDQ pins
VDDQ – I/O pin supply
VDD – Core Logic supply

Pin Mapping given for this part

Pullup for drivers goes to VDDQ
Power clamp goes to VDD



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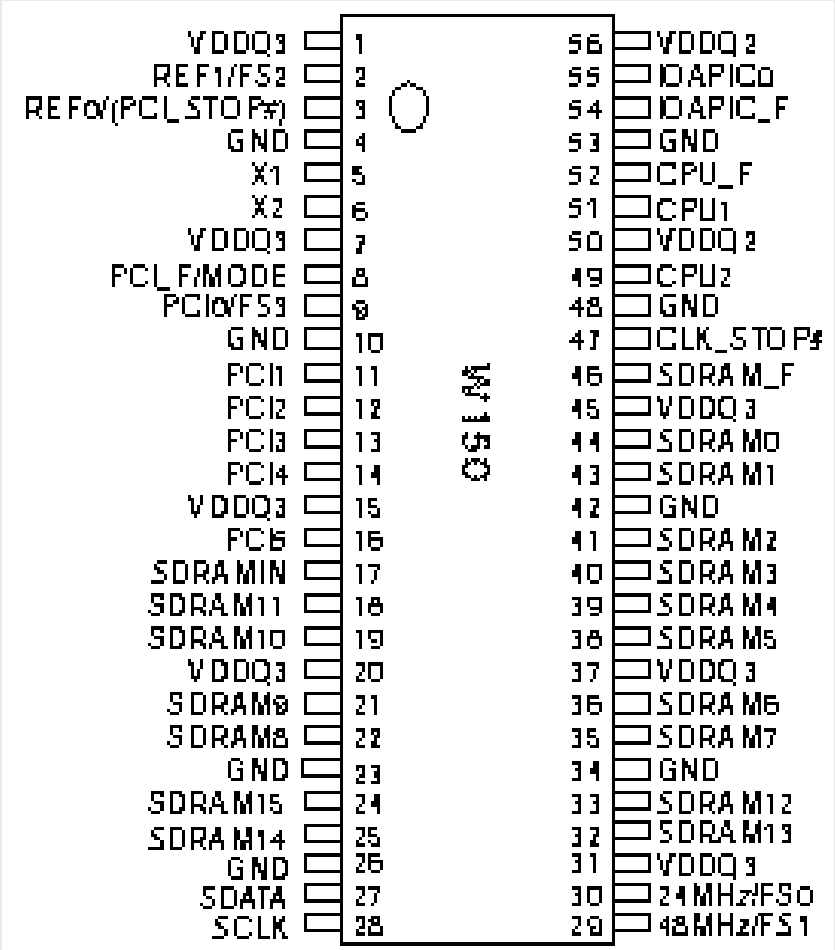
Pin configuration for CYPRESS W150

Has VDDQ2 and VDDQ3 supplies.
VDDQ2 = 2.5 V
VDDQ3 = 3.3 V

Pin Mapping given for this part



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Example of Pin Mapping (Cypress W150)

[Pin]	signal_name	model_name	R_pin	L_pin	C_pin
1	VDDQ3	POWER	70.00m	8.00nH	1.40pF
2	REF1/FS2	ioref1x	80.00m	9.00nH	1.40pF
4	GND	GND	65.00m	7.00nH	1.40pF
7	VDDQ3	POWER	40.00m	6.00nH	1.40pF
10	GND	GND	40.00m	3.50nH	0.85pF
29	48MHz/FS1	iofd48	80.00m	7.00nH	1.40pF
50	VDDQ2	POWER	55.00m	4.50nH	1.40pF

[Pin Mapping]	pulldown_ref	pullup_ref	gnd_clamp_ref	power_clamp_ref
1	NC	PWRBUS1		
2	GNDBUS1	PWRBUS1		
4	GNDBUS1	NC		
7	NC	PWRBUS2		
10	GNDBUS2	NC		
29	GNDBUS2	PWRBUS2		
50	NC	PWRBUS4		

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Conclusions

- Pin Mapping section essential in IBIS Models to do power/gnd simulation.
- Power/Gnd simulation is a zeroth order effect. Accuracy of IBIS model may be a secondary issue for many situations.
- When pin mapping is available, a completely automated linkage of circuit models during board translation beocmes possible. This is true even for power/gnd analysis.

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