PAR FORM

PAR Status: New PAR (Approved PAR)
PAR Approval Date: 2004-09-23
PAR Signature Page on File: Yes

1. Assigned Project Number: 1850

2. Sponsor Date of Request: 2004-07-13

3. Type of Document: Standard for

4. Title of Document:
Draft: Standard for PSL: Property Specification Language

5. Life Cycle: Full-Use

6. Type of Project:
6a. Is this an update to an existing PAR? No
6b. The Project is a: New Standard

7. Working Group Information:
Name of Working Group: Language for Formal Specification of Electronic System Behavior
Approximate Number of Expected Working Group Members:10

8. Contact information for Working Group Chair:
Name of Working Group Chair: Harry Foster
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9. Contact information for Co-Chair/Official Reporter, Project Editor or Document Custodian if different from the Working Group Chair:
Name of Co-Chair/Official Reporter, Project Editor or Document Custodian: F. Erich Marschner
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10. Contact information for Sponsoring Society or Standards Coordinating Committee:
Name of Sponsoring Society and Committee: Corporate Advisory Group
Name of Sponsoring Committee Chair: Chuck Adams
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Name of Liaison Rep. (if different from the Sponsor Chair): N/A
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Name of Co-Sponsoring Society and Committee: Computer Society Design Automation
Name of Co-Sponsoring Committee Chair: Peter Ashenden
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Name of Liaison Rep. (if different from the Sponsor Chair): N/A
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11. The Type of ballot is: Entity Sponsor Ballot
Expected Date of Submission for Initial Sponsor Ballot: 2005-03-30

12. Fill in Projected Completion Date for Submittal to RevCom: 2005-09-30

Explanation for Modified PAR that completion date is being extended past the original four-year life of the PAR: N/A

13. Scope of Proposed Project:
The Accellera Property Specification Language (PSL), a language for formal specification of electronic system behavior, was developed by Accellera, a consortium of Electronic Design Automation (EDA), semiconductor, and system companies. The proposed project will create an initial IEEE standard based upon Accellera PSL version 1.1. The IEEE standard will refine Accellera PSL version 1.1, addressing errata and a few minor technical issues and clarifying how PSL interfaces with various standard electronic system design languages.

Is the completion of this document contingent upon the completion of another document? No

14. Purpose of Proposed Project:
The purpose of this project is to provide a well-defined language for formal specification of electronic system behavior, one that is compatible with multiple electronic system design languages, including IEEE 1076 VHDL, IEEE 1364 Verilog, IEEE 1800 System Verilog, and OSCI SystemC, to facilitate a common specification and verification flow for multi-language and mixed-language designs.

14a. Reason for the standardization project:
As the complexity of Very Large Scale Integration (VLSI) has grown to the degree that the traditional approaches have limitations, and the verification costs have reached 60%-70% of the development resources, the need for advanced verification methodology, with improved levels of observability of the design behavior and controllability of the verification process has become critical. Over the last decade, a methodology based on the notion of "properties" has been identified as a powerful verification paradigm that can assure enhanced productivity, higher design quality and, ultimately, faster time to market and higher value to engineers and end-users of electronics products. Properties, as used in this context, are concise, declarative, expressive and unambiguous specifications of desired system behavior, that are used to guide the verification process. This standardization project will provide the EDA industry with a standard language for specifying electronic system behavior using properties, also referred to as a property specification language. This language will facilitate property-based verification using both simulation and formal verification, thereby enabling a productivity boost in functional verification.

15. Intellectual Property:
Has the sponsor reviewed the IEEE patent policy with the working group? Yes
Is the sponsor aware of copyrights relevant to this project? No
Is the sponsor aware of trademarks relevant to this project? No
Is the sponsor aware of possible registration of objects or numbers due to this project? No

16. Are there other documents or projects with a similar scope? Yes
The scope of this PAR addresses issues that are encompassed, either implicitly or explicitly, by previously submitted PARs, specifically, P1076 (IEEE Standard VHDL), P1364 (Standard for Verilog Hardware Description Language), P1647 (Standard for the Functional Verification Language 'e'), and P1800 (Standard for SystemVerilog Hardware Description Language). These four PARs deal with languages used in the design and verification of electronic systems. While any language developed to support the verification of circuit design must recognize properties and provide methods for their use, this PAR specifically focuses on cross-language, formal specification of properties and is therefore complementary to the existing PARs. Moreover, the teams of these working groups are working in collaboration.

Similar Scope Project Information:

17. Is there potential for this document (in part or in whole) to be adopted by another national , regional or international organization? Do not know at this time
If yes, please answer the following questions:
Which International Organization/Committee?
International Contact
Information?

18. If the project will result in any health, safety, or environmental guidance that affects or applies to human health or safety, please explain in five sentences or less.

19. Additional Explanatory Notes: (Item Number and Explanation)
Item 7: The list of initial IEEE-SA Corporate Members that have been identified to participate in this project include: Accellera Organization, Cadence Design Systems, IBM, Intel, Mentor Graphics, Synopsys and Verisity Design.

Item 13: It is expected that once the initial IEEE Standard for PSL has been completed and approved, the P1850 working group will pursue further extensions to the standard via an updated PAR, as is typical with IEEE standards.