EVE:

EV Engineering as a product and service company specialized in H/W assisted verification and test bench automation, is very interested in participating to the ITC group and the SCE-API sub-group.

We would mainly like to propose and discuss ideas on how to facilitate the use of the SCE-MI norm for both transactor library developers and end-customers.

We are also interested in working on standardization of any type of cycle based interaction between S/W and H/W.

We can devote about 1 day per month for working with the group.

Infineon

Like other users and model developers, Infineon Technologies support the goals of the development of interfaces (high performance and high level) for the purpose of SOC verification. Our engineers have developed API's to link model together and also to link debuggers (hardware and software). Interoperability, with other models (external and internal) and interoperability between tools and emulation is a high concern. We believe that ITC and its subgroups can achieve good standards to solve common challenges that the modeling and verification environment faces today.

Infineon is a supporter of open standards that are available to people with no strings attached. As such Infineon support Accellera ITC and its approved SCE-API subgroup for the development of interfaces. SCE-API is a good start, but we need to expand the interface to other environment especially to software models and debuggers. The representative from Philips has shown a good vision for ITC and we share that vision.

Infineon is committed to support this effort by assigning a person 1 day per week.

TransEDA

TransEDA is dedicated to providing a complete, ready-to-use verification environment including application-specific test automation, bus functional models, coverage analysis and property checking all working seamlessly within a heterogeneous simulation/emulation/acceleration environment.

As a founding member of SCE-API, TransEDA is committed to the success of the ITC and its SCE-API subgroup. TransEDA is particularly committed, in the near term, to supporting the development of a standard interface enabling coverage on emulators, to fulfill one of the requirements of the original SCE-API charter.

TransEDA is prepared to allocate 1 day per week towards the development and realization of these standards.

Cadence

Cadence is committed to the success of the ITC group and the SCE-API subgroup.

We would like to see the group broaden the scope of the models supported to more than emulation through this process. New interfaces should allow both software and hardware engines to be used interchangeably where it makes sense. Where they don't, they should be separate interfaces.

The following are Cadence's position on the issues raised at the last meeting:
* The goals discussed are acceptable: set a roadmap by DAC, complete one interface standard and have a draft in progress for a second by the end of 2002. The roadmap by DAC may be a little too aggressive but it is an acceptable goal.

* Richard Sayde commits to about 2 hours per week.
* Andy Eliopoulous commits to 1/2 to 1 day per month.
* Cadence was not a founding member of the SCE-API and did not sign the technology transfer letter.
* No problem with transferring source documents from SCE-API to Accellera.

CoDesign

Co-Design Automation focuses in the design and verification of systems, with SUPERLOG, a state of the art design language, and SYSTEMSIM, a unique state of the art simulator. Therefore, we are very interested in methods that improve the interfacing of simulation technology with other system level design and verification tools.

The idea of high abstraction data interfaces between the different components in system design and verification environment is one that we find extremely intriguing, and have internal expertise in. We have been focusing on addressing the interface data abstraction challenges using our language and simulation technologies.

We think the work of this committee is very valuable, and are exited to be part of setting standards in this area, as well as implementing such standards as they are ratified.

Axis

Axis Systems would like to participate on the interfaces technical committee for the purpose of creating an SCE-API standard that is available to all emulation vendors. With a level playing field all vendors will compete on technical merit. Currently each vendor has proprietary C modeling interfaces and users are being confused about which C interface is better.

We also believe a standard interface is needed to enable model reuse across hardware platforms. We welcome this reuse and will be happy to enable the use of existing models and tools with our RCC platform.

Axis would also like to participate in the standard development with the goal of making the current donation more generic and adding capabilities that provide a better overall solution and not vendor specific or the least common denominator of what each vendor can implement.

We are especially interested in debugging. Debugging is the highlight of our acceleration and emulation platform and we feel we can contribute to advance the state of the art in this area.

Axis has not participated in SCE-API until now so we are coming in with very little history, but a fresh perspective that will be beneficial to the group.

STM

As a founding member of SCE-API committee, ST is keen on developing the ITC standard under ACCELLERA. SoC design methodology requires a combination of design technologies, operating at different level of abstraction. A standardized integrated environment will provide a solution, that will fill up the performance gap that we are currently dealing with. There are three main objectives that we want to achieve with the ITC committee:

1) Review SCE-MI and release it as an ACCELLERA standard.

2) Define the Control interface, that allows handling multiple-engine configurations. This is a quite general goal and might be split into steps.

3) Interactive debug interface. Of course, improving performances is the main focus of the SCE-API but debug features are important as well.

Since SCE-API started from the need for a significant performance improvement for system validation,it would make sense including some performance analysis features in the standard that will help to identify possible bottlenecks.

STM's people (agrate,crolles and grenoble can work on the ITC for a total of one day per week

---

Philips Semiconductors

has put considerable effort in reducing the time and cost to market company-wide, for both SoCs and IP blocks.

As part of this strategy we feel that a co-ordinated approach to prototyping is critical.

Individual component of this prototyping strategy are readily available and are put to good use in our design flows. Emulators, custom RSP systems (Velocity and NAPA for Philips), software simulators, verification frameworks and languages will continue to serve well our business lines for the upcoming couple of years.

In order to significally advance the state of the art and provide our development groups with the tools they will need a few years from now, we also known that increased interoperability between tools and prototyping systems is required.

We saw great opportunities in the SCE-MI interface and joined the corresponding working group. We're now very exited about continuing this work under the Accellera umbrella. The widened scope of the Interface TC goes a long way towards the vision Philips has for prototyping but at the same time poses significant challenges in terms of organizing the work over a considerable span of time. Philips position has been presented in more detail in some presentations I've delivered to this group, so I won't bore you here.

It is critical, in my opinion, that we reach soon a group agreement as to what we want to accomplish and how to schedule the work over the upcoming months. Having meaningful intermediate deliverables will keep the group focused while providing EDA vendors with something to implement as we go.

I think that finalizing the Modeling Interface will be a useful first step. For Philips this will require some further reviewing rounds from groups that weren't initially involves in order to check compatibility with execution engines different from conventional emulators and proposing changes were we to find problems with the present specification.

A second step I think we've to take rather soon is get the ball rolling on the Control Interface. During one of the last pre-Accellera meetings, it was suggested that customers should have worked on a requirement

document and this might be a reasonable way for getting started. We can also decide to have a formal subgroup devoted to this issue.

A debugging interface is also important, but in my view comes after the points I've just mentioned. If the rest of the group have stronger feelings on this, I'm not against starting some work on this.

It is also critical that each participant makes a reasonable effort to disseminate the work done under Accellera inside their own organization. I'll certainly try to do it for Philips.

From my side, I can devote about 1/2 day/week for working on the normal operation of the working group. More time can be discussed for specific deliverables. I'll also try to get more people in Philips directly involved in this effort (in particular, we have groups which would be potentially interested on different aspects of debugging and might consider participating)

Mentor Graphics

As a founding member of the SCE-API, Mentor Graphics is committed to ensuring the success of the work that has gone on so far with the MI and CI and is eager to see its expansion into new areas. We value the successful implementation and adoption of industry standard interfaces for all facets of verification and are keen to see standards that span multiple levels of abstraction and execution environments. In order to achieve this we would like to concentrate on 3 primary objectives in the near term:

1. A broader review of the SCE-API to bring about industry consensus and the publishing of the first Accellera standard in this area.

2. An extension or layer on top of the MI that would support a distributed multi-client environment that would allow more than 2 parties to be involved in the communications.

3. A completion of the CI interface that includes both the batch and interactive modes of operation such that debugging operations can be performed. This includes not only the DUT but also the transactors.

As a longer term goal, we would like to see a complete peer to peer multi-abstraction environment be created that would allow models from various sources to be easily integrated together to form a virtual prototype spanning the system level through to the implementation. By model we would include not only a DUT, but also test models, 'diagnostic and debug models' and analysis functions.

In order to help Accellera meet these objectives, we will commit 1 day per week of effort from Brian Bailey to act as chair of the TC and contributor to the working groups. In addition, members of the various interface groups within the company will provide review and comments on all materials produced and may be available for direct contributions in specific areas on a short term basis. They will also be working on the implementation of the interfaces as they near completion.

IKOS Systems

is dedicated to providing comprehensive, high-performance verification solutions for integrated circuit design. Accordingly we have developed innovative hardware and software systems, enabling designers to verify their complex designs in every phase of thedevelopment process.

The co-modeling technology, developed in this context, was donated to the SCE-API concortium at its founding, and is the basis of the current SCE-API. Ikos' interest in donating this technology is to promote

standardized high performance transaction based methodologies for use with emulation or similar high-performance hardware platforms.

As one of the founding members of the SCE-API consortium, Ikos is committed to the success of ITC and the SCE-API sub-group. Ikos strongly believes that connecting software models to emulation with performance in the 200khz to 10 MHZ range, is an important part of closing the existing verification gap and of enabling the wide adoption of high gate-count, complex SoC desings.

The need for highspeed connection between emulation and software modeling environments is driven by several trends, including the growing prevalence of high speed architectural models, the increasing use of some form of executable specification, and the increasing difficulty of slowdown for emulation target environments.

Ikos believes that the primary initial goals of the ITC group should be to finish the SCE-API, including the SCE-CI portion, retaining the emphasis on performance and portability and resulting in a standard which can be widely adopted by modeling environment vendors including, but not limited to Verisity, SystemC, transEDA, HDL simulation vendors, Vera, as well as emulation and hardware-acceleration vendors.

Almost all software models are written in the context of some modeling environment. Open standards, usable both directly and by software modeling environment vendors are the best way to facilitate the connection of abstract and efficient software models to hardware accelerated verification platforms.

As SCE-API moves into Accellera, providing an opportunity to broaden its scope, Ikos would like standards to be a part of expanding the role of emulation in the both the architectural exploration and hardware-software verification portions of the design cycle. The increasing software content of designs, the variety of architectural and HW/SW coverification tools and the increasing need for intelligent architectural trade-offs using real performance information from legacy IP blocks make these areas fruitful for exploration within a standards body such as the ITC group.

Finally, within the ITC group, Ikos would like to see greater participation by and advocacy to the vendors of modeling environments.

Verisity

is focused on providing best-in-class solutions to address the challenges of functional verification. Our customers, who use our products to verify the most complex chips and systems, need to create an environment that can get that job done most effectively. Strong commitment to both interoperability and the support of standard interfaces is required by vendors to enable customer to meet that need. Verisity fosters such commitment, at both the interface and language levels, via our own VIP and LicenseE programs and through our participation in Accelera and other external organizations, and we plan to continue our efforts in this arena.

Many of our customers also take advantage of the hardware-assisted verification technologies available today. We are committed to participating in the Accelera ITC and the SCE-API subgroup to develop the open interfaces necessary to enable our customers to gain maximum leverage with these tools. We would like to participate in helping drive the specification and in developing the interfaces and associated debugging capabilities to align closely with testbench automation tools like Specman Elite. Verisity will therefore commit 1 to 2 days per month to help realize these goals via Accellera.

Synopsys

As a leader in verification and system design, Synopsys recognizes customer need for high-performance interoperability between testbenches, simulators, system verification tools and emulation/acceleration

hardware, along with suitable debugging capabilities. We believe that SCE-API as part of ITC can improve and grow the a standard plus drive adoption into the industry to solve real-world verification and design problems. That's one of the reasons we were a charter member of this group.

Synopsys is a leader in driving and supporting open standards that secure broad industry adoption and that truly provide value to the design community. We therefore support the existence and expansion of the SCE-API subgroup for the development of high performance interfaces, and have already begun delivering product solutions that leverage the current SCE-API/SCE-ME draft standard.

We can contribute 2-3 person days per month for discussion, review and feedback on extensions to the current SCE-API spec, leveraging several of our experts in verification and system design.