Accellera ITC co-chair

Maurizio Vitale

Born in 1965. Graduated with a Masters' degree in Electrical Engineering from the university of Genoa. I worked in research (Georgia Institute of Technology, branch penalty reduction for superscalar processor (1993-1997). University of Leuven (Belgium), compilation of cyclostatic dataflow graphs for DSP application (1997-1999)). I've also experience as hardware designer (Video Display Systems, design and prototyping of a graphic workstation and design of a parallel supercomputer for SAR images processing (1991-1993).
Three years ago I joined Philips, at first as responsible for a new line of digital LCD screens for Philips Components. I then moved to Philips Semiconductor where I worked on digital video processing ICs (mainly for Plasma displays). Since the beginning of last year I moved to the System Level Design group where I'm leading the activities for the more long term design flows.
In this context, I've got very interested in the potentials of the SCE-MI and started working with this group. I'm member of a number of working groups. Among the ones outside Philips I participate in the works of the SystemC dataflow working group and the SystemC verification working group.

Elliot Mednick

20 years in computer hardware and software development. 6 years on hardware/software coverification, including integration of ISSs to Seamless, Eaglei, and VCPU as well as development of at least 5 different in-house implementations (including a Verilog/Perl coverification environment for a P6-based system which was used by Data General for 2-3 years).

Other experience includes implementing and selling a full Verilog simulator ("VeriWell"); system bus architecture and implementation and MIPS EJTAG h/w implementation for MIPS-based RISC IP at Lexra; various verification infructructure, ASIC development, system design, and OS development for such companies as Avid Technology, Data General, Wellspring Solutions, Encore Computer, and Prime Computer.

Currently Lead Architect for Embedded Systems Design at [Cadence Design Systems].

Voting member of IEEE 1364-1995 working group; program committee member for HDLCON/IVC 1991-1998, 2002; Program Chair HDLCON [1998]. Have presented several papers and tutorials on Verilog coding style, Verilog for architectural modeling, and Verilog/Perl coverification.

Francesco Sforza

Born in 1960, Ferrara, Italy I got my degree in Electronics from the University of Padova in 1987. After a short experience in Italtel on the configuration process of digital switching telephone equipment, I joined ST, Central CAD group. For the past three years I've led the Dynamic Verification Team in CR&D, focusing on emulation, fast prototyping and Testbench Automation. Current IEEE member, I've participated to the balloting process of a few HDL related Standards.

Accellera ITC SCE-API working group chairs

Duaine Pryor, Ph.D.

is the chief architect of the Ikos CoModeling line of products. He was the author of the TIP API which was transformed into the MMCT API, and then donated by IKOS to the SCE_API group. Duaine served as the technical lead in all of the SCE_MI meetings prior to the transition of the standard to Accellera. As technical lead, he was able to explain the concepts that IKOS was promoting, as well as incorporate the feedback from other participants, into the final version of the specification. More recently, he has been one of 3 key players in the evolution of the SCE_CI specification, and an active technical participant of the System Control working group.

Aside from his CoModeling efforts at IKOS, Duaine has a Ph.D. in Math from Berkeley, and has worked in the areas EDA, scientific computing, networking, pharmaceutical modeling, parallel computing and graphics.

It is without hesitation that I recommend Duaine Pryor as the Chair of the SCE_API working group. [Submitted by Jan Johnson]

Jason Andrews

is currently a Product Manager at Axis Systems, working in the areas of hardware/software co-verification and testbench methodology for SoC design. His experience in EDA and the embedded marketplace includes software development and product management at Simpod, Summit Design, and Simulation Technologies. He has presented technical papers at the Embedded Systems Conference, Communication Design Conference and IP/SoC and written numerous articles related to HW/SW co-verification, simulation acceleration, and emulation. As a recognized industry expert on co-verification he is now focused on verification methodology using C/C++ for test benches over transaction-based interfaces. He has a BS in electrical engineering from The Citadel, Charleston, S.C., and an MS in electrical engineering from the University of Minnesota. He currently lives in the Minneapolis area.

From the nominee.....

The SCE-API has great potential to be a widely adopted industry standard that enables interoperability and produces a win-win situation for EDA vendors and users. I understand there is a lot of history behind the SCE-API that Axis did not participate in. For this reason I believe somebody familiar with this history is best suited for chair of the SCE-API sub-committee. At the same time I believe a new person with a fresh perspective on the current challenges is the best fit for co-chair of the group. I feel that my background in modeling and transaction based environments as well as my software development experience with a different type of acceleration and emulation product (Axis RCC) makes me an ideal candidate for co-chair of the ITC sub-committee.