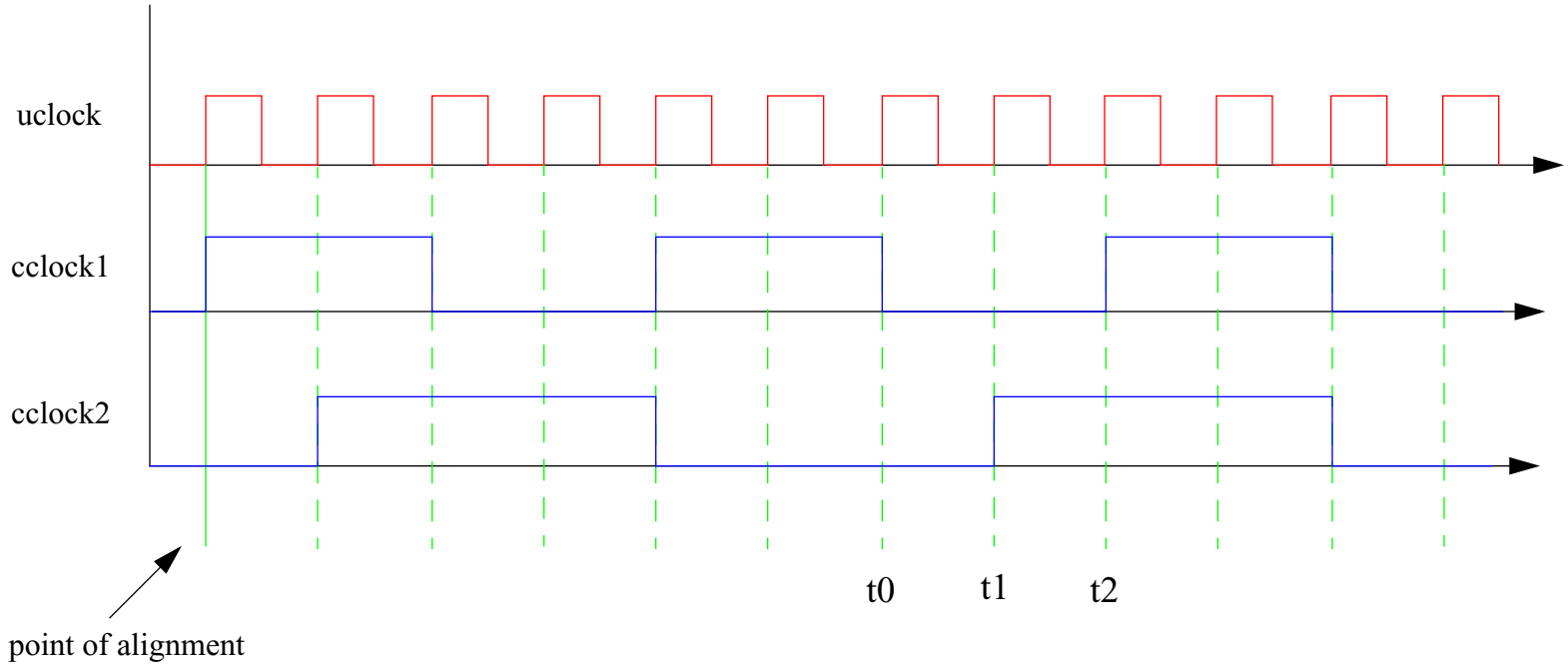
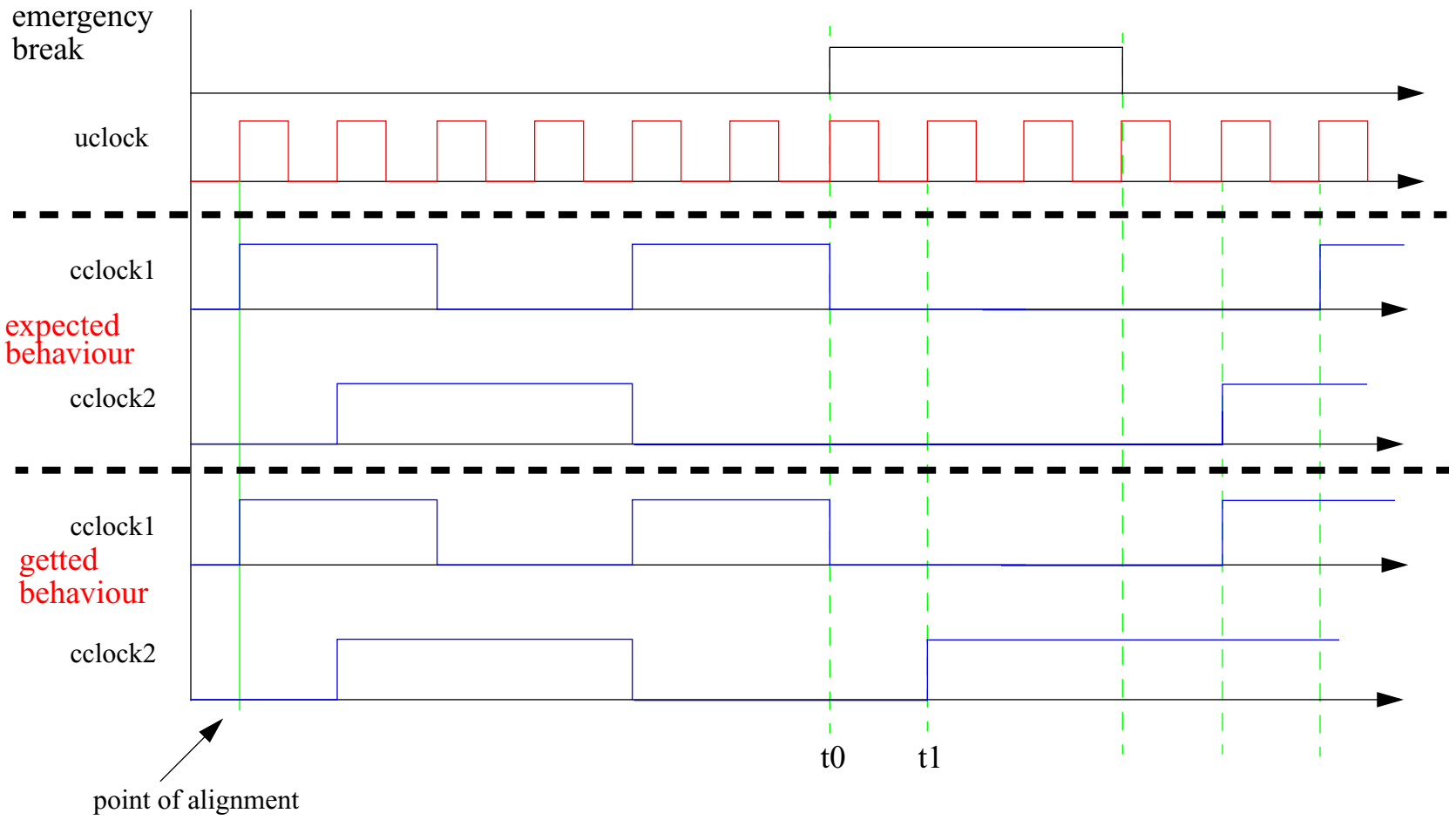


Let’s define two cclocks, cclock1 and cclock2.
cclock1 is the fastest clock, cclocks definitions are:
- cclock1: ratio: 4/1, duty cycle: 50/50, phase: 0
- cclock2: ratio: 6/1, duty cycle: 50/50, phase:5/6*100=83.33
In this example we care about both rising and falling edges of the two cclocks.

Now let’s imagine that an emergency break is required, the corresponding signal becomes high at time “t0”. If this emergency signal is linked with the fatest cclock (so cclock1), the next edge of this cclock will be disabled (no rising

edge at time t2). But because of the “just in time” mechanism, the rising edge of cclock2 will occur at time t1, so the emergency break will fail. (see next graph, “getted behaviour”)
To have the expected behaviour, the emergency break signal should disable the two clocks, the rising edge of cclock2 must not occur. (see next graph. “expected behaviour”)



To conclude, this example shows that using the fastest cclock of the design as a reference for emergency break clock control semantics is not enough. Cclocks phase have an impact on this.