SCE-MI 2.0 Proposals - Cadence vs. Mentor

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This document outlines discussion points of the Cadence and Mentor proposals of SCE-MI 2.0, supporting adoption of Cadence proposal.

1.0 Evolution versus Revolution

As stated in Cadence's presentation of 4/20/2005, the underlying principle of the Cadence proposal is to move the SCE-MI standard in an evolutionary manner. This approach, we believe, provides a more stable standard that will be more readily accepted by end-users, specifically because the primary goal of the standard is to ensure broad vendor support, with a high level of confidence that support of the standard will be consistent across vendors.

In the absence of a SCE-MI qualification suite and/or reference implementation, a more aggressive change to the standard opens the door for new differing interpretations of the standard, with no means (other than trial and review over time) to ensure cross-vendor compatibility.

1.1 Standards

The Cadence proposal remains based on a simple macro-based approach which leverages existing module/entity instantiations for (System)Verilog and VHDL on the hardware side. In contrast, the Mentor proposal is based on new pragmas in the Verilog and VHDL space. While the pragmas themselves conform to existing language syntax, the semantics of the pragmas are newly-proposed, and will require implementation changes on the part of vendors supplying Verilog and VHDL compilers in order to support Mentor's proposal.

1.1.1 Vendor Support

Broad acceptance of SCE-MI by users depends on support by a broad set of vendors. The SCE-MI 1.1 (and the Cadence-proposed 2.0), since they are based on low-level synthesizable HDL on the hardware side, can be supported based on 'off-the-shelf' syn-

thesis tools by smaller vendors. For example, post-synthesis netlists can be analyzed to find the macros within the netlists in a relatively straightforward manner.

The Mentor proposal requires some level of support of the proposed DPI syntax which is not guaranteed to be supported by all off-the-shelf synthesis tools. Smaller vendors will need to interpret Verilog/VHDL pragmas in original HDL, and may need to put requirements on the end user to supply information about SystemVerilog DPI functions that may otherwise not exist in post-synthesis netlists.

1.2 Backward Compatibility

The Cadence proposal's incremental approach bases new functionality directly on the semantics of the existing SCE-MI 1.1 standard. As such, we believe it provides a correct-by-construction means of ensuring backward compatibility and co-existence of newly-proposed functionality and existing SCE-MI 1.1 capabilities.

By contrast, the Mentor proposal is based on an entirely new (DPI, function-call-based) call and synchronization mechanism. It is unclear as to how transactors based on Mentor's newly-proposed SCE-MI will work in an environment with SCE-MI 1.1-based macros.

1.2.1 Synchronization Paradigm

The Cadence proposal leverages the existing SCE-MI 1.X synchronization paradigm. The CPD.a proposal is a 'natural' layer on top of the existing SCE-MI 1.1 macro approach. As such, the means by which the hardware and software sides of the system handshake with one another is understood, and 'correct-by-construction', with respect to backward compatibility with the SCE-MI 1.1 use model.

The Mentor proposal specifies a functional call-based approach which presents an entirely new synchronization and handshake mechanism. While this mechanism may be able to exist alongside the SCE-MI 1.1 mechanism, it is unclear from the data provided to date, as to how the user will create a heterogeneous SCE-MI-based verification system with SCE-MI 1.1 transactors and transactors based on the proposed function-call-based approach.