

OK initiative

it's OK to develop standards for custom design



Open Kit Initiative Launch
DAC 2003
June 2

I'm OK
You're OK

“but custom design isn't feeling that well”

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Today's Agenda

9:00 Welcome - Nick English

9:10 Problem Statement - Jim Solomon

9:25 Open Kit Initiative - Nick

9:40 Accellera - Vassilios Gerousis

9:55 Q&A and Invitation to Join, Vassilios

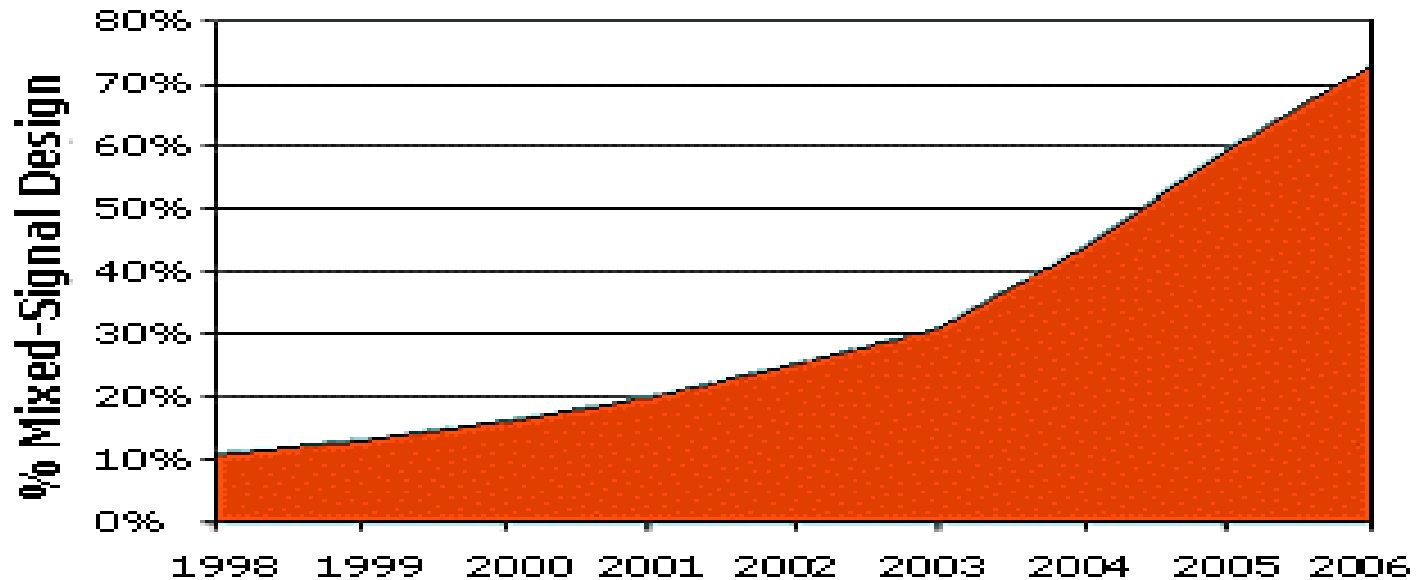
Custom Design Today

OK, so what's the problem?

Jim Solomon

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What is the Market Demanding?



IBS Corp projects that MS-SOCs account for
30% of SOCs in 2003,
DOUBLING to 70% in 2006

Source: Cadence/ IBS Corporation

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What We Need to Meet The Demand

- **Task automation and flow optimization**
- **New, innovative EDA tools**
- **Custom design IP**
- **Reuse of that IP**
- **Rapid access to foundries**

**The direction is known, but
the progress has been slow**

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How are we doing?

- **Productivity**
 - Really, has it improved in 10 years? 20?
- **Automated Design Tools**
 - Still mostly manual today
- **Custom/Analog IP Market**
 - No company with long-term success
- **Standards**
 - Spice? - paper, pencil - word-of-mouth

So What Gives: The Market or The Method?

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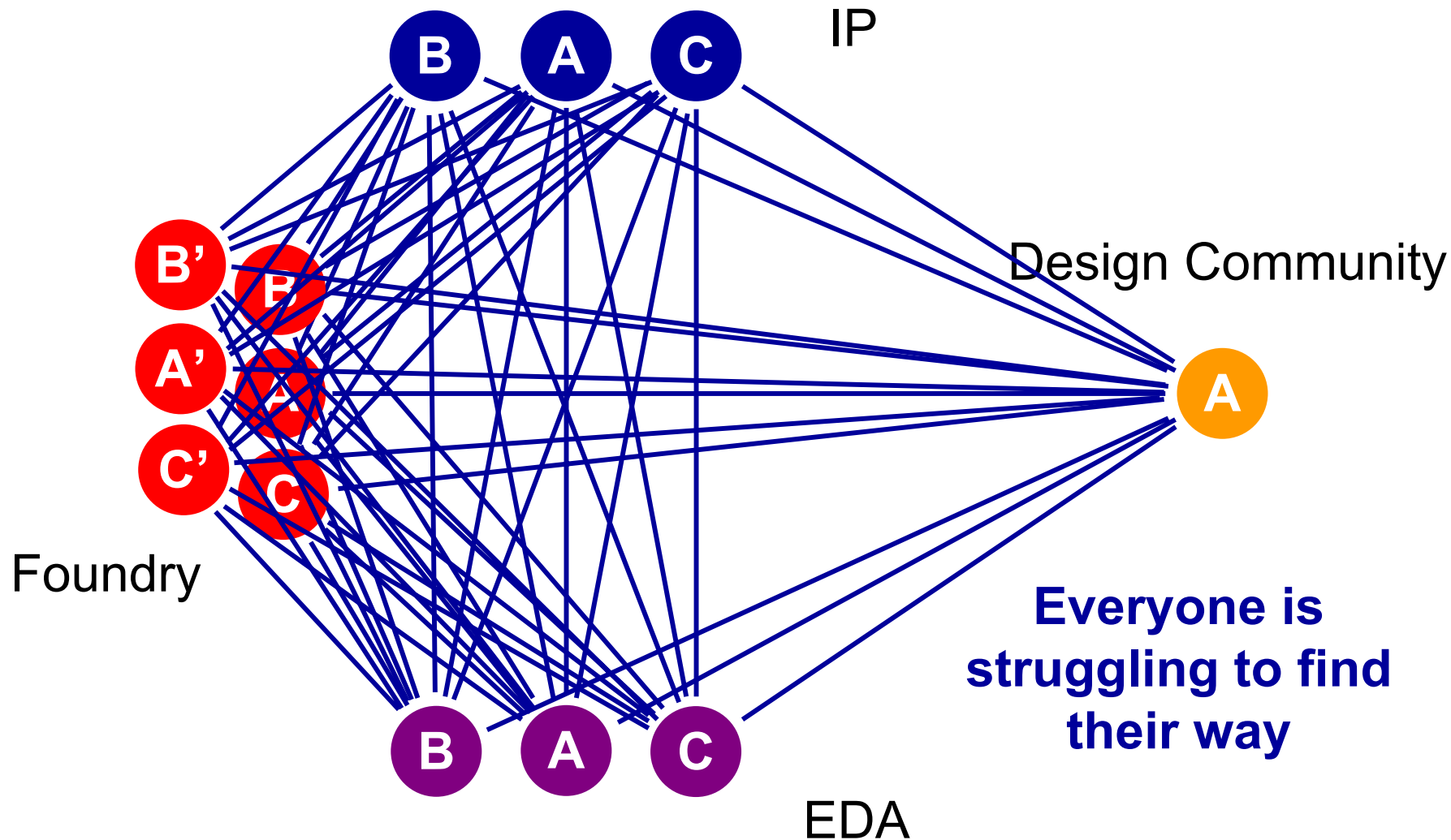
So what's Not OK in Custom Design

	OK	Not OK
Time it takes to integrate design kits		X
Agreement on Design Kit Data		X
Standardized delivery methods		X
Designer's trust of Kit/Tool results		X
Custom IP reuse experiences		X
 "Overall satisfaction in the industry with these elements of the design chain"		 X

**"Now that we share foundries, libraries, and tools,
this stuff matters"**

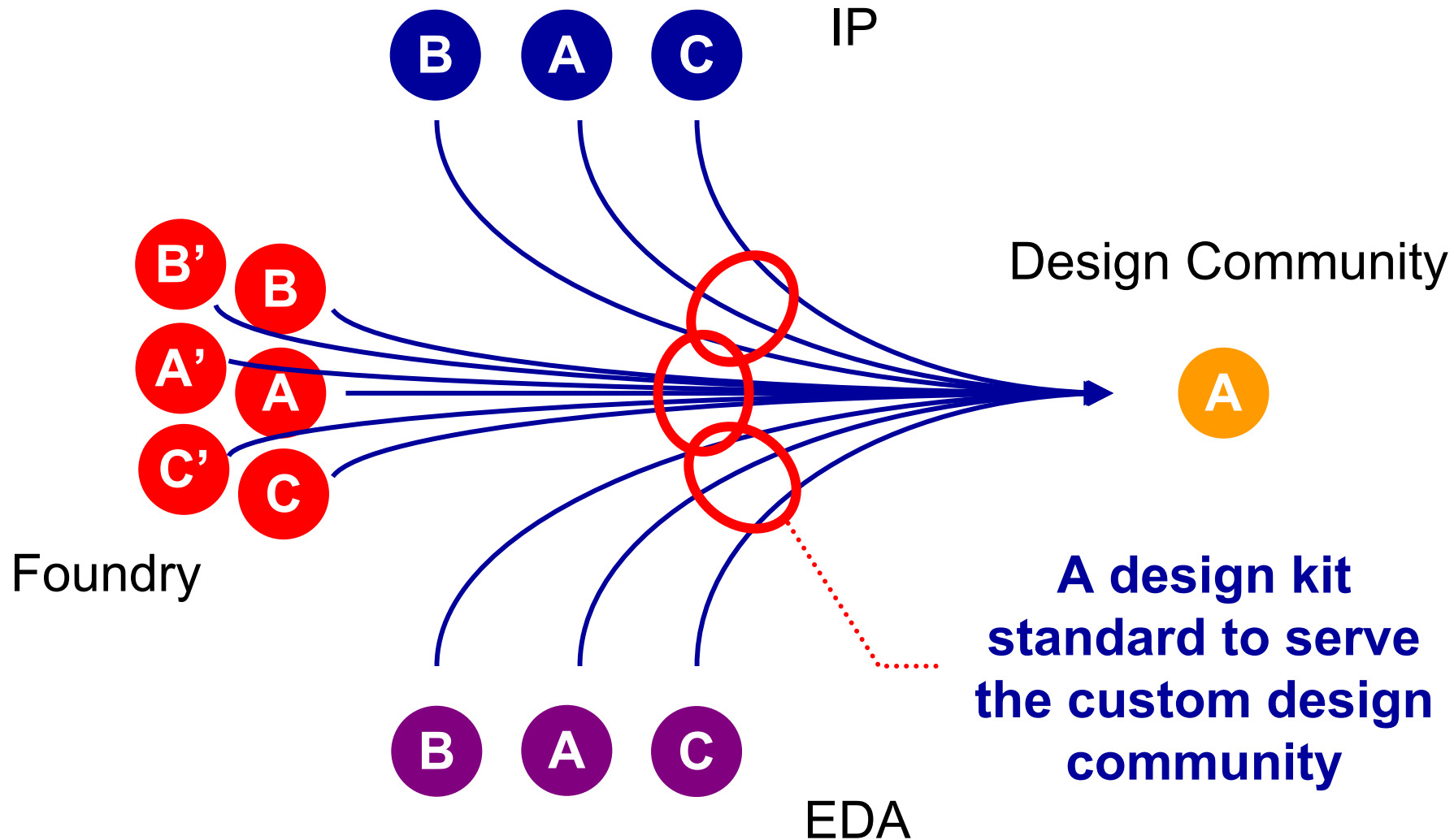
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The 30,000 Foot View: A Jungle



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The 30,000 Foot View: Future



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Silicon World: 5 Basic Components

- **Components**
 - Transistor
 - Diode
 - Res
 - Cap
 - Ind
- **But... Standards?**
 - GDSII?
 - HSPICE?
 - Artist?
 - Calibre?
 - Virtuoso?
 - Cadence PDK?
- **Lack of standards at elemental level**
 - Creates huge inefficiencies
 - Inhibits progress in the custom design world

“We’re proposing a stronger foundation”

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OK!, Here is what we are going to do about it

**Well Nick, I've described the problem, so
how are we going to make it **OK**?**

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OK Objective

Put a Strong Foundation to the IC Design Process

**Reduce Redundant Work by Multiple Companies
and the Inefficiencies and Nuisances**

**Work in Areas of Minimal Competition Between
Vendors**

**Continue Standardization Efforts
That are helping the industry**

Things to work on

- **Design Function, Nomenclature and categories**
- **Design kit elements and formats**
- **Tool & technology fit**
- **Design type and applications**
- **Management of all this stuff**
 - **Ownership**
 - **Qualification**
 - **Revision Control**
 - **Distribution**

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There Is A Way To Go About It

- Isolate **C**omponent from **T**ool from **P**rocess
- Allow **C**, **T**, **P** to advance Independently
- Allow Efficient Commerce in **C** or **T** or **P**
 - Without having to be unduly dependent on one another
- Allow for Exceptions and/or Proprietary IP
- Getting started
 - Outline the entire problem, or as much as we can
 - Simplify that problem to a basic set
 - Do the simple, useful things first

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Who Cares?

- **Designer community**
- **Library & IP developers**
- **Internal DA groups**
- **EDA tool providers**
- **Foundries**

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Benefits to Design Community

- **Fewer mistakes in getting Si out**
- **Less confusion in comparing foundries**
- **More flexibility in choosing tools**
- **Less confusion in comparing tools**
- **Quicker ramp-up of new tool flows**

Benefits to Foundries

- **Fewer Kits to Produce**
- **Faster “bring-up” and easier support of new tool flows**
- **Fewer errors due to versioning and/or compatibility issues**
- **Faster customer adoption of new Kits**
- **Easier to differentiate foundry specialty offerings**

Benefits to Library & IP Developers

- Fewer different elements of the kits to understand and maintain
- Quicker understanding of process differences
- Organized **OK** structures to deal with
 - Common device level foundation
- Easier regression testing of migrated components

Benefits to EDA Companies

- **Speeds new tool adoption/usage/proliferation**
- **Increases value with more of a total solution (tools + standard, i.e. known design kits)**
- **Promotes openness and levels the playing field**
- **Tool writers know what to expect of the data structures and behavior**

Time To Take Action

- Time to find a better way
- Time to stop subscribing to the old beliefs
- Time to establish a foundation that everyone can build on
- Time to empower the Custom IC designer

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Can Accellera Help?

**Well Vassilios, Jim challenged me.
So, let me ask you: How can Accellera
help make it **OK**?**

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Accellera OK Technical Committee



A Proven Standards Approach™

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Accellera Proven Standards

- **Accellera is a business driven standard organization:**
 - **Over 400 technical experts (volunteers).**
 - **Proven standards (Verilog, SDF, ALF, SystemVerilog, PSL, Verilog-AMS, SCE-API, etc.).**
 - **Excellent Technical Standards built with proven donated technology.**
 - **Quick standards for innovative tools.**
 - **Release to IEEE when standards are solid with tools and usage**

Accellera Standard Landscape

Accellera Theme (System To Silicon)

Rosetta (The System Level Language) And Semantics

Property
Specification
Language

PSL 1.01

Open
Verification
Library
OVL

SystemVerilog 3.1
The First HDVL
(Embedded Verification,
Formal Assertion,
Architectural Language,
And C/API Interface)

Verilog-AMS

2.1

High Level
Transaction
For
modeling,
tools,
emulation
and
debuggers

SCE-API
1.0

IEEE ALF library Foundations From RTL to Silicon Modeling

Open Kit (OK)

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Accellera OK Technical Committee

- **Accellera had a kick off meeting to investigate the formation of an Accellera OK Technical Committee.**
- **We developed mission and a set of proposed goals.**
- **All attendees expressed commitment to participate in OK.**
- **The OK Technical Committee Proposal will be presented to Accellera Board for final approval on June 4.**

Open Kit Mission

- **Develop and promote a standard for a design kit to enable and facilitate more efficient and automated custom IC design.**

Proposed Goals/Objectives

- **Build a strong foundation for automated custom IC design**
 - **Standard nomenclatures.**
 - **Interchange format between tools.**
 - **Standard manufacturing manuals**
 - **Device Models**
 - **Layer definitions.**
 - **Netlist and symbols and display files (Color, size, shape, appearance, _)**
 - **Etc.**

Invitation to Join

- **Join the Accellera OK Technical Committee. Join Artisan, AWR, Cadence, Synopsys, Mentor, NEC, and Infineon**
- **Help create the best WG processes**
- **Define the Open Kit roadmap**
- **Begin the OK standard development**

**You can make it
OK!**

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Q&A and Invitation

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Technical Approach

Nick English

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Isolate **Component from **T**ool from **P**rocess**

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Getting started

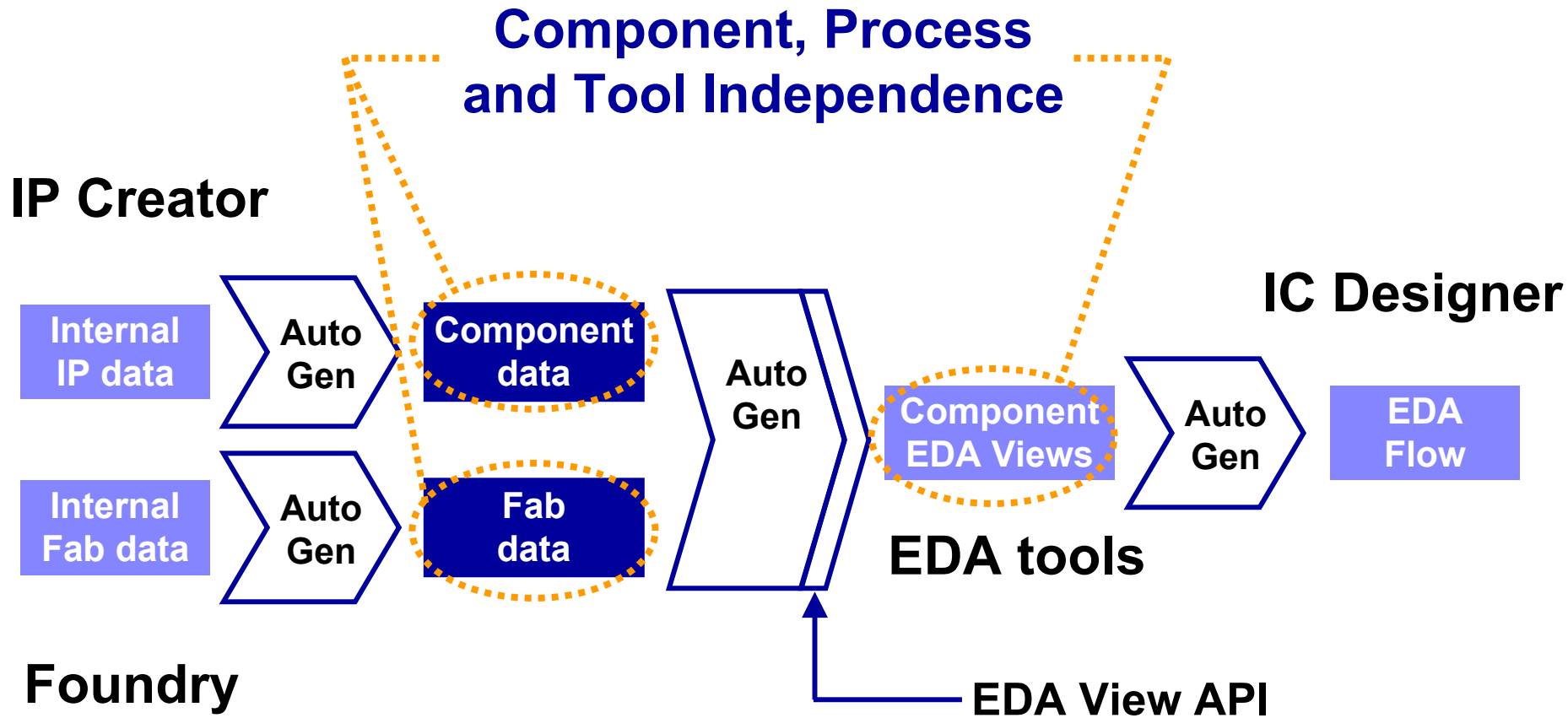
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Standards to Permit Efficient “Value-add”



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Possible Silicon-Level Standards

- **Standards to document...**
 - **Spice Model**
 - **DRC rules**
 - **LVS rules**
 - **Extraction (device/interconnect) rules**
 - **Process Layers**

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Possible Component-Level Standards

- **Standards to document....**
 - **Device name**
 - **Device type: nfet, pfet, diode, etc**
 - **Symbol graphic**
 - **Parameter and Corner methods**
 - **Layout functions**
 - **Electrical and physical relationships**

Organize OK 4-D Table

Design Function Categories	Kit Elements				Vendor's Tools & Technologies					Design Types		

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OK 4-Dimensions

1. Design Functions & Data-Base Categories

- Process, Device, Circuit simulation, Physical Implementation and Verification, Extraction, etc.

2. Design Kit Elements

- Hierarchical Elements of Data
 - Transistor Level data, Models, DR., DRC, LVS, Interconnect, Electrical and Topology data, etc.
 - Tool-Dependent Elements
 - Tool-Independent Elements

3. Vendor's Tools & Technologies

- EDA, Foundry, Library, IP Vendors

4. Design Types and Applications

- Custom Digital, Mix-Sig., Analog, RF
 - Level 1, 2, etc.

Sample OK 4-D Table, Complex..!

Design Function & Data Base Category	Design Kit Elements	Design Kit Elements	Design Kit Elements	Design Kit Elements	Design Kit Elements	Vendor's Tools & Technology	Vendor's Tools & Technology	Vendor's Tools & Technology	Vendor's Tools & Technology	Vendor's Tools & Technology	Vendor's Tools & Technology	Vendor's Tools & Technology	Etc.
	Hierarchy-1	Hierarchy-2	Hierarchy-3	Hierarchy-4	Etc.	Synopsys	Mentor	Artisan	AWR	Cadence ?	IBM ?	TSMC ?	Etc.
Process & Device Simulation													
	Process	SEM Data				Taurus-Process							
		Doping Profile				"							
		Lateral Dim. Vertical Dim.				"							
	Device	CMOS	I-V Data	Ids-Vds	Sweep 0-2v, steps 0.1v	Taurus-Device, Aurora							
	Interconnect	Cross-Sections Topology				Raphael							
		Vertical				"							
		GDSII Files				"							
	Environment, Data-Base					Taurus-Workbench							
Circuit Simulation													
	CMOS Models	BSIM3.3	Global	Typical		HSPICE, NanoSim, StarSim	Edo, etc.						
				Corner		"							
			Binned	Typical		"							
		BSIM4-RF	Global	Typical		HSPICE-RF							
			Corner										
	Diode Models	Typical				HSPICE, NanoSim, StarSim							
	Resistors Models	Poly, Metal				"							
	Capacitors Models	MIM				"							
	Inductors models	Spiral				"							
Physical Implementation													
	P-Cells	Language	TCL			COSMOS-LE							
		Display Files	Skill										
	Place & Route Tech. Files	Routing				Apollo,							
		Rules Files				Astro							
Physical Verification													

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Let's Simplify The Goal

Step 1: For all participants to agree on a first level **Open Kit** for Custom Digital Design

Step 2: Identify Tool-Dependent, Tool-Independent, and Tool-Dependent-Abstracted components (**TD**, **TI**, **TDA**) and decide what to do about each of them

Step 3: When we succeed here, we will proceed to the next level...

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Basic OK 3-D Table, much simpler & more manageable

Design Function & Data Base Category	Design Kit Elements	Design Kit Elements	Design Kit Elements	Design Kit Elements	Design Kit Elements	Digital Custom DESIGN
	Hierarchy-1	Hierarchy-2	Hierarchy-3	Hierarchy-4	Etc.	Standard Level-1
Process & Device Simulation						
	Interconnect	Cross-Sections Topology				TI
			Vertical			TI
			Lateral			TI
		SEM Data				TI
		Dielectric Constants				TI
		Resistivity				TI
		GDSII Files				TI
Circuit Simulation						
	CMOS Models	BSIM3.3	Global	Typical		TDA
				Corner		TDA
			Binned	Typical		TDA
				Corner		TDA
		MOS-9	Typical			TD
			Corner			TD
		MOS-11	Typical			TD
			Corner			TD
	Diode Models	Typical, Corners				TI
		ESD	Typical, Corners			TI
	BJT Models	GP	Typical, Corners			TI
	Resistors Models	Poly	Typical, Corners			TI
		Metal	Typical, Corners			
	Capacitors Models	Typical, Corners	Typical, Corners			TI
Physical Implementation						
	P-Cells	Device, Cell Lib	CMOS			TDA
			BJT			TDA
			R	Poly, etc.		TDA
			C	MIM Cap., etc.		TDA
	Layout Tech. File	Layer Mapping				TI
		Display Files				TI
		Cell GDSII				TI
	Schematic Tech. Files	Symbols	Attributes			TI
		Display Files				TI
	Place & Route Tech. Files	Routing Rules Files				TI
			Antenna			TI

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Proposed Custom Digital Design, OK Level-1

1. Agree on **TI** kit elements
2. Analyze and agree on the **TDA** kit elements. This may require a technical Working Group to develop an abstraction in order to convert or translate the incompatible parameters to a set of new compatible parameters.
 - This may require generation of an automatic conversion / translation utility or code by the Working Group
3. Agree on **TD** kit elements and decide how many different versions of design kits are necessary to be proposed by the Working Group

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OK Management Issues

1. Ownership

- Who owns the “Darn” thing ?

2. Qualification

- EDA-Foundry
- Library-Foundry
- Designer-Foundry

3. Revision Control

- Tool, Process, Library Synchronization

4. Distribution

- Web-Base Accounts
- Automatic Releases
- Schedule Releases

Remember

Outline the entire problem, or as much as we can

Simplify to a basic set

Do the simple things first

And then proceed...

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Thank you



Nick English