

# **VHDL Basics**

**RASSP E&F Module Number: 10**

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**Abstract:** The Basic VHDL module is an introduction to the VHSIC Hardware Description Language and its fundamental concepts. VHDL is a language specifically developed to describe digital electronic hardware and its attributes. VHDL is a flexible language and can be applied to many different design situations. This language has several key advantages, including technology independence and a standard language for communication. The module describes many of the advantages of using VHDL and a short history of the language.

As an introduction to the language, a small design example is shown. This example shows three different methods of describing the hardware. The module then introduces three key models of hardware in VHDL: behavior, structure, and time. These models are important aspects of VHDL and must thoroughly understood. Several basic VHDL constructs are shown next. The module describes the basic data types and objects available to the designer. Builtin data types include integers, floating point numbers, and many others. The designer also has variable, signal, and constant objects available. The difference between sequential and concurrent statements is also explained. The basic VHDL design units, the entity and the architecture, are described in detail. Furthermore, VHDL supports code reuse through its packages and libraries. Finally, the basic operators and attributes of the data types and objects are shown.

The Basic VHDL module concludes with a small but comprehensive design example to illustrate many of the constructs introduced in the earlier sections of the module. Large examples are provided in the later modules. The focus of this module is to introduce the basic features of this language and to provide brief examples of its use.

### **Module Objectives:**

The introduce VHDL such that students can describe and simulate simple digital circuits using VHDL.

### **Specific Objectives:**

The student shall comprehend and apply:

- 1) The purpose of VHDL.
- 2) The overall structure of VHDL
- 3) The VHDL development and execution sequence
- 4) The VHDL simulation cycle
- 5) Basic VHDL object types and declarations
- 6) The syntax and semantics of basic VHDL sequential statements
- 7) The syntax and semantics of basic VHDL concurrent statements
- 8) VHDL modeling techniques for the simulation and evaluation of gate-level digital circuits.

### **Prerequisites:**

**Prerequisite Modules:****Prerequisite Knowledge Aside from Modules:**

Working knowledge of digital logic design particularly at the gate level.

Some experience in programming will be helpful.

**Syllabus:**

- |   |           |
|---|-----------|
| 1) Introduction   | (10 Min.) |
| 2) VHDL Design Example                                  | (15 Min.) |
| a) Simple Introductory Design                           |           |
| 3) VHDL Model Components                                | (30 Min.) |
| a) Entity Declarations                                  |           |
| b) Architecture Descriptions                            |           |
| c) Timing Model   |           |
| 4) Basic VHDL Constructs                                | (80 Min.) |
| a) Data Types   |           |
| b) Objects  |           |
| c) Sequential and Concurrent Statements                 |           |
| d) Entity and Architecture Declarations                 |           |
| e) Packages and Libraries                               |           |
| f) Attributes   |           |
| g) Predefined operators                                 |           |
| 5) Examples   | (20 Min.) |
| a) Review of Module Material via Comprehensive Examples |           |
| 6) Summary  | (5 Min.)  |

**Infrastructure:**

VHDL compiler and simulator, such as Mentor Graphics QuickVHDL or Veribest VHDL Simulator

**Lab Materials:**

A laboratory guide and instructions for using the VHDL simulator.