Structural VHDL

RASSP E&F Module Number: 11

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Abstract: The Structural VHDL module describes the use of VHDL for describing models in terms of component instantiations and interconnections. Structural VHDL can be appropriate at any level of design. For example, testbenches for completed components are often described using structural VHDL. Furthermore, structural VHDL supports the use of libraries and component reuse. The various mechanisms available in VHDL to incorporated predefined components into a VHDL description are presented. The use of idealized local 'components' is described as well as generate statement to create regular structures easily (e.g. RAM, ROM). Additionally, this module shows how VHDL supports libraries and component reuse. Components in structural VHDL are fully described outside the architecture, most often in component libraries. Configuration of these components involves selecting an entity and architecture for the component and specifying parameters for the component. The module concludes with comprehensive example to illustrated much of the material covered in the early sections.

Module Objectives:

To introduce the concepts and constructs supporting structural modeling in VHDL such that students can create models reusing predefined VHDL component descriptions.

Specific Objectives:

The student shall comprehend and apply:

1) The VHDL components instantiation mechanism
2) VHDL generate statements
3) VHDL structural modeling techniques

Prerequisites:

Prerequisite Modules:

Module 10, VHDL Basics

Prerequisite Knowledge:

Working knowledge of digital logic deqign particularly at the gate level. Some experience in programming will be helpful.

Syllabus:

1) Introduction	(10 Min.)
2) Incorporating VHDL Design Objects	(35 Min.)
3) Generate Statement	(15 Min.)
4) Examples	(25 Min)

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5) Summary (5 Min.)

Infrastructure:

VHDL compiler and simulator, such as Mentor Graphics QuickVHDL or Veribest VHDL Simulator

Lab Materials:

A laboratory guide and instructions for using the VHDL simulator

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