Behavioral VHDL

<u>RASSP E&F Module Number:</u> 12

Abstract: The Behavioral VHDL module describes features of the language that describe the behavior of components in response to signals. Behavioral descriptions of hardware utilize software engineering practices and constructs to achieve a functional model. Timing information is not necessary in a behavioral description, although such information may be included easily.

The VHDL process construct is described first. Processes run code sequentially. The statements allowed in a process, referred to as 'sequential' statements, are listed in the module. Subprograms are another behavioral construct; they support code reuse description simplification. One use of subprograms is in bus resolution functions which allow the description of buses with multiple signal drivers. A discussion of packages is also included. Packages can contain subprograms descriptions, custom data types, and numerous other VHDL model fragments that a designer may wish to reuse easily. Finally, the module describes the use of testbenches and lists some problems to avoid in VHDL.

The Behavioral VHDL module ends with a comprehensive example using the quicksort routine. Although a detailed understanding of the algorithm implemented by this routine are not important for a full understanding of the VHDL constructs presented in this module, the example serves as a vehicle for highlighting many of the VHDL features presented in this module. The model also illustrates the similarity between process-oriented VHDL descriptions and other general-purpose high-level programming languages.

Module Objectives:

To introduce the concepts and constructs supporting behavioral descriptions in VHDL such that students can create models with complex behavior with VHDL.

Specific Objectives:

The student shall comprehend and apply:

1) VHDL Processes
2) VHDL sequential statements
3) VHDL packages
4) VHDL modeling techniques for the simulation and evaluation of behavioral-level digital circuits.

Prerequisites:

Prerequisite Modules:

Module 10, VHDL Basics

Prerequisite Knowledge:

Student must have a working knowledge of digital design particularly at the behavioral level.

Some experience in programming is required.

Syllabus:

1) Introduction (10 Min.)

2) Behavioral Modeling (75 Min.)
   a) Processes
   b) Sequential Statements
   c) Packages
   d) Problems to Avoid

3) Examples (40 Min.)
   a) Description of SDSP Microprocessor
   b) Models of the SDSP

4) Summary (5 Min.)

Infrastructure:

VHDL compiler and simulator, such as Mentor Graphics QuickVHDL or Veribest VHDL Simulator

Lab Materials:

A laboratory guide and instructions for using the VHDL simulator