Advanced Concepts in VHDL

RASSP E&F Module Number: 13

Abstract: The Advanced Concepts in VHDL module spans a wide range of topics, including several that may be applied to higher levels of design abstraction. Many of these constructs will have been introduced in the first three VHDL modules in this sequence, but this module covers them more comprehensively. Examples of such constructs include signal assignment statements, and the capabilities and differences when they are used as concurrent VHDL statements or sequential VHDL statements. Similarly, the VHDL procesq is discussed in more detail than in earlier modules. It should also be noted that TEXTIO and shared variables are introduced in this module.

Two illustrative examples showing the use of many of the constructs discussed are provided. The first example shows the implementation of a simple Abstract Data Type implemented with custom VHDL data type and subtype declarations and overloading operators to manipulate signals and variables of those VHDL types. The second example, based on the University of Virginia's ADEPT system, shows the use of records and subprograms (including a Bus Resolution Function) to implement a simple performance-oriented model using VHDL.

Module Objectives:

To provide a deeper understanding of the capabilities of some of the VHDL constructs introduced in the first three VHDL modules in the E&F sequence and to introduce some additional constructs that facilitate the description of complex and/or abstract models.

Prerequisites:

Prerequisite Modules:

VHDL Basics, Module 10
Structural VHDL, Module 11
Behavioral VHDL, Module 12

Prerequisite Knowledge:

Student must have a strong working knowledge of VHDL at all levels of abstraction. In addition, the student must have a working knowledge of digital design, particularly at the behavioral level, and some experience in programming is required.

Syllabus:

1) Introduction (5 Min.)

2) Revisiting Some VHDL Constructs (70 Min.)
   a) Aliases
   b) Foreign Interfaces
   c) TEXTIO
   d) Assert Statements
   e) Processes

f) Signal Assignment Statements
g) Shared Variables

3) Examples (40 Min.)
a) Abstract Data Type Example
b) Example from UVA ADEPT

4) Summary (10 Min.)

Infrastructure

VHDL compiler and simulator, such as Mentor Graphics QuickVHDL or Veribest VHDL Simulator

Lab Materials:

A laboratory guide and instructions for using the VHDL simulator