Scheduling & Assignment for DSP

RASSP E&F Module Number: 22

Module Objectives:

To educate the designer on the concepts and methods used to schedule and assign DSP algorithms to processors.

Prerequisites:

Prerequisite Modules:

None

Prerequisite Knowledge:

None

Syllabus:

1) Fully Specified Flow Graphs (FSFGs) (15 Mins)
   a) Representation of DSP Algorithms
   b) Difference between DSP and general-purpose algorithms
   c) Examples of FSFGs
2) Measures of Performance (5 Mins)
   a) Sample Period
   b) Latency
3) Retiming (15 Mins)
   a) Cut-Sets
   b) Time Scaling
   c) Nodal Transfer
   d) Legal Retiming and Systolic FSFGs
   e) Delay Transfers

4) Iteration Period and Iteration Period Bounds (10 Mins)
   a) Iteration Period and Delays in a loop
   b) Iteration Period Bound (IPB)
   c) Review of Approach
5) Formal Methods for FSFGs (10 Mins)
   a) Non-overlapping Static Schedule
   b) Overlapping Static Schedule
   c) Cyclo-static Schedule
6) Perfect Rate FSFGs and Unfolding (10 Mins)
   a) Perfect Rate FSFGs
   b) Unfolding
   c) Examples
   d) Optimum Unfolding
7) Lookahead (5 Mins)
   a) Lookahead and the IPB
   b) Examples
   c) Lookahead and Hardware cost
8) Scheduling Approaches (5 Mins)

a) Taxonomy of Scheduling approaches
b) Comparison of Scheduling Algorithms

9) Optimal Scheduling & Assignmen (20 Mins)
a) IPB Model
b) FR Model
c) Communications Cost
d) Multi-processor System for a 2nd Order IIR Filter
e) RCC Model
f) Memory and Registers
g) Comparison of Processor Mapping Models

10) Conclusions

Audience:

System design engineer, digital design engineer, first year graduate student.