

Virtual Prototyping using VHDL

RASSP E&F Module Number: 32

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Audience: System design engineer, digital design engineer, first year graduate student.

Module Objectives:

To educate the designer on the concepts, methods, and standards used for virtual prototyping of systems using the VHSIC Hardware Description Language (VHDL).

Specific Objectives:

Provide information on:

- 1) Introduction and definition of terms used for virtual prototyping
- 2) Description of the virtual prototyping process
- 3) Virtual prototyping as a part of the RASSP methodology
- 4) Abstraction levels and limitations of virtual prototyping
- 5) Using VHDL executable requirements in the virtual prototyping process

- 6) The role of VHDL executable specifications in the virtual prototyping process
- 7) Data and control flow modeling in the RASSP design process
- 8) VHDL performance modeling within the methodology
- 9) Where VHDL hybrid modeling fits in the RASSP process
- 10) Designing behavioral models in VHDL for system simulation
- 11) Design example of a single processor system with a VME bus interface
- 12) Relevant Documents and Standards for Virtual Prototyping

Prerequisites:

Prerequisite Modules:

RASSP Methodology Overview

Prerequisite Knowledge:

VHDL Modules 12 and 13

Syllabus:

- 1) Introduction and definition of terms used for VP (30 Min.)
- 2) Description of the virtual prototyping process (20 Min.)
 - a) Goals and scope of virtual prototyping
 - b) The RASSP process and its reliance on virtual prototyping
- 3) Abstraction levels and scope of virtual prototyping (5 Min.)
- 4) The virtual prototyping process (175 Min.)
 - a) Executable requirements in VHDL
 - b) Executable specifications in VHDL
 - c) Data/control flow modeling in the VP process
 - d) VHDL Performance modeling in the VP process
 - e) Hybrid modeling techniques
 - f) VHDL Full behavioral modeling and detailed design
 - i) Design example overview
 - ii) Processor modeling
 - iii) Testbench modeling
 - iv) Testing a model
 - v) Memory controller modeling
 - vi) Memory modeling
 - vii) VME interface model
- 5) Relevant Documents and Standards (5 Min.)
- 6) Summary (5 Min.)