Test Technology Overview

RASSP E&F Module Number: 43

Abstract: This module is intended to provide an overview of digital systems testing to the general design engineer. The module contains basic information on the fundamentals of testing including motivation, current practice, and basic fault modeling techniques. The basic algorithms for test generation and fault simulation for both combinational and sequential designs are then covered followed by a presentation of the theory of IDDQ testing.

The design for test section begins with an overview of standard DFT techniques like scan and LSSD. This material is followed by a presentation of boundary scan. Included in this section are descriptions of boundary scan cells, the boundary scan chip and board level architecture, and the boundary scan test modes. The final material in this section covers Built-in Self-test(BIST). The theory of Linear Feedback Shift Registers for pseudorandom test generation and signature analysis is outlined followed by a presentation of their implementation and use in BIST. A test case of the use of BIST in a DSP datapath is presented. Finally, autonomous BIST and Electronic Systems Test Automation (ESTA) are discussed.

The final sections present material on the inclusion of design for test techniques in the overall design process. The first section covers hierarchical design for test. This is followed by a presentation of synthesis for test which covers not only the insertion of

DFT structures into designs during synthesis, but also automatic construction of an entire test suite for a design. Next, the IEEE and DOD standards that govern the inclusion of test into designs are presented. This includes the IEEE Boundary Scan and MTM standards, and the WAVES standard. The concluding section presents some real-life examples of industrial design flows which include design for test.

Module Objectives:

To educate the general digital systems designer on the fundamentals of test technology in a manner that will assist him/her in designing testable systems.

Specific Objectives:

Provide information on:

1) Fault Models
2) Design for Testability (DFT) Techniques
3) Build-In Self Test Techniques
4) The design trade-offs inherent in the use of the above techniques

Prerequisites:

Prerequisite Modules:

None

Prerequisite Knowledge:

Fundamentals digital logic design, both combinational and sequential.

Outline:

1) Introduction	(7 slides)
2) Fault Modeling	(14 slides)
3) Test Generation	(7 slides)
4) Automatic Test Pattern Generation Algorithms	(13 slides)
5) Fault Simulation Algorithms	(16 slides)
6) IDDQ Testing	(9 slides)
7) DFT Techniques	(20 slides)

a) Ad Hoc Techniques
b) Structured Techniques

8) Built-In Self-Test (25 slides)
a) Test Generation Techniques for BIST
b) Signature Analysis
c) BIST Case Study

9) Hierarchical Design for Test (3 slides)

10) Synthesis for Test (5 slides)

11) DFT Standards (15 slides)
a) IEEE 1149.1
b) IEEE 1149.1b
c) 1149.5
d) MIL-HDBK-XX47

12) Design flows with DFT (14 slides)

13) Summary (1 slide)

14) References (2 slides)

Infrastructure:

NA

Lab Material:

NA