Cost Modeling for Embedded Digital Systems Design

RASSP E&F Module Number: 57

Abstract:
Designers of high-end embedded systems or large volume consumer products are faced with the challenge of rapidly prototyping designs which meet stringent electrical specifications along with tight physical constraints, under restrictive system engineering constraints such as cost time to market (TTM) and resource limitations. The goal is to design a minimum cost system, with consideration of lifecycle costs, as opposed to a minimum cost hardware system. This module describes a new RASSP design methodology called Cost Modeling and its application to the embedded digital system design process. A detailed case study and a thorough description of hardware and software cost estimators are presented.

Module Objectives:
To provide a thorough understanding of cost estimators for hardware and software and their application in the RASSP design process towards the optimal design of embedded digital systems. The techniques are illustrated through a detailed case study.

Prerequisite Modules:
RASSP Methodology Overview

Prerequisite Knowledge:
Fundamentals of digital: logic design; digital chip, electronic CCAs, and signal processing systems: design, manufacturing, support and disposal.

Outline:

1) Introduction to Cost-Modeling Based System Design (30 minutes)
   a) Limitation of Design Process
   b) Impact of resource constraints
   c) Effects of system development time
   d) Cost modeling in early stages of design.

2) Software Cost Estimation Process (20 minutes)
   a) Software lifecyle models
   b) Basic steps in cost estimating.

3) Parametric Software Cost Models (45 minutes)
   a) COCOMO
   b) REVIC
   c) COCOMO 2.0

4) Parametric Hardware Cost Models (45 minutes)

   a) Full custom
   b) Gate array
   c) FPGA

5) Application of Cost Modeling to RASSP Design Process (30 minutes)

6) Summary and Results (10 minutes)

Infrastructure:
A cost modeling tool with associated optimization packages.

Laboratory Material:
A laboratory has been created both for a simple architecture.