Performance Modeling using VHDL

RASSP E&F Module Number: 59

Abstract: This module is intended to present the area of system level performance modeling using VHDL. The first section of the module includes a background of performance modeling including the objectives of performance modeling and definitions of common performance modeling terms. Techniques for performance modeling such a Petri Nets, queueing models, and uninterpreted models are covered along with how simulation based performance modeling is implemented in VHDL.

The second section of the module presents current environments that are available for performance modeling in VHDL. This includes a presentation of the techniques that they employ as well as the libraries of modules that they include. This section is followed by a presentation of several VHDL based performance model examples. These examples illustrate the metrics that can be analyzed using VHDL based performance modeling as well as the features of the environments under which the examples were constructed.

Finally, the module includes a presentation of mixed level modeling. Mixed level modeling is the capability of constructing and simulating models that contain both

uniterpreted system level components and interpreted behavioral level components. Mixed level modeling allows the step-wise refinement of performance models into implementation models. Techniques for mixed level modeling are presented as well as examples that illustrate the benefits of mixed level modeling.

Module Objectives:

To educate the general digital systems designer on the goal and benefits of performance modeling, how performance modeling is done using VHDL, and what environments are available to automate the creation and analysis of VHDL based performance models.

Specific Objectives:

Provide information on:

1) Performance modeling objectives and definitions
2) Performance modeling using VHDL
3) VHDL based performance modeling environments
4) Performance modeling examples
5) Hybrid modeling objectives
6) Hybrid modeling using VHDL
7) Hybrid modeling examples

Prerequisites:

Prerequisite Modules:

VHDL modules

Prerequisite Knowledge:

Familiarity with the need for system level modeling
VHDL.

Outline:

1) Performance Modeling Introduction (30 slides)
   a) Goals and Motivation
   b) Definitions
   c) Performance Modeling in the Design Process
   d) Metrics
2) Performance Modeling Theory (42 slides)
   a) Queuing models

b) Petri Nets
c) Uninterpreted Models

3) Non VHDL-Based Performance Modeling Tools (35 slides)
4) Techniques for performance modeling using VHDL (8 slides)
   a) Hardware Performance Models
   b) Task Level HW/SW Codesign Performance Models
5) VHDL-Based Performance Modeling Tools (54 slides)
   a) ADEPT
   b) Viewlogic EArchitect
      Honeywell PML
   c) LMC ATL Performance Modeling Library
6) VHDL Performance Modeling Examples (30 slides)
7) Mixed Level Modeling (19 slides)
   a) Mixed Level Modeling Objectives
   b) Mixed Level Modeling Approaches
   c) Examples
8) Summary (1 slide)
9) References (1 slide)

Infrastructure:

Mentor Graphic's Design Architect
UVa ADEPT Performance Modeling Tools
VHDL 1076-87 simulation environment
ATL timeline analysis tools

Lab Material:

ATL Performance Modeling Lab