Basic WAVES

RASSP E&F Module 61

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Abstract:
The *Basic WAVES* module discusses the basic idea of a VHDL testbench, and its use in the design process. As part of the testbench discussion, the standard for VHDL Waveform and Vector Exchange (WAVES) - IEEE Std 1029.1 1996 - is introduced as a methodology for describing the input stimulus to be applied to the Unit Under Test (UUT) and the expected outputs which are compared to the actual outputs in the testbench. The module covers all the basic WAVES concepts, which include the WAVES libraries and functions, the WAVES test vector file format, and the WAVES test set.

Specific Objectives:

Provide information on:

1. Testbench Development
2. Design Verification Challenges
3. WAVES Concepts
4. WAVES Constructor Library and Built-Ins
5. WAVES External File
6. WAVES Test Set

7. Decoder Example
8. Algorithmic Waveform Generator Example

Prerequisites:

Prerequisite Modules:

VHDL modules 10-13 & 43.

Prerequisite Knowledge:

Familiarity with testing in VHDL.