esa estec
european space research
and technology centre

WDN/PS/822
Issue 2
January 1995

Support Component List

Components for Spacecraft Electronics

Prepared by P. Sinander

Spacecraft Control and Data System Division (WS)
Keplerlaan 1 - Noordwijk - The Netherlands
Mail address: Postbus 299 - 2200 AG Noordwijk - The Netherlands
Tel: +31-1719-83667 - Telex: 39098 - Cables: Spaceurop, Noordwijk - Fax: +31-1719-84295

Page intentionally left blank

Table of contents

1 INTRODUCTION

1.1 Purpose

This document is a compilation of information concerning components for spacecraft electronics. The purpose of making this information available to designers is to promote existing components and to facilitate the selection of components for new designs.

Using an existing component instead of designing a new one with similar functionality will often reduce cost, schedule and risk. This applies particularly when the existing component is qualified and/or has already been successfully used in flight. Furthermore it has been shown in the past that different component variants supposedly implementing the same functionality can have some incompatibilities. The trade-off between designing a new project-specific component versus using an existing one has to be evaluated in each case.

This document has been organised in four main sections:
- Existing flight components;
- Flight components under development;
- Demonstration designs;
- Company addresses and contact persons.

1.2 Scope

The scope of this document is components for spacecraft electronics available from European sources.

Only components generally available to the space industry should be included, and the companies listed as a component source have been asked to confirm. Nevertheless, it is imperative that the designer verifies the actual availability, price and conditions before deciding to use a particular component.

A selection of which components to be included in this list has been performed, for example components with low complexity have not been included.

1.3 Disclaimer

While the information presented here is believed to be correct, all information is provided *as is*; there is no warranty that the information is correct or suitable for any purpose, neither implicit or explicit.

This document does not necessarily reflect the policy of the European Space Agency.

2 EXISTING FLIGHT COMPONENTS

This section includes components that at the date of issue have been manufactured, tested and delivered at least as prototypes. The status for characterisation, ESA/SCC qualification and lead times for flight quality components may vary.

2.1 MA31750: 16-bit MIL-STD-1750 processor

Single chip MIL-STD-1750A/B 16-bit instruction set architecture processor, A or B version selectable. Performance 2 DAIS Mips at 16 MHz. Address space: 2 x 64 kword without MMU, 1 Mword (A mode) or 8 Mword (B mode) with MA31751 MMU. Features include console mode, timers, fault and interrupt handling. Current *Mark I* iteration is I, current *Mark II* iteration is N.

- Devices and functional support available from GPS as for a standard component;
- Complete data sheet and application notes distributed by GPS;
- VHDL model for board-level simulation under development;
- Package: 84 pin PGA and 84 pin CQFP with 50 mil lead pitch;
- Process: GPS S1.5F 1.5µ shrink CMOS/SOS. 300 kRad total dose guaranteed, low SEU sensitivity, latch-up free;
- ESTEC contact: A. Pouponnot (WSD).

2.2 MA31751: Memory Management Unit for the MA31750 processor

MIL-STD-1750A/B compatible MMU, configurable as MMU and/or Block Protect Unit (BPU). 1 Mword physical address space with write/execute protection of 4 kword blocks as MMU. Protection of 1 kword blocks and global write protection during initialisation as BPU. Up to 16 devices can be used in a 1750B system. Supports DMA. Current *Mark I* iteration is A, current *Mark II* iteration is B (iteration C is foreseen).

- Devices and functional support available from GPS as for a standard component;
- Complete data sheet and application notes distributed by GPS;
- VHDL model for board-level simulation under development;
- Package: 68 pin PGA and 68 pin CQFP with 50 mil lead pitch;
- Process: GPS 1.5µ CMOS/SOS (shrink for the C iteration). 300 kRad total dose guaranteed, low SEU sensitivity, latch-up free;
- ESTEC contact: A. Pouponnot (WSD).

2.3 MA31755: 16-bit EDAC for the MA31750 processor

Fast feed-through (35 ns) 16-bit operation with 6 check bits. Error corrected/ uncorrectable flags. High drive capability.

- Devices and functional support available from GPS as for a standard component;
- Complete data sheet distributed by GPS;
- VHDL model for board-level simulation available;
- Package: 68 pin PGA and 68 pin CQFP with 50 mil lead pitch;
- Process: GPS 1.5µ CMOS/SOS. 500 kRad total dose guaranteed, low SEU sensitivity, latch-up free;
- ESTEC contact: A. Pouponnot (WSD).

2.4 54HSC/T630: 16-bit EDAC

Corrects single-bit errors, detects double-bit errors. Low power. Generates check codes for write in 60 ns, flags read error in 30 ns. All inputs & outputs TTL & CMOS compatible.

- Devices and functional support available from GPS as for a standard component;
- Complete data sheet distributed by GPS;
- Package: 28 pin ceramic DIL and 28 pin flat pack with 50 mil lead pitch;
- Process: GPS 2.5µ CMOS/SOS gate array. 300 kRad total dose guaranteed, low SEU sensitivity, latch-up free;
- Within the ESA/SCC Capability Domain.

2.5 16-bit flow-through EDAC

16-bit flow-through EDAC with double system ports and selectable 6-bit or 8-bit syndrome, the 8-bit syndrome allows detection of chip errors for byte-wide memories. Write time 30 ns, read time 40 ns.

- Designed by Saab Ericsson Space, licensed to MHS for use by the space industry (not confirmed by MHS);
- Package: 100 pin CQFP with 25 mil lead pitch;
- Process: MHS 1.0µ CMOS/EPI gate array MC-RT5K;
- ESTEC contact: A. Pouponnot (WSD).

2.6 MA28151, MA8251: Serial Communication Interface

Based on the Intel 8251 USART. Synchronous and asynchronous operation, 5-8 bit characters.

- Devices and functional support available from GPS as for a standard component;
- Complete data sheet distributed by GPS;
- Package: 28 pin ceramic DIL, 48 pin CLCC and 68 pin CQFP with 50 mil lead pitch;
- Process: GPS 2.5µ CMOS/SOS standard cell. 300 kRad total dose guaranteed, low SEU sensitivity, latch-up free;
- Within the ESA/SCC Capability Domain.

2.7 MA28155, MA8255: Parallel I/O device

Based on the Intel 8255 parallel I/O device. 24 programmable I/O, direct bit Set/Reset. Fully TTL compatible.

- Devices and functional support available from GPS as for a standard component;
- Complete data sheet distributed by GPS;
- Package: 40 pin ceramic DIL and 44 pin CLCC;
- Process: GPS 2.5µ CMOS/SOS standard cell. 300 kRad total dose guaranteed, low SEU sensitivity, latch-up free;
- Within the ESA/SCC Capability Domain.

2.8 MC1031/HAF_12663: Remote Bus Interface (RBI)

Interface between Digital Bus Interface and a microprocessor such as the MA31750 processor. Implements the RBI *Mark I* instruction set, manages OBDH protocol levels 1 and 2 as specified in the Envisat project.

- Devices available from ABB Hafo;
- Support and data sheet available from ADV Technologies. Price and conditions to be negotiated;
- VHDL model for board-level simulation under development;
- Designed by ADV Technologies, licensed to ABB Hafo for use by the space industry;
- Package: 132 pin CQFP with 25 mil lead pitch;
- Process: ABB Hafo SOS4A 2µ CMOS/SOS standard cell. 100 kRad total dose guaranteed, low SEU sensitivity, latch-up free. Transfer to ABB Hafo SOS5 is planned for 1995;
- ESA/SCC qualification of the SOS4A device foreseen Q3 1995.

2.9 L5A5213: Remote Bus Interface (RBI)

Implements the OBDH bus low level protocol, the RBI protocol and a high level protocol to a standard 16-bit processor I/O and DMA interface. Functions are SW configurable allowing protocol flexibility. Contains an expandable 32-bit time counter. Implements the RBI *Mark I* instruction set.

- Devices and support available from Alenia Spazio. Price and conditions to be negotiated;
- Data sheet available from Alenia Spazio;
- Package: 84 pin CQFP with 50 mil lead pitch;
- Process: LSI Logic CMOS/EPI gate array LRH10000 (non-European foundry). 100 kRad total dose guaranteed, SEU LET threshold 80 MeV•cm^2/mg, latch-up free.

2.10 MA28138: Remote Bus Interface (RBI)

DMA interface to the OBDH Bus at Digital Bus Interface level, directly compatible with the MAS281 processor. Implements the RBI *Mark II* instruction set.

- Devices and functional support available from GPS;
- System level support from ESTEC;
- Preliminary data sheet available from GPS, full data sheet under preparation;
- VHDL model for board-level simulation planned;
- Designed by MMS (UK), licensed to GPS for use by the space industry;
- Package: 132 pin CQFP with 25 mil lead pitch;
- Process: GPS 2.5µ CMOS/SOS gate array. 100 kRad total dose guaranteed, low SEU sensitivity, latch-up free;
- Within the ESA/SCC Capability Domain;
- ESTEC contact: C. Smith (WSM).

2.11 MA28139: OBDH Bus Terminal (OBT)

Provides digital functions of modem capability between Litton Bus and Digital Bus Interface (DBI). Decodes and encodes DBI signals to Internal User Bus level. Both functions usable together or separately.

- Devices and functional support available from GPS;
- System level support from ESTEC;
- Complete data sheet distributed by GPS (not in the 1994 GPS data book);
- VHDL model for board-level simulation planned;
- Designed by MMS (UK), licensed to GPS for use by the space industry;
- Package: 132 pin CQFP with 25 mil lead pitch;
- Process: GPS 2.5µ CMOS/SOS gate array. 100 kRad total dose guaranteed, low SEU sensitivity, latch-up free;
- Within the ESA/SCC Capability Domain;
- ESTEC contact: C. Smith (WSM).

2.12 L5A522: Digital PSK Demodulator (BITDEC)

Fully digital, single chip binary phase shift key demodulation device. Programmable bit rate (8 to 4000 bit/s) and subcarrier (8 or 16 kHz), according to the ESA PSS-04-105 *Radio Frequency and Modulation Standard*.

- Devices and support available from Alenia Spazio. Price and conditions to be negotiated;
- Data sheet available from Alenia Spazio;
- Package: 84 pin CQFP with 50 mil lead pitch;
- Process: LSI Logic CMOS/EPI gate array LRH10000 (non-European foundry). 100 kRad total dose guaranteed, SEU LET threshold 80 MeV•cm^2/mg, latch-up free;
- ESTEC contact: C. Smith (WSM).

2.13 Digital PSK Demodulator (DPD)

Digitally programmable single chip phase shift key demodulator supporting the full ESA PSS-04-105 *Radio Frequency and Modulation Standard*.

- Devices and support from Saab Ericsson Space. Price and conditions to be negotiated;
- Short-form data sheet available from Saab Ericsson Space;
- Package: 68 pin CQFP with 50 mil lead pitch;
- Process: GPS 2.5µ CMOS/SOS standard cell. 100 kRad total dose guaranteed, low SEU sensitivity, latch-up free;
- ESTEC contact: C. Smith (WSM).

2.14 MA28140: Packet Telecommand Decoder (PTD)

Single-chip implementation of the ESA PSS-04-107 *Packet Telecommand Standard* according to the PSS-04-151 *Telecommand Decoder Specification*. 6 input channels, Authentication Unit (AU), outputs TC Segments in serial form via up to 63 serial outputs (MAPs) or optionally through a parallel interface. Built-in Command Pulse Distribution Unit (CPDU). Optionally an external AU can be used. Interfaces directly with the ABB Hafo HAF_12396 VCM for CLCW retrieval.

- Devices and functional support available from GPS as for a standard component;
- System level support from ESTEC;
- Complete data sheet distributed by GPS (not in the 1994 GPS data book);
- VHDL model for board-level simulation under development;
- Designed by MMS (F), licensed to GPS for use by the space industry;
- Package: 132 pin CQFP with 25 mil lead pitch;
- Process: GPS 1.5µ CMOS/SOS gate array MA9300. 100 kRad total dose guaranteed, low SEU sensitivity, latch-up free;
- Within the planned ESA/SCC Capability Domain;
- ESTEC contact: P. Sinander (WSM).

2.15 L5A5223, L5A5225: Packet Telecommand Decoder chip set

Implements the ESA PSS-04-107 *Packet Telecommand Standard* according to the PSS-04-151 *Telecommand Decoder Specification*. Eight input channels, up to 63 serial outputs (MAPs). Input data rate up to 66 kbit/s. The chip set consists of one Telecommand decoder PKTDEC (L5A5223), one Command Pulse Distribution Unit (CPDU) (L5A5225) and one optional Authentication Unit (expected 1995).

- Devices and support from Alenia Spazio. Price and conditions to be negotiated;
- Data sheets available from Alenia Spazio;
- Package: 132 pin CQFP with 25 mil lead pitch;
- Process: LSI Logic CMOS/EPI gate array LRH10000 (non-European foundry). 100 kRad total dose guaranteed, SEU LET threshold 80 MeV•cm^2/mg, latch-up free;
- ESTEC contact: C. Smith (WSM).

2.16 HAF_12399: Packet Telemetry Virtual Channel Assembler (VCA)

Implements the ESA PSS-04-106 *Packet Telemetry Standard*. 1 to 8 VCAs + 1 VCM generate transfer frames of length 223, 446, 892 or 1115 octets, up to 12 Mbit/s. The VCA accepts data in byte-wide parallel format or alternatively in serial format. An external standard 8k8 RAM is used as data buffer. The VCA can generate idle packets to fill up transfer frames, as well as idle frames when sufficient data is not available. Optional Built-In Self Test (BIST).

- Devices and functional support available from ABB Hafo as for a standard component;
- System level support from ESTEC;
- Complete data sheet distributed by ABB Hafo;
- VHDL model for board-level simulation available;
- Package: 84 pin CQFP with 25 mil lead pitch;
- Process: ABB Hafo SOS4A 2µ CMOS/SOS standard cell. 100 kRad total dose guaranteed, low SEU sensitivity, latch-up free;
- ESA/SCC qualification foreseen Q2 1995;
- ESTEC contact: P. Sinander (WSM).

2.17 HAF_12396: Packet Telemetry Virtual Channel Multiplexer (VCM)

Implements the ESA PSS-04-106 *Packet Telemetry Standard*. 1 VCM + 1 to 8 VCAs generate transfer frames of length 223, 446, 892 or 1115 octets, up to 12 MBit/s. CLCW, CRC and/or Reed-Solomon coding (using the MA1916) are optional. Two built-in Virtual Channel selection algorithms. TTC-B-01 interface for the CLCW. Optional Built-In Self Test (BIST).

- Devices and functional support available from ABB Hafo as for a standard component;
- System level support from ESTEC;
- Complete data sheet distributed by ABB Hafo;
- VHDL model for board-level simulation available;
- Package: 84 pin CQFP with 25 mil lead pitch;
- Process: ABB Hafo SOS4A 2µ CMOS/SOS standard cell. 100 kRad total dose guaranteed, low SEU sensitivity, latch-up free;
- ESA/SCC qualification foreseen Q2 1995;
- ESTEC contact: P. Sinander (WSM).

2.18 L5A5228: Packet Telemetry device (PKTTLM)

Implements the ESA PSS-04-106 *Packet Telemetry Standard*, frame CRC generation excluded, with frame length 223, 892 or 1115 octets. Each device includes 2 frame formatters (corresponding to 2 Virtual Channels) and the frame multiplexing functions. Serial and 16-bit parallel input. Supports Reed-Solomon encoding on the output using e.g. the MA1916. An external FIFO for each Virtual Channel is used as data buffer.

- Devices and support from Alenia Spazio. Price and conditions to be negotiated;
- Draft data sheet available from Alenia Spazio, full data sheet under preparation;
- Package: 196 pin CQFP with 25 mil lead pitch;
- Process: LSI Logic CMOS/EPI gate array LRH10000 (non-European foundry). 100 kRad total dose guaranteed, SEU LET threshold 80 MeV•cm^2/mg, latch-up free.

2.19 MA1916: Reed-Solomon Encoder

Reed-Solomon encoder (255, 233) plus convolutional encoder, both according to the ESA PSS-04-103 *Telemetry Channel Coding Standard*. The encoders can be used separately or cascaded (concatenation). Reed-Solomon interleave depth of 1, 4 or 5 supported corresponding to frame lengths of 223, 892 and 1115 bytes.

- Devices and functional support available from GPS as for a standard component;
- Complete data sheet distributed by GPS;
- VHDL model for board-level simulation under development;
- Designed by MMS (UK), licensed to GPS for use by the space industry;
- Package: 28 pin ceramic DIL and 28 pin flat pack with 50 mil pitch;
- Process: GPS 2.5µ CMOS/SOS standard cell. 100 kRad total dose guaranteed, low SEU sensitivity, latch-up free;
- Within the ESA/SCC Capability Domain;
- ESTEC contact: C. Smith (WSM).

2.20 HAF_11918: Ion Counter

Contains two long counters, each 4 times 24 bits. Shift registers for serial readout of the counter values. Developed in cooperation with the ESA Space Science Department.

- Devices and functional support available from ABB Hafo as for a standard component;
- Complete data sheet distributed by ABB Hafo;
- Package: 24 pin CQFP with 50 mil lead pitch;
- Process: ABB Hafo SOS4 2µ CMOS/SOS standard cell. 100 kRad total dose guaranteed, low SEU sensitivity, latch-up free;
- ESA/SCC qualified, specification number 9204063.

2.21 HAF_12200: Spin Segment Clock

Divides a fixed timed period (e.g. spacecraft sun pulses) into a number of equal parts up to 65536. It can be used for time activities such as thruster firings.

- Devices and functional support available from ABB Hafo as for a standard component;
- Complete data sheet distributed by ABB Hafo;
- Designed by MMS Systems, licensed to ABB Hafo for use by the space industry;
- Package: 28 pin ceramic DIL;
- Process: ABB Hafo SOS4 2µ CMOS/SOS standard cell. 100 kRad total dose guaranteed, low SEU sensitivity, latch-up free.

2.22 HAF_12201: Main Thruster Logic

Operates in 3 modes: Thruster controller, Interface to the MAS281 processor, or Buffer mode. Works together with the Spin Segment Clock device to control attitude control thrusters.

- Devices and functional support available from ABB Hafo as for a standard component;
- Complete data sheet distributed by ABB Hafo;
- Designed by MMS Systems, licensed to ABB Hafo for use by the space industry;
- Package: 68 pin CQFP with 50 mil lead pitch;
- Process: ABB Hafo SOS4 2µ CMOS/SOS standard cell. 100 kRad total dose guaranteed, low SEU sensitivity, latch-up free.

2.23 HAF_12467: Isolated Relay Driver

Contains four separate, galvanically isolated relay drivers, each capable to drive 50 V and 100 mA. Two switches per die, the package contains two dies for redundancy.

- Devices and functional support available from ABB Hafo as for a standard component;
- Complete data sheet distributed by ABB Hafo;
- Package: 16 pin ceramic DIL;
- Process: ABB Hafo SOS4 2µ CMOS/SOS standard cell. 100 kRad total dose guaranteed, low SEU sensitivity, latch-up free.

3 FLIGHT COMPONENTS UNDER DEVELOPMENT

This section lists a selection of devices under development, where the resulting components are intended to be generally available to the space industry. Indicated availability dates and specifications are subject to change.

3.1 90C601E: Sparc Processor Integer Unit (IU)

Sparc instruction set architecture V7 32-bit RISC processor integer unit. Performance 10 Mips and 2 Mflops (using the FPU) at 14 MHz. High concurrent error detection, 99 % of the registers have parity check. Master-Checker operation possible.

- Development started Q3 1992; prototype devices expected in Q2 1995;
- Devices and support will be available from MHS as for a standard component;
- Complete data sheet will be distributed by MHS;
- VHDL model for board-level simulation will be available;
- Package: 256 pin CQFP with 25 mil lead pitch;
- Process: MHS SCMOS1/2 RT 0.85µ CMOS/EPI standard cell. 50 kRad total dose required;
- ESTEC contact: J. Gaisler (WSD).

3.2 90C602E: Sparc Processor Floating Point Unit (FPU)

Sparc instruction set architecture V7 32-bit RISC processor floating point unit, to be used with the Sparc IU. High concurrent error detection, all registers have parity check. Master-Checker operation possible.

- Development started Q3 1992; prototype devices expected in Q2 1995;
- Devices and support will be available from MHS as for a standard component;
- Complete data sheet will be distributed by MHS;
- VHDL model for board-level simulation will be available;
- Package: 256 pin CQFP with 25 mil lead pitch;
- Process: MHS SCMOS1/2 RT 0.85µ CMOS/EPI standard cell. 50 kRad total dose required;
- ESTEC contact: J. Gaisler (WSD).

3.3 90C609E: Memory Controller (MEC) for the Sparc processor

Support circuit integrating functions of a typical embedded Sparc-based computer. Intended to be used with the 90C601E and 90C602E. Includes address decoders, bus arbiter, EDAC, 2 UARTs, 3 timers and a watchdog. High concurrent error detection, all registers have parity check. Master-Checker operation possible.

- Development started Q3 1992; prototype devices expected in Q2 1995;
- Devices and support will be available from MHS as for a standard component;
- Complete data sheet will be distributed by MHS;
- VHDL model for board-level simulation will be available;
- Designed by MMS (F), will be licensed to MHS for use by the space industry;
- Package: 256 pin CQFP with 25 mil lead pitch;
- Process: MHS 1.0µ CMOS/EPI gate array MC-RT. 50 kRad total dose required;
- ESTEC contact: J. Gaisler (WSD).

3.4 ADSP21020/S: 32-bit Floating-Point Digital Signal Processor

32-bit floating point Digital Signal Processor with Harvard architecture; separate memory interfaces for instructions (48-bit) and data (32-bit). 15 Mips sustained, 45 Mflops peak at 15 MHz clock. Fully compatible with the ADSP21020 from Analog Devices.

- Development to be started Q2 1995; prototype devices expected in 1996;
- Devices will be available from the selected foundry as for a standard component;
- Functional support from Analog Devices;
- Complete data sheet will be distributed by the selected foundry;
- Package: 256 pin MQFP with 25 mil lead pitch (TBC);
- ESTEC contact: Ph. Armbruster (WSP).

3.5 MA31753: DMA Controller for the MA31750 processor

Supports MIL-STD-1750 A or B operation in an MA31750 system. Four independent DMA channels, individually maskable. Capable of processor independent table driven operation. Single word, multi-word or demand mode transfers for memory to memory and I/O from/to memory, with built-in parity generation. Daisy-chaining interface allows for channel expansion.

- Prototype devices expected in Q4 1995;
- Devices and support will be available from GPS as for a standard component;
- Complete data sheet will be distributed by GPS;
- VHDL model for board-level simulation will be available;
- Package: 84 pin PGA and 84 pin CQFP with 50 mil lead pitch;
- Process: GPS 1.5µ shrink CMOS/SOS gate array with RAM MA9A243. 300 kRad total dose guaranteed, low SEU sensitivity, latch-up free;
- ESTEC contact: A. Pouponnot (WSD).

3.6 MA31754: Processor Support Controller for the MA31750 processor

Incorporates bus arbiter, programmable wait state generator, watchdog timer, I/O address decoding, interrupt handling, reset generation and 2 simple serial interfaces.

- Prototype devices expected in Q4 1995;
- Devices and support will be available from GPS as for a standard component;
- Complete data sheet will be distributed by GPS;
- VHDL model for board-level simulation will be available;
- Package: 84 pin PGA and 84 pin CQFP with 50 mil lead pitch;
- Process: GPS 1.5µ shrink CMOS/SOS gate array MA9200 (TBC). 300 kRad total dose guaranteed, low SEU sensitivity, latch-up free;
- ESTEC contact: A. Pouponnot (WSD).

3.7 PEC31750: Peripheral Controller for the MA31750 processor

Forms a two-chip microcontroller together with the MA31750 processor. Contains 4 timer/counters, DMA controller, 4 USARTs, Packet Telecommand support circuitry, chip select and waitstate generators, interrupt controller and 2 kbyte on-chip RAM.

- Development started Q3 1993, devices expected Q2 1995;
- Devices and functional support will be available from GPS;
- Complete data sheet will be distributed by GPS;
- VHDL model for board-level simulation will be available;
- Designed by a consortium led by Inisel Espacio, will be licensed to GPS for use by the space industry;
- Package: 132 pin CQFP;
- Process: GPS 1.5µ CMOS/SOS gate array with RAM. Radiation hard, low SEU sensitivity, latch-up free;
- ESTEC contact: J. Gaisler (WSD).

3.8 MA3764: Mask programmable Read Only Memory (ROM)

Fast 64 kbit mask programmable ROM organised as 8k8. Pre-charged structure, operation related to a clock input.

- Prototype devices expected in 1996;
- Devices and support will be available from GPS as for a standard component;
- Complete data sheet will be distributed by GPS;
- Package: 28 pin ceramic DIL and 28 pin flat pack with 50 mil lead pitch;
- Process: GPS CMOS/SOS. Radiation hard, low SEU sensitivity, latch-up free;
- ESTEC contact: A. Pouponnot (WSD).

3.9 MAT53CTM: MIL-STD-1553 controller

Compatible with the MIL-STD-1553B protocol. Three operating modes: Bus Controller, Remote Terminal or Bus Monitor. Programmable time-out. Programmed via a command list stored in external 16-bit wide RAM; can be interfaced to a wide range of processors.

- Prototype devices expected Q1 1995;
- Devices and support will be available from MMS (F). Price and conditions to be negotiated;
- A *Product Specification* is available;
- Package: 132 pin MQFP with 25 mil lead pitch;
- Process: MHS 1.0µ CMOS/EPI gate array MC-RT35K. 30 kRad total dose design goal;
- ESTEC contact: A. Pouponnot (WSD).

3.10 Ada Tasking Co-processor (ATAC) v. 2.1

Memory mapped device implementing the Ada tasking management for the Ada run-time system. The interface is supported by three major Ada compiler manufacturers, the TLD compiler interface is commercially available. 2 kbyte on-chip RAM foreseen, supports up to 128 kbyte external RAM for more tasks (up to 2047).

- Prototype devices expected Q4 1995;
- Devices will be available from the selected foundry;
- Support and data sheet will be available from R-Tech. Price and conditions to be negotiated;
- VHDL model for board-level simulation will be available;
- ESTEC contact: J-L. Terraillon (WSD).

3.11 Local Time Management System (LTMS)

Using a few synchronisation signals from the OBDH bus (1 BCP bit), a 1553 bus or a dedicated serial Time Bus, the LTMS locally regenerates a copy of the on-board time reference as CCSDS-CUC elapsed time. The interface is MA31750/MAS281 oriented. Datation of events, start of actions at a predefined time as well as a time distribution error management are supported.

- Development to be started Q1 1995, prototype devices expected in Q2 1996;
- Devices and support will be available from the manufacturer as for a standard component;
- Complete data sheet will be distributed by the manufacturer;
- VHDL model for board-level simulation will be available;
- Package: 68 or 84 pin CQFP;
- Process: Radiation hard process with low SEU sensitivity, latch-up free;
- ESTEC contact: D. Mäusli (WSD).

3.12 Packet Telecommand decoder (PDEC)

Implements the ESA PSS-04-107 *Packet Telecommand Standard* according to the PSS-04-151 *Telecommand Decoder Specification*. Six input channels, internal Authentication Unit and Command Pulse Distribution Unit, outputs TC Segments in serial form via a MAP.

- Prototype devices expected Q2 1995;
- Devices and support will be available from Saab Ericsson Space. Price and conditions to be negotiated;
- A data sheet is under preparation;
- Package: 132 pin CQFP with 25 mil lead pitch;
- Process: GPS 1.5µ CMOS/SOS (TBC). 100 kRad total dose guaranteed, low SEU sensitivity, latch-up free;
- ESTEC contact: J. Gaisler (WSD).

3.13 AOS Telemetry support chip set

A chip set supporting the six services defined in the CCSDS *Advanced Orbiting Systems, Networks and Data Links* recommendations. It multiplexes the Virtual Channels and performs output formatting. The chip set consists of the Virtual Channel Input Processor (VCHIP) and the Composite Link Frame Formatter (CLIFF).

- Prototype devices expected Q1 1996;
- Devices will be available from MHS;
- Support will be available from Laben. Price and conditions to be negotiated;
- A data sheet will be distributed by MHS;
- Process: MHS CMOS/EPI MC-RT gate arrays, 45 kRad total dose design goal;
- ESTEC contact: C. Taylor (WSD).

4 DEMONSTRATION DESIGNS

This section lists designs intended to demonstrate and/or validate a specific concept. Whether a specific component has been designed with the intent to be actually used in flight varies. In case a demonstration design has been superseded by an available flight design, the demonstration design has been removed.

In some cases devices could be borrowed from ESA/ESTEC, for example to be used for evaluation purposes.

4.1 32-bit bus-watch EDAC

32-bit bus-watch EDAC with selectable 7-bit or 8-bit syndrome. When using the 7-bit syndrome the device is compatible with the IDT 49C460. The 8-bit syndrome allows detection of chip errors for byte-wide memories. Built-in diagnostic functions.

- Designed by Saab Ericsson Space;
- Samples available through Saab Ericsson Space;
- Flight design, originally foreseen for Columbus;
- Could be made available by MHS if sufficient interest exists;
- A *Product Specification* is available;
- Package: 100 pin CQFP with 25 mil lead pitch;
- Process: MHS 1.0µ CMOS/EPI gate array MC-RT5K;
- ESTEC contact: A. Pouponnot (WSD).

4.2 Space NuBus Controller (NUC)

The NUC is a bus interface controller for the 32-bit NuBus (IEEE Standard 1196-1987). It connects to the NuBus using external buffers. Master & slave operation with single and block transfers is supported.

- Designed by Saab Ericsson Space;
- Samples available through Saab Ericsson Space;
- Flight design, originally foreseen for Columbus;
- Could be made available by MHS if sufficient interest exists;
- A *Product Specification* is available;
- Package: 160 pin CQFP with 25 mil lead pitch;
- Process: MHS 1.0µ CMOS/EPI gate array MC-RT29K;
- Used as ESA/SCC Capability Approval test vehicle for MHS MC-RT;
- ESTEC contact: A. Pouponnot (WSD).

4.3 OBDH Remote Bus Interface & Transceiver (ORBIT) chip set

A chip set of three FPGAs implementing a subset of the MA28138 (RBI, *Mark II* instruction set) and the MA28139 (OBT), with a modular interface for the MA31750 processor. The chip set is intended for breadboarding purposes.

- Designed by MSSL;
- Devices available through MSSL;
- Data sheet and support is available through MSSL;
- Package: three 68 pin PLCCs (other packaging possible);
- Implemented in three Actel 1020 FPGAs;
- ESTEC contact: A. Karlsson (PXS).

4.4 Ada Tasking Co-processor (ATAC) v. 2.0

Memory mapped device implementing the Ada tasking management for the Ada run-time system. The interface is supported by three major Ada compiler manufacturers, the TLD compiler interface is commercially supported. A MA31750 evaluation board with the ATAC is available.

- Designed by R-Tech;
- Prototypes available through ESA/ESTEC;
- Flight version under development, see section 3;
- Evaluation support available from R-Tech;
- Complete data sheet, User's Guide and ATAC simulator available from R-Tech;
- VHDL and ADA Register-Transfer level models available;
- Package: 176 pin PGA;
- Process: ES2 CN11B, 1.1µ CMOS/EPI compiled (Genesil);
- ESTEC contact: J-L. Terraillon (WSD).

4.5 Local Time Management System (LTMS)

Using a few synchronisation signals from the OBDH bus (1 BCP bit), a 1553 bus or a dedicated serial Time Bus, the LTMS locally regenerates a copy of the on-board time reference; CCSDS-CUC elapsed and CDS Universal Time are supported. The interface is 8086/MAS281 oriented. Datation of events, start of actions at a predefined time as well as a time distribution error management are supported.

- Designed by IMEC;
- Prototypes available through ESA/ESTEC;
- Flight version under development, see section 3;
- Complete data sheet is available from ESA/ESTEC;
- Support by ESTEC;
- Package: 84 pin PLCC;
- Process: ES2 EPCD10 1.0µ CMOS/EPI standard cell;
- ESTEC contact: D. Mäusli (WSD).

5 ADDRESSES AND CONTACT PERSONS

This section lists addresses, telephone and fax numbers to related companies and organisations.

ABB Hafo AB
P. O. Box 522
S-175 26 Järfälla
SWEDEN
Phone: +46-8-58 02 45 00
Fax: +46-8-58 03 19 52
Commercial contact: Mr Phil Todd
Technical contact: Mr Bengt Larsson

GEC Plessey Semiconductors (GPS)
Doddington Road
Lincoln, LN6 3LF
UNITED KINGDOM
Phone: +44-522-500 500
Fax: +44-522-500 550
Commercial contact: Mr Trefor Davies
Technical contact: Ms Debra Robinson

Matra Harris Semiconducteur (MHS)/TEMIC
B. P. 309
F-78054 St-Quentin-en-Yvelines Cedex
FRANCE
Phone: +33-1-30 60 70 87
Fax: +33-1-30 60 90 24
Contact: Mr Amar Guennoun

ADV Technologies
Parc Technologie du Canal
16, Avenue de l'Europe
F-31520 Ramonville Saint Agne
FRANCE
Phone: +33-62 19 04 44
Fax: +33-62 19 03 54
Contact: Mr Philippe Mercier

Alenia Spazio S.p.A.
Via Tiburtina, 1210
I-00131 Roma
ITALY
Phone: +39-6-41 51 36 02
Fax: +39-6-41 51 36 77
Contact: Mr G. Di Antonio

Inisel Espacio
C/ Provença, 382-386 3a. planta
E-08025 Barcelona
SPAIN
Phone: +34-3-459 05 05
Fax: +34-3-459 36 26
Contact: Mr Xavier Lobao

IMEC
Kapeldreef, 75
B-3001 Leuven
BELGIUM
Phone: +32-16-28 12 11
Fax: +32-16-22 94 00
Contact: Mr Patrick Pype

Laben
S. S. Padana Superiore 290
I-20090 Vimodrone
ITALY
Phone: +39-2-25 07 51
Fax: +39-2-25 05 515
Contact: Mr L. Campa

Matra Marconi Space (MMS), France
B. P. 1
F-78146 Vélizy-Villacoublay Cedex
FRANCE
Phone: +33-1-34 88 48 35
Fax: +33-1-34 88 49 43
Contact: Mr Noël Vallet

Matra Marconi Space (MMS), United Kingdom
Anchorage Road
Portsmouth, Hampshire, PO3 5PU
UNITED KINGDOM
Phone: +44-705-66 49 66
Fax: +44-705-69 04 55
Contact: Dr Graham Evans

Mullard Space Science Laboratory (MSSL)
Holmbury St. Mary
Dorking, Surrey, RH5 6NT
UNITED KINGDOM
Phone: +44-483-20 41 94
Fax: +44-483-27 83 12
Contact: Mr Nigel Bray

R-Tech AB
Surbrunnsgatan 60
S-113 27 Stockholm
SWEDEN
Phone: +46-8-33 19 20
Fax: +46-8-33 19 25
Contact: Mr Joachim Roos

Saab Ericsson Space AB
S-405 15 Göteborg
SWEDEN
Phone: +46-31-35 00 00
Fax: +46-31-35 95 20
Contact: Mr Per Blomqvist

ESTEC
P. O. Box 299
NL-2200 AG Noordwijk
The NETHERLANDS
Phone: +31-1719-86555
Fax: +31-1719-17400

APPENDIX A: ABBREVIATIONS

ASIC	Application Specific Integrated Circuit
ASSP	Application Specific Special Product
BIST	Built-In Self Test
CCSDS	Consultative Committee for Space Data Systems
CLCC	Ceramic Leadless Chip Carrier
CLCW	Command Link Control Word
CMOS	Complementary Metal Oxide Semiconductor
CQFP	Ceramic Quad Flat Pack (leaded)
DAIS	Digital Avionics Instruction Set
DMA	Direct Memory Access
DIL	Dual In Line
EDAC	Error Detection And Correction (also called ECC)
EPI	Epitaxial
ESA	European Space Agency
ESTEC	European Space Research and Technology Centre
FPGA	Field Programmable Gate Array
I/O	Input / Output
LET	Linear Energy Transfer
MFLOPS	Million Floating-point Operations Per Second
MIPS	Million Instructions Per Second
MMU	Memory Management Unit
MQFP	Metal Quad Flat Pack (leaded)
OBDH	On-Board Data Handling
PGA	Pin Grid Array
PLCC	Plastic Leaded Chip Carrier
PSK	Phase Shift Key
RAM	Random Access Memory
RISC	Reduced Instruction Set Computer
ROM	Read Only Memory
SEU	Single Event Upset
SOS	Silicon On Sapphire
SW	Software
TBC	To Be Confirmed
TTL	Transistor Transistor Logic
USART	Universal Synchronous / Asynchronous Receiver / Transmitter
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit

Page intentionally left blank