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The VHDL Standard

An overview of activities, organizations and European tool efforts

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Document Reference: E2S/ESTEC/SCADES 2/WO5-D1
Document Version: 1.1
Document Release Date: 30 May 1994

ABSTRACT

This report is deliverable WO5-D1 resulting from the work packages 5100 and 5200 of Work Order 5 in the ESTEC / WDN / SCADES 2 contract.

The report gives an overview of activities, organizations and European tool efforts related to the VHDL standard. An extensive list of contact points and additional information sources allowing further in-depth studies has been included. The report is not an introduction to VHDL, its usage or its various application areas.

This document is a synthesis of information collected from many sources and documents. E2S would like to thank the many individuals who provided inputs to the report. Thanks also goes to Peter Sinander (ESTEC) for the constructive comments he provided on the draft version of the report.

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List of Acronyms

ASIC	Application Specific Integrated Circuit
ATCC	AVI Technical Coordinating Committee
ATPG	Automatic Test Program Generation
AVI	Analog VHDL International
CAE	Computer Aided Engineering
CEC	Commission of the European Communities
CFI	CAD Framework Initiative
DASC	Design Automation Standards Committee
DASS	Design Automation Standards Subcommittee
DATC	Design Automation Technical Committee
DoD	U.S. Department of Defense
DOD	Design Objectives Document
ECSI	European CAD Standardization Initiative
EDA	Electronic Design Automation
EDIF	Electronic Design Interchange Format
EIA	Electronic Industries Association
FIPS	Federal Information Processing Standard
IEEE	Institute of Electrical and Electronics Engineers
ISAC	Issue Screening and Analysis Committee
LCS	Language Change Specification
LRM	Language Reference Manual
OVI	Open Verilog International
PAR	Project Authorization Request
RTL	Register Transfer Level
SCC-20	IEEE Standards Coordinating Committee
SDF	Standard Delay File
SVWG	Shared Variables Working Group
VASG	VHDL Analysis and Standardization Group
VFE	VHDL-Forum for CAD in Europe
VHDL	VHSIC Hardware Description Language
VHDL-A	Analog VHDL
VHSIC	Very High-Speed Integrated Circuit
VI	VHDL International
VI MAC	VI Marketing Advisory Committee
VI TAC	VI Technical Advisory Committee
VITAL	VHDL Initiative Towards ASIC Libraries
VIUF	VHDL International Users' Forum
WAVES	Waveform and Vector Exchange Specification
WG	Working Group

1 INTRODUCTION

This report is intended to give an overview of the current status of the VHDL IEEE Standard 1076. The objective of this document is *not* to provide an overview of VHDL. The objective is to help positioning the existing VHDL standards as well as the ongoing standardization activities. The report also highlights important European VHDL activities.

Chapter 1 is this introduction.

Chapter 2 lists existing standards and standardization activities. For each activity, it highlights the objectives, current status and future plans.

Quite some organizations are working on VHDL standardization or other VHDL promoting activities. To help understand the positioning and the goals of these organizations, Chapter 3 contains a list of these organizations.

Chapter 4 provides some details on European VHDL related tool efforts.

Chapter 5 gives a few examples of European companies using VHDL. The chapter also lists European R&D programmes related to VHDL.

Chapter 6 lists some conclusions.

All practical information available has been gathered into Chapter 7. This includes electronic repositories (which ones and how to access them) and an extensive list of contacts within companies and organizations, plus various other information.

2 STATUS OF THE VHDL STANDARD

2.1 VHDL IEEE Std 1076-1987

The VHDL language was an offshoot of the VHSIC (Very High-Speed IC) program, funded by the U.S. Department of Defense (DoD), and was first proposed in 1981. The development of VHDL was carried out by IBM, Texas Instruments, and Intermetrics, starting two years later in 1983. In August 1985, version 7.2 of the language was released for public review.

Besides gaining the advantages of a hardware description language, the VHDL developers sought to unify the designs of all the VHSIC contractors and subcontractors into a single language. VHDL would allow anyone working on the program to define circuits and models independently of design tools and independently, too, of technology or vendor of the end product. Thus, a circuit could be designed and archived in VHDL, and later fabricated with the most advanced technology.

In principle, functional parts of a design could be reused in different applications and different technologies without repeating valuable design work. These benefits were especially attractive to the DoD, which is often faced with obtaining equipment and spare parts for decades from multiple suppliers through multiple generations of new technologies. VHDL ultimately was included in Military Standard 454, and is a requirement for all DoD projects.

In March of 1986, the IEEE took on the effort of standardizing VHDL. The VHDL Analysis and Standardization Group (VASG) was set up to review the language, with the goal of repairing known problems with the language and modifying the language where a broad consensus formed around the modifications. The Air Force fully supported this work by awarding a contract to Intermetrics to develop the support software for the new language standard, now known as IEEE Std 1076.

VHDL has been compared to ADA and many of the goals are the same as for the ADA language. VHDL evolution however has differed from ADA and as a result is establishing itself as an industry standard language more rapidly. From the inception of the VHDL program, the DoD acknowledged the weaknesses in the ADA standardization approach and took steps which have resulted in a strong language. VHDL has benefited from substantial industry review and participation throughout its development.

When in March 1986 all rights to the VHDL language were transferred to the IEEE, the original version 7.2 language went through a phase of substantial changes driven primarily

by industry representation from CAE vendors as well as users. The goals of the IEEE in developing a standard language were broader in scope. Driven by the need for a production quality language suitable as a design tool to be used throughout the design cycle, the IEEE enhanced the language substantially.

This effort resulted in the creation of a world-class hardware description language which was ratified in December 1987 as the first industry standard hardware description language with overwhelming support from industry. One important reason for the strong support VHDL has received throughout industry is that unlike ADA, there are no other standard languages which VHDL must compete against. Recently, however, the IEEE standardization of the Verilog Hardware Description Language has started.

2.2 VHDL IEEE Std 1076-1993

Since its emergence as an IEEE standard, VHDL has been quite a success story. Despite the fact that VHDL was created from scratch, more and more companies signal that they are entering the VHDL marketplace or that they are expanding their current offerings. VHDL has established itself as the premier hardware description language.

The IEEE is very determined that standards be used by their communities. Therefore, it is an official IEEE requirement that all standards be reaffirmed at least every 5 years. This reaffirmation may be anything from reaffirmation simpliciter to a radical change. The important point is that a group of experts and users within the standard's designated community must care enough about the standard to keep it alive.

For VHDL, the 5 year reaffirmation IEEE requirement means that the language had to be reballoted during 1992. Therefore, the VHDL Analysis and Standardization Group (VASG) began planning the eventual reballoting in June of 1990.

The first decision made was to disallow radical changes to VHDL during this restandardization period. The language had great forward momentum in the marketplace, and radically altering it —even for sound technical reasons— could have a devastating impact to that momentum. Second, for much the same reason, it was decided to make the new version of VHDL as upward compatible as possible. Finally, it was decided to allow change requests to come from the users.

In December 1992, the VHDL ballot successfully passed the IEEE requirements for the first time. Then, the resolution process for the comments received during this first ballot started. The team in charge to answer these comments changed the Language Reference Manual, so there had to be a second ballot.

The second ballot was held in May 1993. The ballot results were positive: 155 affirmative, 40 negative and 14 abstention votes. This reflects a return rate of 85.6% and an approval rate of 79%. The standard was then formally approved at the September 1993 meeting of the IEEE Standards Board's Review Committee.

The IEEE Std 1076-1993 was published during the first quarter of 1994. The new Language Reference Manual (LRM) is self-sufficient, which means that the "old" LRM has become obsolete. The new LRM includes an appendix identifying portability issues.

During the restandardization process, several working groups were formed. The following working groups submitted a PAR (a PAR is a Project Authorization Request, which gives a group a formal status as a working group moving towards a standard) to the IEEE New Standards Committee, and were approved:

- 1076a Shared Variables - amendment to IEEE 1076-1993
- 1076.1 Analog Extensions to VHDL
- 1076.2 Standard Mathematical Package
- 1076.3 Standard Synthesis Package
- 1076.4 VHDL Timing and Back Annotation
- 1076.5 Utility Libraries

Recently (April 1994) a new DASC Test Study Group is being formed.

Another PAR which was approved, is the standardization of the Verilog HDL (PAR 1364). As only the VHDL Hardware Description Language is within the scope of this report, we did not include any further information on this PAR. However, we mention it for completeness.

Section 2.3, titled *Extensions of VHDL*, gives information on PAR 1076a and PAR 1076.1. Section 2.4, titled *Definition of Standard Practices*, gives information on PAR 1076.2, PAR 1076.3, PAR 1076.4, PAR 1076.5 and the Test Study Group. As the IEEE Standard Multivalue Logic System for VHDL Model Interoperability (IEEE Std 1164-1993) and the IEEE Waveform and Vector Exchange Specification (IEEE Std 1029.1-1991) also define "Standard Practices", there are subsections giving information on this standard.

First, we have another subsection on VHDL '93, highlighting some reflections on VHDL '93.

2.2.1 Reflections on VHDL ’93

The user requirements gathered during the restandardization process can be classified as follows:

- bugs and repairs (e.g., textio, which was ill-defined),
- improvements (e.g., provide a no-change option for conditional signal assignments), and
- new concepts (e.g., introduce analog modelling).

An additional division can be made between

- requirements regarding the language itself and
- requirements regarding its use (e.g., provide a SIN function).

Some of the requirements, mainly the synthesis-related ones, could be answered by the standardization of ’standard’ packages, such as the std_logic_1164 package defining a nine-state multi-value logic type and its associated resolution and logical functions (which has already been voted on) or the standard packages of Ada. Such packages could be written in pure VHDL and introduced as part of the standard or of sub-standards. An example of a VHDL application that became a standard is WAVES.
Other requirements included changes in the definition of the language itself.

Among all the requests from users for a VHDL ’93 standardization, the requirements concerning analog domain, and more precisely mixed-mode simulation, were most numerous: about one fifth of the total. Europeans are particularly interested in this field.

In the very early stages of the standardization process, it became apparent that it would not be possible, due to the very different levels of requests as well as to scheduling, for analog extension to be included in VHDL ’93. However, because of the interest of designers in this topic, a PAR (a Project Authorization Request) of VHDL has been launched. The first draft of the Language Reference Manual is expected to be balloted by the end of 1994.

Thus, VHDL ’93 (like VHDL ’87) does not cover the analog domain. Nevertheless, it is easy to find many papers and even tutorials explaining how to model analog parts in VHDL ’87. For limited purposes, this has been done with VHDL ’87 and, of course, is possible with VHDL ’93.

Indeed, VHDL ’93 offers some new possibilities for this purpose. The main one is the introduction of a foreign "mechanism" that allows foreign models to be interfaced. These models can potentially be described in an analog modelling language. This is not a "pure" VHDL solution, and the interface is described so briefly that problems of portability and dependency on tool vendors are inevitable. Nevertheless, this interface does exist, which is an important advantage.

For people in search of a "pure" VHDL solution, one of the main problems is to identify the "steady states" of the digital world during which the analog kernel may execute. Last-delta activation processes should solve this. It is also possible to imagine calling foreign subprograms from these processes to activate an external analog kernel.

Analog modelling very often depends on parameters that can vary dynamically during simulation. One example of this is temperature. The dynamic characteristics of such parameters cannot be represented by the use of generic parameters. Their representation as global signals or specific ports is definitely not satisfying. Shared variables, which are in fact global variables, have been introduced into VHDL ’93 and could be used for this purpose.

2.3 Extensions to VHDL

2.3.1 Analog VHDL (VHDL-A) Working Group

Name : **Analog Extensions to VHDL WG** (VHDL-A)
PAR : 1076.1
Chair : Jean-Michel Bergé
Contact list : see section 7.5
Information : see section 7.5 for details on how to get more information

Objectives

- The purpose of the VHDL-A working group is to develop analog extensions to VHDL, i.e. to enhance VHDL such that it can support the description and simulation of circuits that exhibit continuous behaviour over time and over amplitude.
- VHDL-A must be suitable for the description and simulation of digital, analog, and mixed digital/analog systems. VHDL-A must be able to support any design methodology and be technology independent.
  Technology independence means that components of any technology (electrical, mechanical, thermal, optical, fluid,...) must be supported, for example the attitude and orbit of a satellite.
  Mixed analog/digital simulations are a very important usage of VHDL-A, for example mixed analog/digital simulation of an ASIC as well as mixed simulation of a mechanical system (such as attitude and orbit of a satellite), together with a digital system (such as the digital implementation of the satellite control system).
- The analog part of VHDL-A should be targeted primarily towards the following applications:
  - DC and transient analysis,
  - electronic circuits (OpAmps, PLLs, comparators,...),
  - lumped element systems (meaning that microwaves cannot be handled).

The other domains (mechanical, thermal,...) could be easily introduced as they are analogous to the electrical domain.
- Using VHDL-A, it should be possible to describe the structural composition of analog subcircuits connected by analog wires. Analog components could embody SPICE netlists since the analog simulator should understand this de facto standard description.
- Using VHDL-A, it should be possible to describe the behaviour of analog circuits. Two styles should be provided: relations or equations, and procedural models. These two styles will form the "core" of the analog part of VHDL-A.

Activities completed

The Design Objectives Document is completed and is available via anonymous ftp from the VHDL-A repository mentioned in section 7.5.

Activities planned

Language design phase, documentation and validation phases are going on Goal: the LRM (Language Reference Manual draft #1) will be ready for balloting by the end of 1994. Responses from the first ballot should be received and ready for analysis by March 1995. Further steps are to respond to all balloting responses, determine the result of the ballot, modify documents as required, and resubmit for balloting. Most probably, there will be at least two ballots. The earliest that balloting could be complete is August 1995. This schedule is rather ambitious. As more information is gathered and work progresses, the Work Group will reschedule the activities.

Relationship with other Working Group / Standards
- Through DASC meetings.
- It has been decided that VHDL-A will be an extension of the current VHDL and not a supplement: i.e. the ballot only concerns analog extension (and not the entire language) and the result (if positive) will consist in two standards. The previous STD 1076 remains the same and the analog standard is created and refers to it.

2.3.2 Shared Variables Working Group

Name : **Shared Variables WG** (SVWG)
PAR : 1076a
Chair : Stephen Bailey
Contact list : see section 7.5
Information : see section 7.1 for details on how to get more information

Objectives

Shared Variables received the largest percentage of negative votes and/or comments in balloting for VHDL 1076-1993. The working group was formed with the charter of

proposing an amendment to VHDL 1076-1993 (1076a) that would re-design the language implementation of shared variables in order to address as many as possible of the concerns that balloters of 1076-1993 have as possible.

Activities completed

The work is currently in the requirements phase. Requirements have been collected and shortly the voting on each requirement's relative importance will start (some requirements are in conflict with others). The final requirements document was planned to be complete by the end of February 1994.

A technical writer, LRM editor and technical review committees have been formed. A requirements committee is completing the requirements work.

Activities planned

Once the relative importance of each requirement has been established, the technical committee and writer will begin work on a language re-design proposal. Language changes will be limited to areas related to shared variables.

The proposal will be submitted to the technical review committee and re-worked as required by the committee's feedback. Finally, the proposal will be submitted for a vote of the voting membership of the SVWG. If approved, the proposal will be given to the LRM editor who will integrate the changes with the LRM. The revised LRM will be reviewed and then submitted to the IEEE for balloting.

Relationship with other Working Groups / Standards

Amendment to IEEE 1076-1993.

The OO-VHDL study group will be monitoring the shared variables progress since one possible approach (monitors) is object-oriented.

2.4 Definition of Standard Practices

2.4.1 Mathematical Package Working Group

Name : **VHDL Mathematical Package WG**
PAR : 1076.2
Chair : Jose A. Torres
Contact list : see section 7.5
Information : see section 7.1 for details on how to get more information

Objectives

Develop a set of standard VHDL mathematical packages that include:

- most often used real and complex elementary functions, and
- the required data types and type conversion functions.

Activities completed

- Strawman proposal for a math real and complex package is done (includes package definition and body).
  - Real functions include common real constants, common real functions and real transcendental functions.
- Work is in progress to put together a test bench.
  - The NBS FORTRAN tests of math functions will be reused (15/10/93)
  - The WG is checking with Mentor Graphics if the tests for their math package can be used as a basis for the test bench (15/10/93).
  - The Vantage test bench template can be used as a basis for the test bench (15/10/93).
  - Some funding is available from Synopsys to develop a prototype of the test bench for the math package (15/10/93).
- Electronic form of the package is available on request.

Activities planned

- Finish test bench,
- Verify proposed functions,
- Incorporate suggested changes, and
- Ballot the package.

Currently, they are looking at June-July 1994 to start balloting the packages.

Relationship with other Working Groups / Standards

- This standard is meant to be compliant with VHDL Standard 1076.
- The VHDL Analog Extensions WG will submit analog requirements to the Math WG. No requirements were received by 25/11/93.
- The minutes of the 15/10/93 Math WG meeting mention the following: "There is still the issue about the need for double precision functions and the possibility that a new real type called FLOAT may be part of the VHDL-A effort. This type will require greater accuracy than the current REAL type. The current proposed solution for this requirement is to develop two math packages: one for each real type.
  One consequence of such a decision is that we could ballot the REAL based math package almost immediately and could ballot the FLOAT package at the same time that analog is balloted."
- The COMPLEX package is intended to support analog needs, complex numbers should probably be based on FLOATS.

2.4.2 Synthesis Package Working Group

Name : **VHDL Synthesis Package WG**
PAR : 1076.3
Chair : Alex Zamfirescu
Contact list : see section 7.5
Information : see section 7.1 for details on how to get more information

Objectives

Enhance portability of synthesizable models by developing standard practices and definitions for representing design information needed for synthesis.

Activities completed

A draft *Standard VHDL Synthesis Package* document is available. The (draft) standard defines standard practices for synthesizing binary digital electronic circuits from VHDL source code. The standard treats the following topics:

- Interpretation of std_logic_1164 values
- Initial values and default expressions
- STD_MATCH function (wild card matching for the don't care value)
- Standard arithmetic packages

For the purpose of this standard, the synthesis tool is any system, process, or tool that interprets VHDL source code as a description of an electronic circuit and produces an alternative description or form of that circuit in accordance with the terms of this standard. The user is a person, system, process, or tool that generates the VHDL source code to be processed by the synthesis tool.

Activities planned

- In the short-term, the group will focus its efforts on turning the draft standard into an official IEEE standard.
- In the longer-term, the group will promote additional standards in the synthesis domain which will help make synthesizable VHDL descriptions more portable.

Relationship with other Working Groups / Standards

The VHDL Synthesis Package Standard shall be used in conjunction with the IEEE Std 1076-1993 and the IEEE Std 1164-1993 (std_logic_1164).

2.4.3 The VHDL Timing Working Group / VITAL

Name : **VHDL Timing Working Group** (VITAL)
PAR : 1076.4
Chair : Victor Berman
Contact list : see section 7.5
Information : see section 7.1 for details on how to get more information

Objectives

The Timing Working Group is exclusively focused on VITAL (VHDL Initiative Towards ASIC Libraries). The objective of the VITAL initiative is to *"accelerate the development of sign-off quality ASIC macrocell simulation libraries written in VHDL by leveraging existing methodologies of model development."*

Activities completed

- The VITAL Model Development Specification (version v2.2b, released March 25, 1994) document reflects the results of inputs and discussion by ASIC foundries, end users and EDA vendors in response to version v2.1e (released end of December 1993). This specification is approved by the VITAL members.

Activities planned

- The VITAL Model Development Specification will be handed off to the IEEE 1076.4 Timing WG to proceed forward with the standardization effort. VITAL will be releasing the design and all VHDL packages to the IEEE.
- While the standardization of VITAL is ongoing, products and services will be developed that leverage the techniques and packages specified by the VITAL Model Development Specification.
- An initial draft standard should be available for the EuroDAC '94 conference in September. The goal is to have VITAL balloted by December 1994. The VITAL standard might then be accepted by the IEEE Review Committee by September 1995.

Relationship with other Working Groups / Standards

This standard is meant to be compliant with the IEEE Std 1076-1987 and the IEEE Std 1164-1993 (std_logic_1164) and uses the Open Verilog International (OVI) Standard Delay File (SDF) format. The SDF format will form the basis for the implementation of back-annotation in VHDL.

Additional information

The VITAL Organization: the VHDL Initiative Towards ASIC Libraries (VITAL) is an industry-based, informal consortium formed with the following in mind:

- Charter: Accelerate the availability of ASIC libraries across industry VHDL simulators.

- Objectives: (1) High-performance, accurate (sign-off quality) ASIC simulations across VITAL-compliant EDA tools from a single ASIC vendor description, and (2) aggressive time-to-market.
- Approach: Define a modelling specification (in conjunction with VHDL packages) that leverages existing practices and techniques, is compliant with IEEE Standards 1076 and 1164, and utilizes OVI's SDF timing format. Standardize the approved result through the IEEE.
- End-Product:
  - VHDL Package defining standard, acceleratable timing procedures for delay value selection timing checks and timing error reporting;
  - VHDL Package defining standard, acceleratable primitives for boolean and table-based functional description;
  - Usage of the OVI Standard Delay File (SDF) format to back-annotate delays after the layout has been performed.
  - Model Development Specification document defining utilization of VITAL and VHDL elements for ASIC library development.

The main focus of the VITAL activity is ASICs, but the timing modelling concept and the back-annotation using SDF could also be applied for components to be used for Board-level simulation.

2.4.4 VHDL Utility Library Working Group

Name : **VHDL Utility Library Working Group**
PAR : 1076.5
Chair : Gabe Moretti
Contact list : see section 7.5
Information : see section 7.1 for details on how to get more information

Objectives

- Maintain and update the IEEE Std 1164.
- Develop additional packages which support and encourage good modelling technology and which span more than one PAR.

Activities completed

- None. This is a new working group.

Activities planned

- Update of IEEE Std 1164 to VHDL '93.
- Interoperability of VHDL / Verilog package(s).
- Modelling utility package(s).

Relationship with other Working Groups / Standards
This standard will produce an update of the IEEE Std 1164-1993 (std_logic_1164). All work produced will be compliant with the IEEE Std 1076-1993.

2.4.5 VHDL Test Study Group

Name : **VHDL Test Study Group**
PAR : —
Chair : Z. Navabi
Contact list : see section 7.5
Information : see section 7.1 for details on how to get more information

Activities planned
This new DASC study group is being formed. During March / April '94, the group was gathering ideas, views and possible issues that the group should consider and deal with. The group will first do some study work and will then start on standardization. The following list of ideas exists:

- Test Modelling: VHDL models for test generation, critical path tracing, fault simulation, fault collapsing,...
- Test Utilities: VHDL utilities for test application, random test pattern generation, generic LFSRs, signature analysis,...
- Test Languages: VHDL subsets for test related formats such as fault lists, fault dictionaries, test patterns,...
- Test Environments: VHDL environments for activation of testable models, test application, test grading, report generation,...
- Testability

People who want to participate in this study group, can send a mail with their views and issues they like to be considered to navabi_z@irearn.bitnet or to navabi@nuvlsi.coe.neu.edu.

2.4.6 Std_logic_1164 Package (IEEE Std 1164-1993)

Using VHDL, you can build up a more complicated circuit model by interconnecting "component" circuit models. However, VHDL requires that the ports to be interconnected and the signals that are to interconnect them must be declared with the same type. Historically, designers have used logic systems that contained anywhere from four to 128 logic levels. Models written in different logic systems cannot be interconnected.

This resulted in the need for a standard logic system that allows models created by different designers with different tools to be interconnected. In April 1990, industry members formed the VHDL Model Standards Group under PAR 1164 of the IEEE Design Automation Standards Committee (DASC) with the goal of developing and promoting a standard logic system. The group developed a nine-state multivalued-logic type declaration that provides a common interface type-declaration for VHDL models of digital systems. This system is useful for models written at the gate level up through the systems level.

While the nine-state logic system was officially signed off as an IEEE standard in March of 1993, it has been the de facto standard for much longer. And virtually every developer of computer-aided engineering tools has incorporated the approach into its logic suite.

The nine states are:
- 'U' - uninitialized, representing the value of a signal that has never changed
- 'X' - forced unknown, representing a power supply strength signal that is unknown (could be true or false)
- '0' - forced false, representing a power supply strength that has the value false
- '1' - forced true, representing a power supply strength that has the value true
- 'Z' - high impedance, a floating value (undriven) with no value
- 'W' - weak unknown, representing a weakly driven value (not connected directly to the power supply) with an unknown value (could be true or false)
- 'L' - weak low, representing a weakly driven value with the false value
- 'H' - weak high, representing a weakly driven value with the true value
- '-' - don't care, used primarily by synthesis tools in which a don't care value is useful

2.4.7 WAVES, Waveform and Vector Exchange Specification (IEEE Std 1029.1-1991)

The WAVES definition and standardization effort which resulted in 1991 in the IEEE standard 1029.1-1991, was jointly sponsored by two groups, representing design and test activities, respectively:
- the Design Automation Standards Subcommittee (DASS) of the IEEE Computer Society Design Automation Technical Committee (DATC), and
- the IEEE Standards Coordinating Committee-20 (SCC-20).

SCC-20's main responsibility is to develop test standards. Its chief product is the ATLAS test language. People from SCC-20 interested in a standard language for test vectors and people from DASS interested in the test application of VHDL joined forces in the WAVES Analysis Standardization Group (WASG), chaired by Robert Hillman of the US Air Force Rome Air Development Centre.

WAVES integrates design and test activities. As a test vector language, WAVES specifies the input and output signal waveforms for a device under test. The device under test may be a VHDL model exercised by a simulator during design, the actual hardware exercised by automatic test equipment (ATE) during test, or some combination of software models and hardware components.

WAVES offers a degree of interoperability between testers, just as VHDL offers a degree of interoperability between simulators. If ATE vendors support the WAVES interface to their particular testers, then a test set described in WAVES, called a WAVES data set, can be easily retargeted to different testers.

The entire WAVES data set is expressed in VHDL—and optionally in ASCII text files that are compatible with the VHDL file I/O, using the VHDL package, textio. Thus WAVES data sets can be used as waveform sources in any standard VHDL implementation without translating them further.

Currently, there seem to be little products available that are based on WAVES, and there is not much activity going on.

To conclude, there is the following user testimony. Advanced MicroElectronics is the developer of the VHDL Standard Component Library. All models include a test bench compliant to WAVES. The CAD vendors used by Advanced MicroElectronics (Cadence and Synopsys) also support WAVES. By experience, Advanced MicroElectronics found out that by standardizing on the test benches, they can readily translate their vectors to other simulators. Currently, they use five different logic simulators in-house.

3 ORGANIZATIONS DEALING WITH VHDL

[Address information and contact persons can be found in section 7.5]

3.1 VI, VHDL International

VHDL International was founded in June 1991 *to cooperatively and proactively promote the VHSIC Hardware Description Language (VHDL) as the standard worldwide language for the design and description of electronic systems.*

VHDL International provides recommendations to the Institute of Electrical and Electronics Engineers (IEEE) and other standards organizations for favourable solutions to user core issues such as model availability, tool interoperability, methodologies, verification compliance and education.

In addition to promoting the use of VHDL, VHDL International provides information to VHDL users, supports and facilitates VHDL organization efforts, and coordinates and funds ongoing activities to support and advance the language.

To further the common goal of promoting and supporting VHDL on a world-wide basis, VI explores working relationships with VHDL-related organizations in Europe and in Japan. Specifically, there is a working understanding with the European CAD Standardization Initiative (ECSI) organization. A number of cooperative projects might be sponsored by both VI and ECSI. See section 3.2.2 for more information on the close relationship between VI and ECSI.

The VI activities are supported through four working committees, each focusing on a particular aspect of VI activities:

- The **VHDL International User Forum Committee** (VIUF) manages all user related activities of VI. VIUF is responsible for the VHDL user efforts within VI's charter to promote individual and institutional VHDL user initiatives.
  VIUF's principal services include the biannual VIUF conferences, which have grown to be the premiere forums for following VHDL technology. Keynote addresses, tutorials, special interest panels, vendor demonstrations, and technical papers present a comprehensive report of VHDL technology. Covering the range from research to application VIUF conferences also provide the opportunity to interact with the general VHDL community to exchange experiences, meet a new colleague, or discuss problems / solutions.

Starting in 1994, VIUF conferences will be held in conjunction with other VHDL-related meetings to promote mutual agendas. Also, VI established Internet services to support worldwide VHDL-related communication and repository functions. VIUF is also establishing local chapters in many geographic areas to extend VIUF services and activities to address regional needs on a timely basis.

- The **Marketing Advisory Committee** (MAC) deals with promotional activities. It has chosen five objectives for 1994:
  - *Promote cell and component model availability in VHDL* - The goal of this program is to work with vendors and users to actively promote both the availability of models in VHDL as well as to support standards efforts for VHDL modelling.
  - *Promote VHDL '93* - Users have raised many questions regarding the deployment of the VHDL '93 standard. When will vendor tools actually support VHDL '93? What considerations do users need to make when upgrading from a VHDL '87 environment to the VHDL '93 environment? MAC's goal is to provide the user community with guidelines on what to expect and how to plan for the VHDL '93 standard.
  - *VHDL User Survey* - The objective is to promote the findings of the first VHDL user survey conducted by VI in the Spring of 1993, as well as to plan follow-on surveys to track the progress of VHDL and identify new issues.
    These were some important findings of the first user survey:
    . VHDL tools
      The survey highlighted some interesting trends in the evolving VHDL marketplace:
      . 71 % of the respondents said that they are currently using multiple VHDL tools in their design environment indicating that VHDL is being used in multiple phases of the design process; - 100% of the respondents indicated that they are using VHDL for simulation; - 76% indicated that they also use VHDL for synthesis;
      . 82% of the users indicated that tool quality is good to excellent;
      . 18% responded that tool quality is fair or poor.
    . ASIC design
      A number of other issues were also identified. 90% of the respondents felt that ASIC design support in VHDL was either critical or very important, while 87% said that support for ASIC libraries was either critical or very important. To address this issue, VHDL International is continuing to support and work with the VITAL initiative to promote the adoption of a VHDL-based ASIC modelling standard.
    . System design
      System design with VHDL was also highlighted in the survey. 89% of the respondents felt that system design capability in VHDL was either critical or very important. These findings indicate that the design community is viewing VHDL in the context of a broad design solution.

. Tool compatibility
Tool compatibility also continues to be an issue with VHDL users. 90% of the responses indicated that the ability to move VHDL-based designs between different tools was either critical or very important. This finding gives additional support to VHDL Internationals' current project to develop a standard VHDL test suite that will give users a tool for relative measurements of tool adherence to the VHDL language standard.

- *Productize, release and market the VHDL Test Suite* - The aim of the VHDL Test Suite being developed by VI is to address user concerns regarding transportability. The Test Suite will provide users with a tool for objectively measuring how various simulators interpret the VHDL language, thus giving insight into how transportability may or may not be impacted among different tools. MAC's role will be to publicize and market the test suite once completed.
- *Corporate Membership* - The goal is to double the number of corporate members. This is critical to enabling VI to pursue its mission. Increasing the number of corporate members gives VI more momentum and foundation for accelerating the adoption of VHDL. Secondly, increasing membership gives VI more funds that can be used to implement programs and publicity that benefits VHDL users.

- The **Technical Advisory Board** (TAC) sets the technical direction for VI. The following topics have been / are being focused:
  - the need for a standard VHDL value system for model libraries (IEEE Std 1164),
  - the need for a standard method for back-annotating timing data to a VHDL simulator (sponsoring of VITAL),
  - the need to have an independent validation of VHDL simulators (the VHDL Test Suite): VI initiated the development of an industry standard, non vendor-specific VHDL Simulator Test Suite. The Test Suite provides a reference for objective evaluation of simulator compliance to the VHDL specification, thus allowing end-users to focus their tool selection time on other issues such as tool features, performance and cost. The Test Suite will help to assure that designs based upon products complying with the VI Test Suite will have the lowest development risks. VI has selected the VHDL Technology Group to provide technical direction for the program. The Test Suite itself will be administered by VI.
  - standards for modelling methodology (evaluation of several alternative approaches, the result will be a set of carefully conceived guidelines which, if followed, will result in highly portable and interoperable VHDL models),
  - Verilog inter-operability with VHDL,
  - survey of VHDL users.

- The **Education Advisory Committee** (EAC) addresses VHDL education in industry and in academia.

3.2 ECSI, the European CAD Standardization Initiative

3.2.1 Introduction

ECSI was incorporated at Grenoble in May 1993. The European CAD Standardization Initiative is a non profit organization aimed at promoting, all over Europe, the EDA standards (EDIF, CFI, VHDL...). ECSI has been continuously supported by the CEC through the ECIP / ESIP project.

In July 1993, VHDL ’93 was positively voted and in September ’93 it was adopted as the new VHDL ’93 IEEE standard.

There is a real correlation between these 2 types of events: the people fully involved in the elaboration of EDA standards in many different European countries have joint their efforts, with significant help of the CEC through ESPRIT projects, to make the voice and experience of Europe listened to. This means in the particular case of VHDL more than 120 Europeans involved with VHDL restandardization (versus 4 in 1987). This resulted in the introduction of important European user-oriented new requirements into VHDL ’93 and also in a new PAR to define an "Analog VHDL".

ECSI is now recognized as "the" European partner for existing international bodies such as the International Electrotechnical Commission (IEC), CENELEC (European Committee for Electrotechnical Standardization), the International Federation for Information Processing (IFIP), IEEE, the CAD Framework Initiative (CFI), the Electronic Industries Association (EIA), VHDL International (VI).

3.2.2 Relationship with other organizations

ECSI does not compete with CFI, EDIF, VI etc. ECSI wants to encourage and support the work of these organizations and provide a stronger European input. By strengthening European input, ECSI will achieve a better balance of the work in EDA standards between Europe and the USA.

Individual and corporate membership of multiple organizations can be expensive. In addition, active participation is especially expensive for European members because most of the activities are in the USA. ECSI would seek to negotiate benefits on behalf of its members with those organizations so that Europe can fully participate in a more cost effective way.

The first results have been obtained already. Agreement was signed with IEEE-DASC, with IFIP, negotiation is opened with CFI and EIA EDIF-division.

ECSI and VI are fully complementary, and therefore the ECSI Executive Committee and the Board of Directors of VI agreed that ECSI represents and supports VI in Europe. The agreement contains the following points:

- Dissemination of 1150 copies of the VI newsletter "VHDL Times" to the people on the ECSI VHDL Newsletter mailing list,
- Organizing forums or conferences in cooperation,
- Having the same kind of support to VITAL,
- Helping with the development of a "simulation validation suite",
- Installation of reflectors on the VI repositories,
- Involving the VHDL Technical Centre of ECSI in the next phase of development of VHDL validation suites,
- Accessing international standardization bodies (like CENELEC) through the privileged links that ECSI has with these bodies.

A point of this agreement which is still under study, is the common individual membership. Both VHDL International and ECSI offer many services for the membership fee to individuals. Both organisations will draw a list of their cumulated services and decide what could be included in the basic fee which will give common membership to ECSI and VI. Then, other existing services will be added as options on the registration form, which will require an extra amount of money. This deal will be fixed during the VIUF Spring conference organised in the beginning of May 1994.

3.2.3 ECSI Objectives

- To contribute to the creation and promotion of standards, specifications and recommendations acceptable to industry in the area of Electronic Design Automation (EDA).
- To promote the use of such standards, specifications and recommendations.
- To promote the creation of services to provide access to these products for the benefit of its members and European industry.
- The founding members are / have been working to form close relationships with bodies such as CFI, VI and EDIF to avoid duplication of effort and ensure standards reflect worldwide needs. Funding will primarily be from user subscriptions with important funding from specific European programs such as Esprit.

3.2.4 ECSI Activities

The main areas of concern to users are CFI, EDIF and VHDL. Technical centres in these areas have been established and can offer help and active advice to members in the areas of:

- Timely publication of information on developments in EDA standards.
- Guidance on where to use EDA standards.
- Access to electronic repositories of up-to-date information.
- Training services.
- Compliance evaluation and benchmark testing of products.
- Consultancy for members.
- Coordination of User Group activities in Europe.
- Opportunity to participate in International Pilot projects for user trials of proposed EDA standards.

In addition, experts are available to assist with Information Modelling.

3.2.4.1 The VHDL Technical Centres

The VHDL Technical Centres have been established with the support of the Commission of the European Communities (ESPRIT 2072 ECIP) in order to **promote and support standardization** efforts (at IMT, France), as well as encourage **industrial exploitation of VHDL** (at Siemens, Germany).

The IMT has been involved in the VHDL ’93 restandardization process from the very beginning. Due to the synergy between this standardization background and the access to advanced technical work, IMT’s VHDL Technical Centre:

- Gathers and publicizes information on advanced and prototype tools, such as specification using graphic formats or VHDL supersets, high-level synthesis and formal proof of hardware.
- Provides support and expertise on VHDL and holds seminars on advanced aspects of VHDL.
- Issues the VHDL Newsletter (quarterly) and Standardization related documents and books.

VHDL-based design, design methodology and modelling techniques with VHDL are the key issues for the exploitation of VHDL in industrial applications. In order to drive the exchange of VHDL users’ experience and to provide a link between industrial users and experts active in standardization activities, Siemens’ VHDL Technical Centre:

- Provides industrial user support, through seminars on language, tools and VHDL-based design, and tutorials on VHDL principles.
- Organizes the VHDL Forum for CAD in Europe (twice a year). Activities include:
  - Presentation and panel sessions on VHDL-related topics (simulation, synthesis, formal verification, test) and the Industrial application of VHDL.
  - Standardization activities and working group meetings.
- Chairs and organizes the European working group on synthesis requirements for VHDL.

3.2.4.2 Information Modelling

Information Models have become a central aspect of the definition of standards for the exchange of description of engineering data. By means of an information model the area of interest can be described clearly and unambiguously by capturing the relevant entities, their relationships and semantic rules on their values.

Several organizations and bodies working towards standards have implemented procedures which require the provision of an information model to define standards, for example EDIF and CFI. Furthermore, information models of different standards form a basic resource to support work towards interoperability of these standards.

The goals of the modelling project are:

- To support the standards EDIF and VHDL by describing their semantics by means of information models.
- To support the interoperability of standards by comparing their underlying semantics based on a comparison of their information models, e.g. VHDL structure model, and supports other groups who are creating information models, e.g. EDIF, EDIF TC, CFI Design Representation.

3.3 VFE, the VHDL-Forum for CAD in Europe

- **Background**
  The VHDL-Forum for CAD in Europe (VFE) is the European users' group active in VHDL-related topics and standardization efforts and was founded at the International Federation for Information Processing (IFIP) conference VLSI '89 in Munich by IFIP WG 10.2/10.5. Since this time it has been continuously supported by CEC through the ECIP/ESIP project. Additionally, the activities of the VFE are promoted via the VHDL Newsletter under sponsorship of the European CAD Standardization Initiative (ECSI). The members belong to an international range of companies, institutes and universities.

VFE collected diverse European experiences in the field of hardware description languages and related topics.

- **Business**
  During the first two years, the main emphasis of the VFE were the promotion and education of VHDL in Europe and the establishment of relationships to international VHDL users' groups (USA, Japan) and standardization groups. The VFE and the EuroVHDL conferences, as complementary, more research-oriented events, have built the European VHDL network with international connections. Today, more and more European users are in the migration phase towards VHDL. Exchange of design experiences is required. Therefore, the emphasis of the VFE has changed towards the application of VHDL in practise, although the link between research and industrial application of VHDL is an important issue as well.

- **Meetings**
  Two meetings a year are scheduled, a 3 days meeting in Spring and a 1 day meeting joint with the "EuroDAC with EuroVHDL" conferences in Fall. Proceedings can be obtained for previous meetings of the VFE (see contact address of VFE in section 7.5). Topics addressed during the last meeting (Spring '94) were:
  European VHDL users are confronted with various facets of VHDL today, including the application of VHDL and the implied design methodology in ASIC, PCB, and HW/SW (system) design. Exchange of design experiences is necessary. The standardization process is still emerging, although VHDL '93 was balloted. Analog VHDL, working groups defining standardized packages and recommendations, the VITAL initiative and further activities outline the face of VHDL in future. The user benefits from these activities, but must be informed about and be part of the process. This is the role of the VHDL-Forum for CAD in Europe as the European VHDL network with international connections. During three and a half days a tutorial session, 6 technical presentation sessions, a vendor presentation session, 2 panel sessions, a national VHDL users' group session, and a working group session addressed VHDL-related topics and news.

- **VFE & National Users' Groups**
  The VFE is present on the European as well as the international VHDL scene since 1989 and has built up an international network. As the still increasing interest in VHDL in Europe reflects, there is a need for a European VHDL users' group as well as for national VHDL users' groups to exchange experiences and disseminate information. To strengthen the relationship between the European VHDL communities, special sessions are scheduled at each meeting of the VFE to report about the various national activities.

3.4 AVI, the Analog VHDL International Consortium

The creation of AVI has been officially announced during the EuroDAC / EuroVHDL conference in Hamburg (September 1993). It should be a consortium of vendors, users and universities concerned with the development and use of IEEE analog extensions to VHDL (VHDL-A). The main goal of AVI is to promote the development and the acceptance of VHDL-A by providing additional support to the 1076.1 working group.

The AVI Technical Coordinating Committee (ATCC) is responsible to provide an environment in which the VHDL-A language can be evaluated against real constraints. Several subcommittees were created for that purpose.

- **ATCC Validation Suites Subcommittee**
  One goal of this subcommittee, is to review the products of the VHDL-A working group (i.e. the requirements and the language proposal) to trace any inconsistency, inadequation to user needs or non-feasibility. A later validation of simulators and analog libraries is also planned. All this work will be performed in close coordination with the 1076.1 Validation Group.

- **ATCC Usage Model Subcommittee**
  The goal is to formalize the usage of VHDL-A in a real world environment. This will mainly consist of collecting information from real users (designers, tool producers,...) about how they consider the use of VHDL-A for their own purposes and of writing them down into specific documents (such as example sheets or data sheets).

- **ATCC Library Issues Subcommittee**
  One goal is to define rules and mechanisms to cope with existing analog libraries that are not written in VHDL-A. This includes SPICE models of components (written in Fortran or C) and SPICE netlists. Another goal is to define standard guidelines to develop new VHDL-A libraries to promote a real interoperability between models.

- **ATCC Additional Design Requirements Subcommittee**
  The goal is to collect new requirements from AVI members and to forward them to the 1076.1 working group after some first processing from AVI.

3.5 EIA, the Electronic Industries Association

For several years the Electronic Industries Association (EIA) has been active in defining criteria for models that would help to insure uniformity between different vendors and countries. EIA is an accredited national standards organization and is a major influence in the development of international standards.

The standard that affects EIA in the VHDL world is the 'VHDL Modelling Interface Standard for Electronic Components.' This standard is coded EIA-567 and defines the contents and acceptance criteria of VHDL behavioral models for commercial electronic components. Full function VHDL models are addressed. Any subset models (i.e. those models that do not incorporate all of the functions that the underlying component is capable of performing in accordance with its data sheet) are excluded.

EIA-567 was originally released as a formal standard in 1990. With more people using VHDL, short-comings were found in the original specification. During the process of updating the document the DoD instituted it for one of their programs. With this adoption there were many people that tested and improved the document. Since that time, EIA has modified their efforts to make the standard more commercially appetizing.

The text for EIA567.1 is completed. The new standard circulated for review within March / April 1994.

EIA has liaison with VHDL International and works with individuals involved in the VITAL program.

3.6 DoD, the U.S. Department of Defense

The DoD, Department of the Air Force, being very concerned about difficulties obstructing successful development and acquisition of software intensive hardware (e.g. digital systems, digital line replaceable units / modules, digital circuit cards, complex digital components), wrote the *Acquisition Policy 92M-017* about "Software Intensive Hardware Risk Reduction".

This memorandum promotes the use of simulation as part of a disciplined structured engineering process to reduce the risk and cost associated with front-end design and analysis of digital systems. VHDL, along with the commercial availability of design, analysis, synthesis and accelerator tools, provides the designer the ability to employ systems engineering trade-offs, design simulation, and design iteration, as well as to make design changes and examine architectural trade-offs prior to hardware selection.

An optimum balance of risk and life cycle cost with desired performance and schedule must be applied to software intensive hardware for Air Force weapon systems. System program offices will therefore encourage contractors to utilize VHDL to simulate design of digital systems (processors and other digital equipment) before building hardware, and will develop contractual vehicles that motivate contractors to utilize appropriate tools as part of their risk/cost management approach.

3.7 United States Government

As of December 31, 1992 the United States Government has made VHDL a Federal Information Processing Standard (FIPS). A FIPS is the government's reference manual of standards for computer and communications systems.

As a result of the FIPS for VHDL (reference FIPS PUB 172), any digital system supplied to the government must be specified in VHDL. The FIPS for VHDL is applicable for several applications, including primary design and documentation, formal specifications, test generation, and re-procurement and re-design of digital systems.

Objectives. Federal standards for high level digital design information and documentation languages permit Federal departments and agencies to exercise more effective control over the design, production, management, and maintenance of digital electronic systems. The primary objectives of this Federal hardware description language standard are:

- to encourage more effective utilization of design personnel by insuring that design skills acquired under one job are transportable to other jobs, thereby reducing the cost of programmer training;
- to reduce the cost of design by achieving increased designer productivity and design accuracy through the use of formal languages;
- to reduce the overall life cycle cost for digital systems by establishing a common documentation language for the transfer of digital design information across organizational boundaries;
- to protect the immense investment of digital hardware from obsolescence by insuring to the maximal feasible extent that Federal hardware description language standards are technically sound and that subsequent revisions are compatible with the installed base;
- to reduce Federal inventory of electronic digital replacement parts;
- to increase the sources of supplies which can satisfy government requirements for mission specific electronic digital components.

4 EUROPEAN VHDL TOOL EFFORTS

[Address information and contact persons can be found in section 7.5]

4.1 Dassault Electronique (D.E.)

As long ago as 1987, Dassault Electronique (D.E.) got interested in VHDL, when it was a brand new standard, and trained some of its engineers. By 1988, as first CAD vendors proposed their VHDL environment, some benches were carried out.

In 1990, these benchmarks led D.E. to buy the Vantage (now a Viewlogic company) simulator which is extensively used within D.E.'s projects. Some other simulators have been acquired since then:

- Vsystem developed by Model Technology,
- Leapfrog developed by Cadence (originally developed by SEED),
- System 1076 developed by Mentor Graphics.

D.E. developed its own logical synthesis tools for **internal** use (called Frenchip) based on VHDL. The tools use the VTIP kit from Compass.

VHDL is now an international and industrial standard for behavioural and ASIC modelling and cannot be avoided by design engineers any more. D.E. follows the standardisation process in order to understand the language changes. D.E. participates at the main VHDL meeting (like EuroDAC) in Europe and is a member of:

- the technical committee "VHDL ad hoc group" of the SPER (Syndicat des industries de matériel Professionnel Electronique et Radioélectrique).
- the French-speaking VHDL Users' Group created during the EuroDAC '93 at Munich.
- the VITAL initiative.

Papers dealing with projects achieved at D.E. are regularly submitted and presented at international conferences (Cave workshop, EuroVHDL, Avionic conference and exhibition,...).

D.E.'s point of view on VHDL:
VHDL:

- is an industrial standard. So all the modelling projects are portable and perennial.
- has a large spectrum of application: from system level to gate level.
- is a high level language based on a top-down methodology and has several characteristics that make it a specification language.

4.2 INPG/CSI - IST

The INPG / CSI (Institut National Polytechnique de Grenoble / Laboratoire Conception de Systèmes Intégrés) laboratory initially developed the VHDL tool **ASYL**+, which is an optimizer of netlists, a partitioner and synthesizer tool for ASIC libraries as well as for FPGA or CPLD targets.

To trade and further develop the ASYL+ tool, the IST (Innovative Synthesis Technologies) company was founded, and there was a technology transfer from the INPG / CSI laboratory to IST.

The INPG / CSI laboratory plans the following activities:
- Development of interfaces between ASYL and other tools (e.g. tools like SPeeDCHART that generate VHDL specifications from graphical inputs)
- Development of a compilation tool to put in front of ASYL+.
- Development of a VHDL simulation tool to allow simulation before synthesis.

IST is preparing a VHDL subset for synthesis and two synthesis modes. The first one is dataflow oriented, the second one control and architectural oriented. IST is planning and working together with other European companies to propose a complete VHDL solution with a simulator, the IST synthesizer, a test tool and an analyzer to eventually replace the Compass VTIP that they are currently using. However, this is not yet realized.

IST plans to extend their synthesis from VHDL capacities: ASYL+ should accept more and more VHDL clauses and constructions. They try to propose and define user directives for the synthesis process and to allow synthesis on macro blocks libraries. IST thinks about replacing the VHDL analyzer they use for cost reasons, but it is a hard task. They started to develop a simple test generator from VHDL. They plan with other companies to integrate a VHDL simulator. In their kit they propose a low level design partitioner. In the near future, they will work on a high level tool, possibly with a VHDL input.

IST's point of view on VHDL:
In the flow IST proposes, VHDL has several advantages. First of all, it proposes in principle a technology independent description of a design, a clear description easily commented. Then, it is a very easy way to check efficiently if what you propose to synthesize corresponds to your customer or constraint specifications with a first simulation of your model. The synthesis process is run, and a new simulation of the resulting VHDL netlist (structural VHDL and VHDL models of the target library) can permit to check easily the functionality of the synthesized circuit. When formal proof tools can be used, a complete comprehension between VHDL descriptions before and after synthesis can be performed.

4.3 LEDA, Languages for Design Automation

LEDA is a French company providing training, consulting, modelling and development services. LEDA also developed the LEDA VHDL System and announced a crypter of VHDL models.

- The **LEDA VHDL System** is a full VHDL compiler running on UNIX platforms and MacIntosh. The compiler can be integrated as front-end in various CAD tools, including simulation and synthesis tools. It generates an intermediate format (based on the IEEE VHDL Schema Definition 1.02) that is accessible through an ANSI C procedural interface.
- LEDA announced a **crypter of VHDL models**. It transforms VHDL into VHDL. The tool allows you to deliver a functionally correct model, without delivering for free its documentation, its synthesis tunings, its resource packages.
  Input to the crypter is the complete closure of units constituting a model. Output of the crypter is a set of units, functionally equivalent to the input set.
  The names used in the model are changed into computed names. VHDL semantics (overloading) is used to make this translation very difficult to reverse.
  The resources of the model (packages) are made unreusable, mainly by the removal of all objects which are not used, and by inlining static values. All synthesis-related attributes (if not used by simulation) are removed.
  Indentation is broken, comments are removed, all names are made using the O and I characters, ones and zeroes.
  The user can choose to leave a part of the model uncrypted, for example the external interface or some internal object important for simulation trace. Standard packages (like 1164) may be left uncrypted, thus shared with other VHDL code.
- **VHDL** "**Workshop Seminar**" (1.5 day): presentation of VHDL, its main concepts, the different technologies and tools.
- **VHDL** "**Modelling Seminar**" (5 days): study and practice of VHDL modelling techniques.
- **VHDL** "**Modelling and Synthesis Seminar**" (5 days): study and practice of VHDL modelling techniques for simulation and for synthesis.
- **VHDL** "**Project Kick-Off Seminar**" (3 to 5 days, according to the project): helping the customer to start a real modelling project, on site and using the customer's environment.

4.4 Philips ED&T

LOCAM: Timing driven logic synthesis from VHDL

- Existing package extended with timing driven matching.
- Front end created to synthesize from a restricted VHDL subset.
- Extension to allow modular, incremental synthesis of hierarchical designs.
- Extension of mapping to include non-boolean functions.
- Efficiency improvements for large networks.
- Extension to maximal synthesizable VHDL subset.
- Architecture based on the use of SIL signal flow graph enabling extension to high level synthesis.

OPTIMA

- Optima is a tool for the optimization of digital designs, using the retiming technique. By shifting, adding or removing flipflops it optimizes the sequential part of IC designs.
- Features of the Optima tools:
  - allows retiming and pipelining,
  - design optimization to minimal area, maximal clock speed, minimal dissipation,
  - EDIF input and EDIF & VHDL output,
  - scan chain insertion option,
  - fast design and static timing analysis,
  - built-in design data and flow management.

4.5 Siemens

VOTAN: VHDL high-level synthesis system

- VHDL-to-VHDL transformations.
- Value-added platform to commercial RT-synthesis tools.
- Targeted to control-flow dominated applications.
- Full support of WYSIWYS principle "What you simulate is what you synthesize". => automatic verification of the synthesis results is possible.
- Scheduling with a variety of objective functions.
- Multiple wait-statement to single wait-statement transformation ("wait folding"), including state minimization.

4.6 SPeeD

SPeeD is an international VHDL modelling company. It has been founded in 1987 by Peter Busch. Today's shareholders are Sumitomo Corp., Siemens Nixdorf Information-systems,

European Technology Holding AG, and Peter Busch. Currently, 15 people are working for SPeeD, all holding engineering degrees.

SPeeD deploys the following (main) activities:

- Development and production of electronic systems including ASIC development with focus on cost reduction engineering.
- Development and sales of simulation and synthesis models for electronic systems, integrated circuits and libraries using the VHDL language with possible outputs to Verilog HDL and C.
- Development and sales of conversion software, like VHDL2C translator, M2Verilog translator,...
- Development and sales of SPeeDCHART, the graphical tool for the generation of simulation and synthesis models in VHDL, Verilog HDL, C.

SPeeDCHART

The SPeeDCHART tool is a graphical specification environment that is aimed at increasing the productivity of system modelling and design. The tool is typically used as a front-end to other CAE tools, but may also be used as a stand-alone design and verification environment. SPeeDCHART can be used for modelling simple or complex systems at low or high levels of abstraction.

SPeedCHART comprises a number of different graphical editors, called Designers which are based on textual and graphical specification formalisms. Each of these has a consistent user interface that is easy to learn for the beginner and easy to use for the more advanced user. Behavioral blocks described using any of these editors may then be combined together using a schematic editor called Schematic Designer.

Other parts of SPeeDCHART are: the SPeeDCHART Simulation Engine and the SPeeDCHART Translation.

4.7 Synthesia

Synthesia is a Swedish knowledge based company. It is a spin-off from the Swedish Institute of Microelectronics. Synthesia offers high level EDA solutions including both products and services. The company has more than 60 person-years experience in the use of VHDL and has been engaged in VHDL work since 1985.

The Synthesia Products form a complete set of tools for high-level design based on VHDL. The products are developed in close cooperation with the Swedish electronic industry. This has made the tools both efficient in the design process and easy to use.

The Services are general in terms of tools and techniques. Some areas where Synthesia has special competence are: high-level synthesis, VHDL simulation in mixed environments, HW/SW coverification and VHDL modelling.

SYNT High-Level Synthesis
SYNT is a VHDL High-Level Synthesis tool. It accepts VHDL inputs on algorithmic level and produces interactively a design on RTL level. The output design is a Finite State Machine and a Data Path. The result is given in VHDL for further process by Logic Synthesis tools. The output format is general and can be accepted by all major Logic Synthesis tools available.
SYNT High-Level Synthesis performs scheduling and allocation. The components are reused for reduced area and cost. The designer can interactively control and influence the design process. He can easily make trade-offs between area/cost and speed. The multiplexers and registers are optimized with respect to life time.

The MINT System
The MINT system comprises a number of programs supporting simulation of VHDL descriptions. Simulation can be performed interactively during the design debugging phase, or in batch mode for fully automatic design verification.

The MINT/SYNT System
The MINT/SYNT system comprises a number of programs supporting the higher abstraction levels of a VHDL based design flow. Produced results are accepted by existing logic synthesis tools, in order to provide a closed path from algorithmic design specification down to silicon.

Hardware/Software Coverification Package
The exploitation of a methodology for functional verification of the interaction between hardware and software parts in a mixed system during early design phases, will provide additional support for concurrent engineering, thus significantly shorten overall system design times. The general purpose Hardware/Software Coverification support package allows software execution to be verified against VHDL simulation of external hardware by applying interprocess communication. Multiple channels may be created. Each channel will operate according to a client/server relationship.

4.8 Translogic

Translogic B.V. was founded in January 1990 to supply sophisticated graphical VHDL design entry tools. Translogic also offers VHDL training, both desktop courseware for a quick start with VHDL and extensive, five days workshops.

EASE/VHDL: Entity-Architecture Schematics Editor for VHDL
EASE/VHDL is a tool that utilizes schematics and graphical state machine entry, in combination with textual (VHDL) entries.

5 EUROPEAN COMPANIES AND R&D PROGRAMMES

[Address information and contact persons can be found in section 7.5]

5.1 A Few Examples of Companies Using VHDL

5.1.1 Alcatel SDM, Société de Microélectronique

Alcatel SDM is a Belgian company, located in Charleroi. SDM has pilot projects running with VHDL. They used VHDL for design and simulation (ASIC development). For synthesis SYNOPSYS software is being used. Since the end of 1993, all new digital designs are described in VHDL. The VHDL Leapfrog simulator from CADENCE is being used.

Alcatel SDM's point of view on VHDL:

- Advantages: fast and secure description, VHDL is a standard (everybody uses the same language), very easy retargeting, multi chip simulation.
- Recommended for all *digital* design.

5.1.2 EASICS, Engineering ASICs

Easics is a Belgian company, located in Leuven, with several years of experience in using VHDL for ASIC designs and in providing VHDL expertise to ASIC design teams. ASICs and FPGAs have been designed in various domains: high-speed telecommunications, complex image processing, Digital Signal Processing, cryptography,... VHDL has been used in projects for documentation, RTL design, system design, simulation, synthesis and test.

Easics plans to use VHDL more on the system level, for Digital Signal Processing (SCADES 2), and for formal verification.

The VHDL '93 restandardization activities have been followed and the VHDL Synthesis Package Work Group (PAR 1076.3) will be closely followed.

EASICS's point of view on VHDL:

- Through VHDL, you have one description for documentation, simulation, synthesis, system down to gate level, and test.
- A major advantage is the design productivity gain if VHDL is used with synthesis, and when a proper design methodology is used.
- VHDL is a standard.
- VHDL is not to be recommended for structural descriptions.

5.1.3 ES2, European Silicon Structures

ES2 is a major European semiconductor supplier, with branches in various European countries. VHDL is considered strategic by ES2. Their interest and active involvement started with the IDPS project (see section 5.3.3), but is now reaching far beyond.

The advantages of VHDL (standardization, CAE software and vendor independence, design reusability, top-down design approaches etc.) are well known. ES2 considers it in their interest to help their customers in taking best possible benefit of the VHDL advantages. Additionally, VHDL represents direct advantages to ES2, mainly but not only, because of reduced modelling effort and multi CAE vendor support with the ES2 libraries.

The difficulties with VHDL (language constraints, simulator performance, programming hurdle, accurate and standard timing modelling and backannotation at the gate-level etc.) are also well identified. ES2 hopes and is confident that ongoing efforts to solve these problems by enhancing existing or adding new standards will succeed in the near future.

5.1.4 GEC Plessey Semiconductors

GEC Plessey Semiconductors is a major European semiconductor supplier, with branches in various European countries. VHDL is currently being used for both behavioural simulation and synthesis for CMOS digital designs. Analog behavioural simulation will be used when it becomes available.

GEC Plessey Semiconductors are not actively involved in the VHDL restandardization process, but are following progress of the VHDL Timing Work Group - VITAL.

GEC Plessey Semiconductors considers the advantages of VHDL to be:
- the high-level behavioural capability,
- the route to synthesis (from RTL level),
- the standardization.

5.1.5 Hollandse Signaalapparaten (Signaal)

Signaal is a highly specialized company providing electronic equipment for defense and civil authorities all over the world. Signaal operates several plants. The main plant is located in Hengelo, the Netherlands. In 1990 Signaal moved from its position within the Philips concern to become a part of the multinational Thomson-CSF.

In 1991 a pilot project was set up to improve the design flow of an ASIC. The goals for the design flow were:

- high level design phase standard VHDL instead of proprietary HDL,
- one and the same source for simulation and synthesis,
- ASIC design flow integrated in the system design flow,
- automatic synthesis of the complete design, i.e. including datapath logic, control logic, clock networks and full internal scan,
- automatic verification of gate level implementation against VHDL behavioural model.

Up to now, several ASICs have been designed using the new VHDL based design flow. The pilot project team proved that the VHDL based design flow makes it possible to describe ASICs at a higher abstraction level, giving ASIC designers the possibility to increase their productivity and span of control.

Signaal's VHDL experience points out:

- During the high level design phase, writing the behaviour of the decomposed functions, using a VHDL description style suited for the synthesis, *it became clear that it was not the language itself that was difficult. Thinking and designing at a higher abstraction level turned out to be the obstacle*, because hardware designers are used to thinking in gates, flip-flops and counters. Now they must think in process, behaviour and values of variables. The step from describing explicit Finite State Machines, controlling a Data Path, towards describing implicit State Machines, including the Data Path, was a bottleneck in realizing the VHDL model.
- Already at a very early stage of the design phase a complete foundry independent VHDL functional model was available for the board level designer. Therefore, errors could be found in the total functionality which were not covered by the specification. The ASIC designers could easily repair these errors in a structural way.

5.1.6 Siemens Semiconductor Group

The Siemens Semiconductor Group is a major European semiconductor supplier, with branches in various European countries. VHDL has been / is being used within projects for documentation, behavioural description, simulation and synthesis purposes.

The VHDL '93 restandardization process has been followed. However, the progress / activities of the VHDL working groups is not being followed.

Siemens's point of view on VHDL:

The evaluation of electronic IC-specification together with customers and the mutual optimization is a major advantage of using VHDL. Another advantage is the system simulation possibility.

5.2 JESSI, the Joint European Submicron Silicon Program

5.2.1 Profile and Mission of JESSI

JESSI is a EUREKA project: a European cooperative R&D program defined by industry, focusing on Microelectronics, in which more than 150 project partners from 14 European countries are participating. JESSI is a large and impressive program, in every respect:

- more than 30 companies and research institutes participated in making a detailed organizational and technical plan; a plan which comprises about 1000 printed pages;
- the actual technical work started in mid 1989 and the complete program will not be finished before 1996;
- now more than 2,500 scientists and engineers are working on JESSI projects; and
- the total cost will exceed 3,000 million ECUs.

JESSI is a program initiated by industry and governments. It is run and financed by Industry and Research Institutes with financial support from national Public Authorities and the Commission of the European Community.

The mission of the JESSI program is to strengthen the whole European Microelectronics Industry Chain, i.e. the Electronic Systems Industry, the Microelectronics Components Industry and the Semiconductor Production Equipment and Materials Industries. This strengthening means world competitiveness, now and in the future.

In summary, the JESSI objective is to secure the availability in Europe of resources for the design, manufacture and application of Integrated Circuits.

There are currently two JESSI projects directly related to VHDL. These are discussed in the subsequent sections.

5.2.2 JESSI AC-3 Project: HDL, Component Modelling & Libraries

The main objectives of this project are:

- To produce a breakthrough in the availability of modern HDL-based component and system models of European semiconductor manufacturers for usage by the system houses.
- To apply HDL-based simulation and verification technologies to the design of complex systems and to enhance the communication between semiconductors and system houses.

Industrial demonstrators will be used as focus of all activities. Associated *triads* (component manufacturer, system house, modelling company) will be defined.

Thirteen partners from five European countries participate in this project: Anacad, Bosch, Bull, CNET, IBM, IM, INPG, Olivetti, SGS-Thomson, SPeeD, Thomson-TCS, Thomson-SCTF, and Univ. J.Fourier. 44 person years are being spent per year.

The main subprojects are:
- SP1: Analog / Digital Automotive System Modelling
- SP2: High-frequency System Modelling
- SP3: Computer Subsystem Modelling and Formal Proof
- SP4: Computer and Peripheral System Modelling, Simulation and Validation
- SP5: Mixed-Modelling of Telecommunication Subsystem
  - The main demonstrator, provided by SGS-Thomson, is a monochip image encoder-decoder involved in a video-telephone. This system contains 13 blocks. The goal is to simulate, through a VHDL-RTL description, each block of the codec for video-telephone system immersed in its real environment.
  - Milestones related to the main demonstrator:
    . June 1993: Methodology in codec simulation
    . December 1993: Methodology in test
    . December 1993: Simulation of codec environment, control flow
    . 1994: VHDL modelling of the decoder function
    . 1995: VHDL modelling of bit-stream generation, of digital picture encoding and of triple red / green / blue digital / analog converter

5.2.3 JESSI AC-8 Project: Synthesis, Optimization and Analysis

The main objective of this project is *Synthesis of digital circuits and systems*, to cope with the complexity of design and to reduce the design time.

From this, the following **project goals** are derived:

- Application-driven synthesis tool development.
- User entry on various levels of abstraction.
- Textual and graphical specification.
- Synthesis from VHDL.
- Incorporation of formal methods.
- Targeting ASICs, FPGAs and PCBs.
- Tool commercialization and in-house application.

The **partners** of this project are divided in four groups:
- Main Partners: Bull, Philips, SGS-Thomson, Siemens.
- Associate Partners: AHL, INPG, Synthesia.

- Users: Bosch, ISDATA (this was planned in Sept'93), Siemens-Nixdorf, Thomson-TCS.
- Subcontractors: FhG, FZI, TH Darmstadt, TU Chemnitz (this was planned in Sept'93), TU München.

The **project schedule** contains three phases:
- Startup Phase: 140 person.year, 7/90 - 12/91
  Tasks: Studies, Prototype tools
- Main Phase I: 230 person.year, 1/92 - 12/94
  Tasks: Tool development, Tool evaluation & application, Tool productization
- Main Phase II: 180 person.year, 1/95 - 6/96
  Tasks: Finishing, Tool integration, Productization

Among other tools, this project deals with the following VHDL-related tools:
- VOTAN (Siemens): subproject "High-Level Synthesis"
  - Function: VHDL High-Level synthesis for control-dominated applications
  - Version 1 of this tool was scheduled for the end of '93.
- LOCAM-VHDL (Philips): subproject "RT-Level Synthesis"
  - Function: SIL-based VHDL synthesis
  - This tool was scheduled for the end of '93.
- ASYL-Plus (INPG/IST): subproject "RT-Level Synthesis"
  - Function: RT-level synthesis from VHDL, control flow charts (and other specifications) to FPGAs, CPLDs and standard cells.
  - This tool is available.
- SYNT 1.2 (Synthesia): subproject "FPGA Synthesis"
  - Function: SYNT high-level synthesis for FPGA technology and dataflow-oriented applications.
  - Version 1.2 is available. Version 2 containing the dataflow-oriented synthesis is scheduled for the end of '94.

Chapter 4 *European VHDL Tool Efforts* gives more information on the tools mentioned above.

5.3 ESPRIT, the European Strategic Programme for R&D in IT

5.3.1 ESPRIT 2072: ECIP, the European CAD Integration Project

ECIP investigated the area of data exchange and infrastructure standards with the objective of defining and promoting standards within the European Electronic Design Automation (EDA) industry. The final goal of ECIP is the definition of a multilayered open model for CAD systems with recommendation for rules or standards at each level.

In addition to amplifying the work started in ECIP1, ECIP2 addressed the standardization of high-level description languages and the provision of objective ways of measuring the performances of CAD modules.

ECIP has been a key contributor to the establishment of the use of conceptual modelling techniques (also known as information modelling) to underpin the consistency of EDIF (Electronic Design Interchange Format) and CFI (CAD Frameworks Initiative). ECIP has also stimulated interest in the new ballot on VHDL standard in 1993 to the point where up to 40% of those registered to vote are from the Community.

ECIP has established channels for communication with and participation in related international standardization activities. The project sponsored the European CAD Standardization Initiative (ECSI). Three technical centres were established in Europe to be centres of expertise and exploitation of the three main EDA standards (EDIF, CFI and VHDL). These technical centres are being formed from both industrial and academic partners to ensure that they cater for the needs of industry but take into account the longer-term issues and challenges.

5.3.2 ESPRIT 6128: FORMAT, Formal Methods in Hardware Verification

The objective of FORMAT is to reduce the design time for complex hardware modules by providing a set of system-level methods and design tools supporting an enhanced version of VHDL. Emphasis will be placed on formal verification and synthesis methods, whose introduction is expected to lead not only to designs of greater reliability but also to earlier recognition of errors in the design cycle. A transformation approach will also be explored.

FORMAT will specify and develop a graphical front-end and a specification language (VHDL-S) for use by designers. The graphical interface will use timing diagrams augmented to describe hierarchy and structure. Internally, specifications are automatically translated to either temporal logic or LOTOS, depending on the application domain and the approach envisaged.

The verification approach will use temporal logic as an intermediate language to capture, refine and process the specifications. VHDL descriptions will be internally translated into petri-net models from which transition systems will be generated, which will be checked against the specifications. Structural properties will be analyzed directly in the petri-net model and interpreted in the VHDL description.

The transformation approach will use LOTOS to refine the specification through the use of formal methodology. This approach will specifically target the synthesis of

communication controllers. The tools developed will be integrated with the LAMBDA system, the most advanced general theorem-prover framework.

Industrial demonstrators are planned in the fields of communications, advanced general-purpose processors and embedded control systems.

5.3.3 ESPRIT 5075: IDPS, Integrated Design and Production System

IDPS, the European standard for ASIC design and manufacture stands for:

- State-of-the-art performance in 0.7µm CMOS.
- VHDL based top-down design of complex ASICs.
- A common cell library available from European multiple sources (ES2, GEC Plessey Semiconductors, Philips Semiconductors, SGS-Thomson Microelectronics and the Siemens Semiconductor Group).
- Standardization of the library views leading to a European industry standard.
- Multiple sourcing based on the standard netlist description
- Availability of library and design tools on a variety of workstations.
- Fast prototyping.

IDPS provides an ASIC design methodology which is independent of both design tool and silicon manufacturer right up to (and including) gate level timing simulation. You can design your ASIC using VHDL, verify the design's functionality and perform full timing simulations without ever committing yourself to a supplier.

Using your own ASIC design tools, you define your design in VHDL. The VHDL description allows you to perform VHDL simulations to verify the functionality of your design before synthesizing down to gate level using the IDPS Core Library. Full timing simulations can now be performed to check that the design is capable of the required speed in the technology chosen.

With the design verified at gate level, a supplier is then selected and Place and Route is performed using that supplier's layout libraries. The back-annotated interconnect loadings are fed back into the timing simulations which this time are performed using the chosen supplier's detailed gate timings.

5.3.4 ESPRIT 8370: ESIP, EDA Standards Integration and Promotion

This project is based on a previous project ECIP2 (see section 5.3.1) which finished in September 1993. The objective of this project is to spearhead the development and use of EDA standards within Europe.

The emergence of EDA Standards is enhancing the traditional relationships between EDA developers, EDA vendors and EDA users.

EDA standards will allow the user more flexibility and freedom in the choice of EDA development environments, and allow better reusability of design parts. They will enable EDA developers to concentrate on the value-added, application-oriented aspects of their projects. Finally, EDA standards will permit EDA vendors to integrate more easily competitive EDA solutions for their respective markets. This provides an opportunity for SMEs to establish themselves as niche players by providing effective design exchange interfaces through internationally recognized standards, e.g. VHDL, CFI and EDIF.

The ESIP project will therefore continue to focus on five major goals, designed to bring Europe to the leading edge in the development and exploitation of EDA standards. Of these goals, G1, G2 and G5 are to be achieved through the incorporation of ECSI (supported through ESIP during its early stages). G3 and G4 are to be achieved through the Technical Centres and Pilot Projects.

G1 **Be THE main leading and co-ordination body for the involvement of Europe in EDA standards:** to be effective, European participation in world-wide EDA standardization activity has to be coordinated, and contributions to the standardization bodies need to be synchronized. To this end, ECSI should become recognized as Europe's voice in all major EDA standardization committees. ECSI will set up formal relationships with recognized EDA standardization bodies world-wide, e.g. VHDL International, CAD Framework Initiative (CFI), Electronic Industries Association (EIA), Design Automation Standardization Committee (DASC / IEEE), ISO, IEC.

G2 **Be THE European communication platform in EDA standards:** it is essential that EDA developers, EDA vendors and EDA users should be able to communicate efficiently and effectively. In Europe, ECSI should play the leading role in informating EDA end users and EDA developers in all major Microelectronics ESPRIT projects, as well as Industry managers, about EDA standards issues. Using newsletters and electronic repositories and the expertises available at the Technical Centres, ECSI will promote the flow of information throughout the European EDA community.

G3 **Be THE European Competence Centre in EDA standards:** the experience acquired in EDA standards in the previous phases of the project should be extended in some areas, especially where distinct advantages can be gained. For example, some Pilot Projects are to be set up with the specific goal of accelerating the development of certain standards, exploiting the experience gained to date and providing consortium members with unique opportunities. New participants will broaden the influence of this work and the expertise available for it.

G4 **Be a services supplier for the profitable use of EDA standards by the relevant user community(ies):** as well as needing a provider of up-to-date information on EDA standards, end users want to see very concrete services installed which enable them to benefit more rapidly from their use of EDA standards. This is being done in ESIP by providing a firm foundation in the form of Technical Centre services. The wider audience and broader set of members provided by ECSI will help provide a well defined market for exploitation of these centres of expertise.

G5 **Influence the European strategy for the industrial exploitation of EDA standards:** the community of users is far larger than the one represented by the Consortium and this wider community will be available to the project via ECSI membership. The project will support Pilot Projects which will accelerate this exploitation by providing a supportive framework for early adopters and active developers of the standards.

VHDL Workpackage Objectives

Participants: Anacad, Artemis, Bull, CNET, IMT, Synthesia, TGI, Thomson-CSF (leader), UCI, University of Cantabria, University of Madrid, University of Paderborn

Objectives: The objectives of this workpackage are to contribute efficiently to the on-going standardization activities related to VHDL. The contributions consist of standard definition, standard validation and issue of requirements. Covered domains address activities in which the standardization process is presently very active.

6 CONCLUSION

With the approved ballot for the new, enhanced IEEE Std VHDL, we can expect wider application of VHDL in the areas of specification modelling, hardware / software codesign, performance modelling, and design verification, as well as more sophisticated applications at the more conventional layers of design and test.

With work continuing in the standards area for the use of VHDL in the analog design environment, the system aspects of analog / digital design in a common environment becomes more interesting.

The rising interest in VHDL is due to a range of problems brought about by technological advances. They include the demands of increasingly dense IC technology, the pressure on time to market, and the changes in the available design tools.

In the late 1970s and 1980s, much progress has been made possible by ever more powerful tools, each new tool and vendor has forced the designer to learn yet another proprietary language for describing the circuit. Many companies' investments in designs and in training from a single tool vendor were at the vendor's mercy. Likewise, application-specific IC (ASIC) designs targeted at one vendor's technology or process put the user's product at risk if the vendor or the process changed. Thus, emphasizing on VHDL standardization is even more important for users or organizations subcontracting such designs.

In contrast, VHDL promises to provide a common language for describing circuits that is accepted by simulators and synthesis tools from multiple vendors, independently of silicon supplier and technology. Add to this a higher level of abstraction for increased productivity. As is often the case, though, the reality has yet to fulfil everyone's expectations.

For users or organizations subcontracting ASIC designs, VHDL is mainly an interchange format and documentation means. Whether the subcontractor uses synthesis for the production of the ASIC or not, is less important.

7 PRACTICAL INFORMATION

7.1 VHDL International Internet Services (VIIS)

The VIIS is an electronic information service that is available for public use and access. The service is provided and fully supported by VHDL International, and is offered through the "vhdl.org" machine connected to the Internet.

The system has been set up to provide a focal point for standards activities in an electronic forum and to disseminate information about VHDL activities such as VHDL International Users' Forum (VIUF) Local Chapter meetings, VIUF conferences, survey results, discussion groups, and more. The general public can access information via Internet (ftp / Gopher), dial-up, or an email request / response system.

In addition to serving VHDL International and its members, VI has made vhdl.org available to related users groups and standards groups. These other participating groups are able to manage their own email-based discussion groups (reflectors, information lines, auto-archiving of discussions, etc.), file repository systems of important files and documents, form news discussion groups (like comp.lang.vhdl) and perform other important activities. Current groups participating on the VIIS include:

GROUP NAME	CODE NAME
VHDL International (VI)	*vi
VHDL International Marketing Committee Survey Results	*survey
VHDL International Users' Forum	*viuf
Analog VHDL International	*analog
Usenet comp.lang.vhdl Newsgroup	*comp.lang.vhdl
VITAL (VHDL Initiative Towards ASIC Libraries)	vital
IEEE CS DASC VHDL EDIF Interoperability WG	vhdledif
IEEE CS DASC VHDL Math Package WG	math
IEEE CS DASC VHDL Parallel Simulation WG	parallel
IEEE CS DASC VHDL Shared Variables WG	svwg
IEEE CS DASC VHDL Synthesis WG	vhdlsynth
IEEE CS DASC VHDL Utility Library WG	libutil
IEEE CS DASC VHDL Test WG	vhdl_test
IEEE CS DASC VHDL ASG VASG ISAC	*isac
Misc. submissions on VHDL topics	*misc

(* = general email discussion group is not available)

Users can interact with VIIS using the following conventions:

- To find out more information about a group or to provide feedback to the working group only, rather than to the whole reflector list, send an email to: <code-name>-info@vhdl.org, for example vital-info@vhdl.org.
- To be added/deleted to/from an email discussion group and receive notices about activities, email your email address to: <code-name>-request@vhdl.org, for example vital-request@vhdl.org.
- To broadcast a message/info to all on the reflector, send an email message to: <code-name>@vhdl.org, for example vital@vhdl.org.

Email Access:

Send an email message to archive@vhdl.org. The subject is ignored. If a line in the body begins with the word "help", then a description of commands available is sent. Basically, you communicate with the ftp archive server through commands in the body of your email message. It then responds automatically to your request. You should always include the command: path <your_email_address> in every request to assure the server knows where to send the results to.

The following are a few examples of useful commands you could send in the body of your mail message. Each assumes you have requested to mail a message to archive@vhdl.org and included the path command in the body.

path <your_email_address>	- email address (always use)
help	- to get Help
index vi	- to get a listing of the available files and
index vi/vital	directories at a given level
send vi vhdlsynth/00readme_2404	- to ask for a file to be sent to you
send vi 00README	

Dial-Up Access:

Dial-up to the vhdl.org system at +1 408 945 4170. Any baud (up to 14.400), parity, start & stop bits, and v.* settings will do. Login as "guest". Once in, simple UNIX commands such as "cd vi/vital", "ls" and "cat 00README" are available. Also, you can download desired files using "kermit", "zmodem" or "sz" (zmodem).

Internet Access:

The ftp (File Transfer Protocol) tool lets you use a series of UNIX commands to navigate through the "vhdl.org" machine, find the correct file and retrieve it. Use "ftp vhdl.org" (or "ftp 198.31.14.3") and login as user "anonymous". Look into "vi/vital", as an example. Also, Gopher is available and highly recommended if you have it available. Gopher to "vhdl.org".

By sending a blank message to "anonymous" ftp, you receive a help file. Remember to set "binary" mode for any binary files you may elect to receive.

In general, most documents are available in source ASCII exchange format (such as RTF, SyLK, and MIF) and in postscript form ready to be sent to your printer directly. The file size increases accordingly as you move away from the source form.

7.2 USENET Newsgroup comp.lang.vhdl

The newsgroup comp.lang.vhdl was created in January 1991. It's an international forum to discuss all topics related to the VHDL language. Included are language problems, tools that only support subsets etc., but not other languages such as the Verilog HDL. However, if the need exists to discuss information exchange from EDIF to VHDL, this can be a topic of the group.

The information of the comp.lang.vhdl is also made available in the VI repository in the directory vi/comp.lang.vhdl. Via email access, and by sending the following script to archive@vhdl.org you retrieve the information available. Note that before retrieving the files, you can first check whether there is new information available by asking for an index of the vi/comp.lang.vhdl directory.

```
path <your_email_address>
archiver tar
pack compress
encoder uuencode
size 60000
length 80
send vi/comp.lang.vhdl FAQ.books
send vi/comp.lang.vhdl FAQ.general
send vi/comp.lang.vhdl FAQ.productsServices
```

The archiver, pack, encoder, size and length parameters provided are those used at E2S. Please refer to the help file (see above) to know your own settings.

7.3 The Public ADA Library (PAL)

The Public ADA library is a library of ADA and VHDL software, courseware and documentation on the wuarchive.wustl.edu (WUARCHIVE) host computer. The PAL is located in the directories languages/ada and languages/vhdl if you access WUARCHIVE

by ftp, Gopher or FTPMAIL. The PAL reached the Initial Operational Capability milestone in its evolution on June 21, 1993.

The purposes of the PAL are:

- to help make ADA- and VHDL-oriented software, courseware, and documentation that has been released for public distribution (as shareware, freeware, GNU Copyleft, etc) readily available to the public.
- to support ADA and VHDL educators by providing a convenient mechanism for them to exchange material and ideas.
- to support the ADA and VHDL user communities in general by providing a resource in support of their activities.

The PAL consists of five collections of material. The collection related to VHDL is a mirror of the VHDL Repository at the University of Cincinnati, host uceng.uc.edu. This collection is maintained by Dr. Harold Carter of the Department of Electrical and Computer Engineering at the University of Cincinnati. As a mirror, updates occur automatically within 24 hours.

To begin using the PAL, read the PAL.FAQ file (posted on USENET and available in the languages/ada/userdocs/faqfile subdirectory). It is highly recommended that users obtain the current PAL Catalog (named PALCAT.DOC in the subdirectory languages/ada/userdocs/catalog as well.

The PAL can be accessed by a wide variety of mechanisms. These mechanisms include, but are not limited to, the following:

- ftp to WUARCHIVE itself
- NFS mounts on WUARCHIVE
- Gopher servers wuarchive.wustl.edu and gopher.wustl.edu
- PAL mirror sites at ftp.cnam.fr and ftp.cdrom.com
- FTPMAIL email servers
- CDROM distributions
- AdaNET distributions and customer support (AdaNET is free to users)

Users wishing to access the PAL by ftp can use anonymous ftp to contact the main PAL host (wuarchive.wustl.edu) or the PAL mirror sites (ftp.cnam.fr and ftp.cdrom.com). Two hosts support access to the PAL as gopher servers: wuarchive.wustl.edu and gopher.wustl.edu.

7.4 Repository of VHDL Models and Benchmarks

It was announced that a repository of VHDL Models and Benchmarks is available via anonymous ftp from the site erm1.u-strasbg.fr. When verifying the address, I could not connect, but it is possible that this was a temporary problem.

The contact person for this ftp site is:

Dr. Yannick Hervé
MACAO Team of ERM/PHASE
ENSPS, Parc d'Innovations
F-67400 Illkirch, France
P: +33 88 65 50 00
E: yann@sobel.u-strasbg.fr

This site contains a large number of VHDL models developed in the above named centre, or collected from other sites. It also contains the ISCAS85 and ISCAS89 benchmarks in VHDL format. There are currently 62 benchmarks available (17 combinatorial + 45 sequential benchmarks.

Other models which are available are:

- Amd2901 mproc slice
- Amd2910 adress sequ
- I851 UART
- Kalman filter
- 5th order elliptic filter
- GCD controlled by FSM
- Traffic light controller
- Controlled counter
- Differential Equation solver
- DP32
- DLX ver 1
- DLX ver 2
- Shift&add multiplier
- 4 bit register
- Mark2 processor
- Z80 (extracts)
- Parity generator
- 54s151
- 4 bit serial adder
- 8 bit serial multiplier
- 8 bit barrel shifter
- Linear feedback shift register
- 8085 compatible

and

- parser(s)
- packages (random, math, ieee,...)
- papers.

7.5 Contacts List

IEEE - VHDL Committees		
DASC - The Design Automation Standards Committee The DASC primary activity is to promote the development of standards for the Design Automation industry. This organization is the replacement for the Design Automation Standards Subcommittee (DASS) of the Design Automation Technical Committee (DATC) of the Computer Society of the IEEE. Around February 1993, the DATC was withdrawn and the DASS has been changed to the DASC. DASC working groups moving towards a standard, have submitted a Project Authorization Request (PAR) to the IEEE New Standards Committee. Participation in a DASC working group is open to all interested parties, and voting rules are governed by the DASC bylaws.		
Paul Menchini Chair DASC Steering Committee	P: +1 919 990 9506 F: +1 919 990 9507 E:mench@mercury.interpath.net	Menchini & Associates 2 Davis Drive P.O. Box 13036 Research Triangle Park, NC 27709-3036 USA
VHDL Analysis and Standardization Group (VASG), PAR 1076		
Clive Charlwood Chair	P: +1 415 694 4307 F: +1 415 965 8637 E: crc@synopsys.com	Synopsys, Inc. 700 East Middlefield Road Mountain View, CA 94043-4033 USA
VHDL Model Practices, PAR 1164 The Model Practices group is responsible for defining practices appropriate for the use of the VHDL language. The IEEE Std 1164-1993 (std_logic_1164) results from the work of this group.		
William D. Billowitch Chair	P: +1 610 882 3130 F: +1 610 882 3133 E: wdb@vhdl.com	The VHDL Technology Group 100 Brodhead Road, Suite 140 Betlehem, PA 18017 USA
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- Submit new names to be put on the mailing list to
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1076-1-exec@epfl.ch</td></tr>
<tr><td rowspan="2">1076.1 Repositories</td><td colspan="2">- ftp nestor.epfl.ch (or ftp 128.178.50.20)
Material related to the 1076.1 WG is in the directory
incoming / vhdl / analog
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Material related to the 1076.1 WG is in the directory
doc / standards / ieee / 1076.1 / analog</td></tr>
<tr><td colspan="2">Using anonymous ftp and the following script, you can retrieve some interesting documents from nestor.epfl.ch (the main repository)

reply <email_address>
connect nestor.epfl.ch
get incoming / vhdl / README
get incoming / vhdl / analog / working / presentations / vhdl-white.ps.Z
get incoming / vhdl / analog / ref / DOD / DOD_1.1.PS.Z
get incoming / vhdl / analog / ref / DOD / requirements.txt
get incoming / vhdl / analog / ref / glossary / Glossary_2.0.txt
ls incoming / vhdl / analog / working
ls incoming / vhdl / analog / ref
quit</td></tr>
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Email reflector + Repository	See section 7.1. <code-name> = vital	
	Using email access and the following script, you can retrieve the VITAL Model Development Specification (v2.2b) from archive@vhdl.org path <email_address> archiver tar pack compress encoder uuencode size 60000 length 80 send vi/vital announce.refl send vi/vital Spec_ps.tar.Z.enc	
VITAL Steering Committee	A steering committee consisting of members from The VHDL Technology Group, Ryan&Ryan, Synopsys, Cadence, Hewlett-Packard and Texas Instruments provides the day-to-day operations of the VITAL program.	
VITAL Membership	Over 45 companies have participated in the development of the VITAL technical plans. They have been led by William D. Billowitch, Steve Schulz and Eric Huyskens.	

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VHDL Newsletter	The VHDL Newsletter is sent for free (due to CEC support) to 1150 persons in Europe. By sending a request to the ECSI Office, you can obtain it.	

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Membership	The VFE is open to all interested persons. Membership can be applied by sending a letter to the address given above.	
Proceedings	Proceedings from previous VFE meetings can also be obtained at the same address.	

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