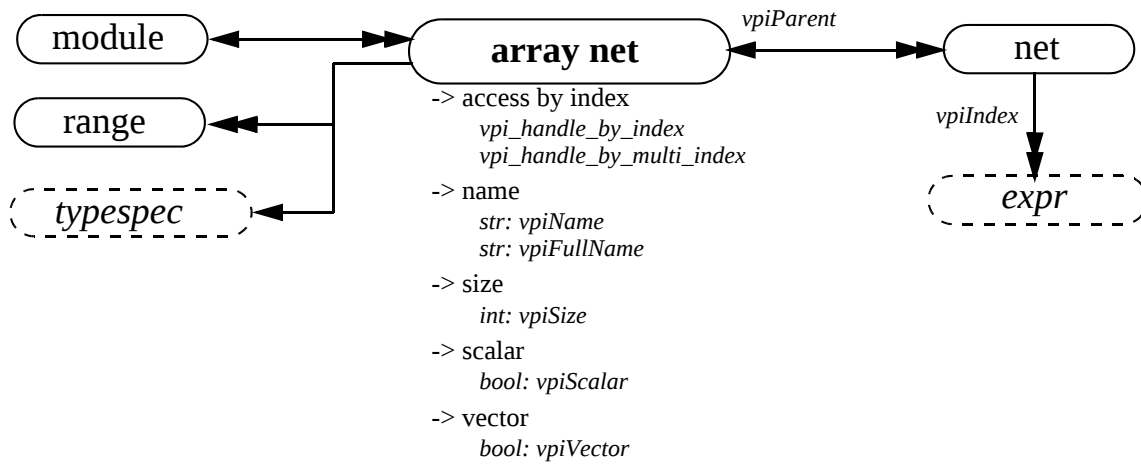


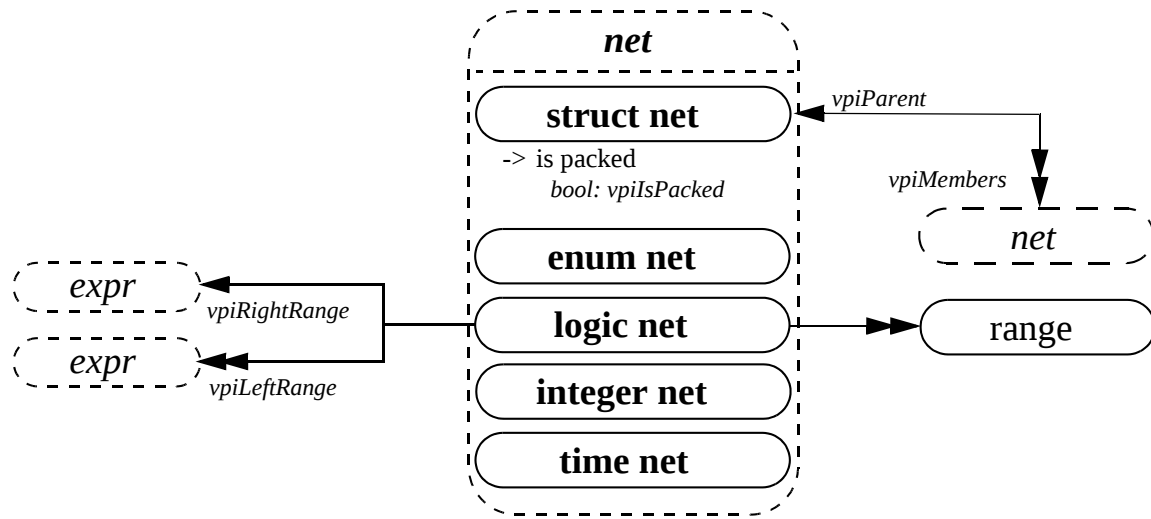
The diagram illustrates the internal structure of the VPI (Verilog Port Interface) component. It is organized into several hierarchical levels and components:

- Ports:** At the top left, there are two dashed boxes labeled *ports*. Arrows labeled *vpiPortInst* and *vpiLowConn* point from these ports to the *nets* component.
- Nets:** A large dashed box labeled *nets* contains:
 - An *array net* (rounded rectangle) at the top.
 - A *net* (dashed box) below it, which contains a *vpiParent* arrow pointing up to the *array net*.
 - A *net bit* (rounded rectangle) at the bottom, which has a *vpiBit* arrow pointing up to the *net*.
- Net Bit Details:** Below the *net bit* is a note: *-> constant selection bool: vpiConstantSelect*.
- External Connections:**
 - On the right, a series of arrows point from the *nets* component to various external modules: *vpiDriver* and *vpiLocalDriver* (pointing to *net drivers*), *vpiLoad* and *vpiLocalLoad* (pointing to *net loads*), *cont assign*, *prim term*, *path term*, *tchk term*, *vpiSimNet* (pointing to *nets*), and *typespec* (pointing to *typespec*).
 - On the left, a box labeled *vpiIndex* has two arrows pointing to *expr* (dashed boxes). One arrow is labeled *vpiIndex* and the other is unlabeled.

- (Notes not yet included)



(Notes not yet included)



-> access by index
vpi_handle_by_index
vpi_handle_by_multi_index
 -> array member
bool: vpiArray
 -> delay
vpi_get_delays()
 -> expanded
bool: vpiExpanded
 -> implicitly declared
bool: vpiImplicitDecl
 -> name
str: vpiName
str: vpiFullName

-> net decl assign
bool: vpiNetDeclAssign
 -> net type
int: vpiNetType
int: vpiResolvedNetType
 -> scalar
bool: vpiScalar
 -> scalared declaration
bool: vpiExplicitScalared
 -> sign
bool: vpiSigned
 -> size
int: vpiSize

-> strength
int: vpiStrength0
int: vpiStrength1
int: vpiChargeStrength
 -> value
vpi_get_value()
vpi_put_value()
 -> vector
bool: vpiVector
 -> vectored declaration
bool: vpiExplicitVectored

(Notes not yet included)