

Summary of Comments on SystemVerilog 3.1/draft 1

Page: 1

Sequence number: 1
Author: dwarmke
Date: 2/19/2003 4:50:18 PM
Type: Note
"a foreign code" should be "foreign code"

Sequence number: 2
Author: dwarmke
Date: 2/19/2003 4:51:16 PM
Type: Note
"chose" should be "choose"

Sequence number: 3
Author: dwarmke
Date: 2/19/2003 4:51:34 PM
Type: Note
"the" should be "a"

Sequence number: 4
Author: dwarmke
Date: 2/19/2003 4:56:04 PM
Type: Note
Suggest swapping this "Formal arguments..." paragraph with the paragraph above. That way open arrays will be defined before they are used. (Since the above paragraph currently forward references the concept)

Sequence number: 5
Author: dwarmke
Date: 2/19/2003 4:57:06 PM
Type: Note
Why "packed arrays and System Verilog arrays"? Do you really mean "both packed and unpacked arrays"? packed arrays are a kind of System Verilog array, so somehow this sentence isn't making sense.

Sequence number: 6
Author: dwarmke
Date: 2/19/2003 5:11:55 PM
Type: Note
The Overview section should explain the terms "extern function" and "exported function" early on (maybe even in the first paragraph, which is a related topic). The terms are referenced pretty often with no definition given. Most of the section is dedicated to type handling, array issues, and argument issues. If we want the overview at this level of detail, we should also cover function attribute types such as context and pure. We should also mention important limitations such as the prohibition on consuming time within a callee function.

Page: 2

Sequence number: 1
Author: dwarmke
Date: 2/19/2003 4:59:15 PM
Type: Note
Here I prefer "SV_CANONICAL_SIZE" over "sv_CANONICAL_SIZE".

Sequence number: 2
Author: dwarmke
Date: 2/19/2003 4:59:44 PM
Type: Note

"the binary compatability" should be "binary compatability"

Page: 3

Sequence number: 1

Author: dwarmke

Date: 2/19/2003 5:18:07 PM

Type: Note

"The Formal arguments" should be "Formal arguments"

Sequence number: 2

Author: dwarmke

Date: 2/19/2003 5:45:18 PM

Type: Note

The wording in this "The principle..." paragraph is confusing to me. A more natural English rendition would go something like, "External functions show up in two contexts on the SystemVerilog side of the interface: declarative and call-site. Formal argument types are completely governed by extern function declaration sites. If the actual argument types used at the call sites do not precisely match the formal arguments of the declaration, the system will coerce the actual types to match the formal types. This is the same behavior that already exists for Verilog-to-Verilog function calls."

Another point about this entire section is that it only mentions "external functions". I don't believe this section applies to exported functions, but I haven't seen the SV-side-interface in a long time. If there are separate declaration and definition sites for exported functions, then perhaps the same logic should apply to exported functions.

In any case I think we need a section that discusses a few basics about prototypes and formal argument types for exported functions called in C code. This might seem obvious, but I think we should mention for completeness that the user will be responsible for properly #including function prototypes for exported functions that are defined in SystemVerilog. We could also give the hint that friendly compilers could offer automatic generation of such function prototypes when compiling exported function declarations.

For the time being I think the title of the section should reflect that only external functions are treated. Perhaps call it "Formal argument types for external functions"

Page: 4

Sequence number: 1

Author: dwarmke

Date: 2/19/2003 5:25:22 PM

Type: Note

"the control" should be "control"

Sequence number: 2

Author: dwarmke

Date: 2/19/2003 5:26:07 PM

Type: Note

"their call" should be "their call instances" or "their call sites" (?)

Sequence number: 3

Author: dwarmke

Date: 2/19/2003 5:29:24 PM

Type: Note

"read or write anything" is pretty vague. Perhaps "read or write any operating system objects"?

Page: 5

Sequence number: 1

Author: dwarmke

Date: 2/19/2003 5:34:51 PM

Type: Note

"conveniently typedef'd" should be "conveniently typedef'd in svc.h or svc_src.h" (Otherwise the reader might think we are instructing them on how to write their code :)

Sequence number: 2
Author: dwarmke
Date: 2/19/2003 5:36:00 PM
Type: Note
"The layout of the unsized..." should be "The layout of unsized..."

Sequence number: 3
Author: dwarmke
Date: 2/19/2003 5:36:38 PM
Type: Note
"can be accessed with pointers" should be "can be accessed from C code with pointers"

Sequence number: 4
Author: dwarmke
Date: 2/19/2003 5:41:08 PM
Type: Note
This sentence "DirectC also supports the following SystemVerilog data types." doesn't really fit with the two bullets that follow. Rather, I would say "The following data representation requirements also apply." Maybe it's not even necessary to have the second bullet, since it is already thoroughly treated in the third bullet item directly above.

Page: 6

Sequence number: 1
Author: dwarmke
Date: 2/19/2003 5:45:57 PM
Type: Note
Could there be a cross-reference to a section that defines the "equivalence of packed types"?

Page: 7

Sequence number: 1
Author: dwarmke
Date: 2/19/2003 6:30:20 PM
Type: Note
I think we should include two unpacked dimensions in this example. This will make it clear that the unpacked dimensions are not linearized. Change to "logic [2:3][1:3][2:0] b [1:10][0:31]" and normalized form: "logic [17:0] b [0:9][31:0]" (Note: Andrzej should verify that the 31:0 is in the right order)
Point 3) above seems to indicate that the C type corresponding to a N-dimensional unpacked array should itself be a C array of N dimensions. This could be clarified by further extending this example to show an example of actual C code corresponding to such an argument. The main point is that the C code should look something like
sv_LOGIC_PACKED_ARRAY(18, b) [10][32];
Note the double-dimensioned array range specifier.
Maybe Example 2 (Sec 1.8.4) could be extended to include two unpacked dimensions, and then it could simply be cross-referenced here?

Sequence number: 2
Author: dwarmke
Date: 2/19/2003 5:56:54 PM
Type: Note
"The function arguments" should be "External function arguments"

Sequence number: 3
Author: dwarmke
Date: 2/19/2003 5:57:52 PM
Type: Note
"The actual arguments" should be "Actual arguments"

Sequence number: 4
Author: dwarmke
Date: 2/19/2003 5:58:04 PM
Type: Note
"The access" should be "Access"

Page: 8

Sequence number: 1

Author: dwarmke

Date: 2/19/2003 6:16:34 PM

Type: Note

A couple more points could be made in this section (Calling SystemVerilog functions from C):

1) If a C function needs to call an exported SV function that has arguments of native SV types (e.g. logic, packed array) then it will necessarily have to use "svc_src.h". Thus such C code is not guaranteed binary compatibility.

2) The C programmer needs to be careful to understand when an exported SV function is expecting arguments to be passed by reference rather than value. (Cross-ref the table or paragraph showing which types are passed by reference and which are passed by value.) If the rules are not followed, unexpected (and possibly disastrous) behavior will result.

NOTE from DOUG: Actually after I read the following sections 1.7.3-1.7.5, I realize the above points have already been covered.

Perhaps my additional observations here could be inserted into the appropriate sections.

Sequence number: 2

Author: dwarmke

Date: 2/19/2003 6:07:05 PM

Type: Note

"of the type" should be "of type"

Sequence number: 3

Author: dwarmke

Date: 2/19/2003 6:07:30 PM

Type: Note

"Statical allocation" should be "Static allocation"

Sequence number: 4

Author: dwarmke

Date: 2/19/2003 6:07:42 PM

Type: Note

"the knowledge" should be "knowledge"

Sequence number: 5

Author: dwarmke

Date: 2/19/2003 6:08:10 PM

Type: Note

"the binary" should be "binary"

Page: 11

Sequence number: 1

Author: dwarmke

Date: 2/19/2003 6:20:55 PM

Type: Note

"of the convenience" should be "of convenience"

Sequence number: 2

Author: dwarmke

Date: 2/19/2003 6:21:49 PM

Type: Note

"VCS" should be replaced with "a SystemVerilog simulator"

Page: 14

Sequence number: 1

Author: dwarmke

Date: 2/19/2003 6:34:44 PM

Type: Note

"writing a more" should be "writing more"

Sequence number: 2

Author: dwarmke

Date: 2/19/2003 6:35:02 PM

Type: Note

"inquires" should be "inquiries"

Sequence number: 3

Author: dwarmke

Date: 2/19/2003 6:40:30 PM

Type: Note

This intro area should specify that both packed and unpacked array dimensions can be unsized.

Sequence number: 4

Author: dwarmke

Date: 2/19/2003 7:27:11 PM

Type: Note

"as a open" should be "as an open"

Page: 15

Sequence number: 1

Author: dwarmke

Date: 2/19/2003 6:38:45 PM

Type: Note

"a variable argument list function" should be "variable argument list functions".

Sequence number: 2

Author: dwarmke

Date: 2/19/2003 6:38:57 PM

Type: Note

"the specialized" should be "specialized"

Sequence number: 3

Author: dwarmke

Date: 2/19/2003 7:28:31 PM

Type: Note

"shall be used" should be "shall be used when working with elements."

Sequence number: 4

Author: dwarmke

Date: 2/19/2003 8:04:22 PM

Type: Note

"element" should be "elements"

Sequence number: 5

Author: dwarmke

Date: 2/19/2003 8:04:36 PM

Type: Note

"the arrays" should be "arrays"

Sequence number: 6

Author: dwarmke

Date: 2/19/2003 8:04:49 PM

Type: Note

"the vendors" should be "vendors"

Sequence number: 7

Author: dwarmke

Date: 2/19/2003 8:05:19 PM

Type: Note

"it is not be possible" should be "it is not possible"

Sequence number: 8

Author: dwarmke
Date: 2/19/2003 8:05:32 PM
Type: Note
"such array" should be "such an array"

Sequence number: 9
Author: dwarmke
Date: 2/19/2003 8:05:44 PM
Type: Note
"such array" should be "such an array"

Page: 16

Sequence number: 1
Author: dwarmke
Date: 2/19/2003 8:06:22 PM
Type: Note
This comment is indented one tab stop too far.

Sequence number: 2
Author: dwarmke
Date: 2/19/2003 8:06:37 PM
Type: Note
"array's" should be "array"

Sequence number: 3
Author: dwarmke
Date: 2/19/2003 8:09:05 PM
Type: Note
Change title of section to "Access to elements via canonical representation"

Page: 17

Sequence number: 1
Author: dwarmke
Date: 2/19/2003 8:10:34 PM
Type: Note
Change title to "Access to scalar elements (bit and logic)"