Minor Corrections

1.1 Unmatched parenthesis on Page 214 in Section 17.7.2

Change

```
This is equivalent to:
a ##1 ((!b [*0:$] ##1 b) + [*min:max]) ##1 c
```

Change

```
This is equivalent to:

a ##1 ((!b [*0:$] ##1 b) + [*min:max]) ##1 !b[*0:$] ##1 c
```

1.2 Semantic rules on Page 214, Section 17.7.2

Change

```
— expression [*n:m], where n-is the minimum, m-is the maximum [*m:n], where m is the minimum, n is the maximum, and m >= 0, m<= n or n is $</p>
```

1.3 Changes on Page 218 in Section 17.7.4

Change

The following example is an expression with the and and operator, where the two operands are single sequence evaluations. The operation is illustrated in Figure 17-4.

The operation as illustrated in Figure 17-4 shows the evaluation attempt at clock tick 8. Here, The the two operand sequences are (tel ##2 te2) and (te3 ##2 te4 ##2 te5). The first operand sequence requires that first te1 evaluates to true followed by te2 two clock ticks later. The second sequence requires that first te3 evaluates to true followed by te4 two clock ticks later, followed by te5 two clock ticks later. Figure 17-4 shows the evaluation attempt at clock tick 8.

1.4 Change on Page 225 in Section 17.7.11

Change (paragraph just before Figure 17.14)

specifies looking for the rising edge of frame within two clock ticks in the future. After frame toggles high, irdy must also toggle high after one clock tick. This is illustrated in Figure 17-14 for the evaluation attempt at clock tick 6. 'data_end_exp is acknowledged at clock tick 6. Next, frame toggles high at clock tick 7. Since this falls within the timing constraint imposed by [1:2], it satisfies the sequence and continues to monitor evaluate further. At clock tick 8, irdy is evaluated. Signal irdy transitions to high at clock tick 8, satisfying matching the sequence specification completely for the attempt that began at clock tick 6.

1.5 Complete the example on Page 258, Section 17.13

Change

- default clock, for example

```
default clocking master_clk @(posedge clk);
property p4; (a ##2 b); endproperty
```

assert property (p4);

1.6 Change on Page 258 in Section 17.13.

Change (Above Table 17-3)

These example sequences are used in Table 17-2 to explain the clock resolution rules for a sequence definition. The clock of any sequence when explicitly specified is indicated by X. The absence of a clock is indicated by a dash. Otherwise, it is indicated by a dash.