SystemVerilog 3.1a
SV-AC Update
13 November 2003

Faisal Haque (Cisco) – Chairman

Arif Samad (Synopsys) – Co-Chairman

Status

- Extensions
  - Received 16 proposals which have been accepted
  - All proposals have been reviewed in committee meetings
    - Committee meeting weekly
    - Several proposals have been revised based on feedback
  - Planning to hold straw poll this week to determine which proposals have support
  - Authors of proposals that have reasonable support will create drafts in form suitable for inclusion in LRM
- Errata
  - 8 items considered in committee
  - 7 items had corrections approved
  - Additional errata proposed in e-mail but not yet discussed in committee
- Committee Membership
  - Active participants from Cadence, Cisco, Intel, LSI, Motorola, Novas, Sun, Synopsys
  - 10 individuals have voting status
  - 8 companies have voting status