SystemVerilog Basic Committee

Johny Srouji (Chair)
Karen Pieper (Co-Chair)

SV-BC Participants

17 Active Participants

Matt Maidment	- Intel
Brad Pierce	- Synopsys
Karen Pieper	- Synopsys
Johny Srouji	- Intel
Dan Jacobi	- Intel
Dave Rich	- Synopsys
Francoise Martinolle	- Cadence
Jay Lawrence	- Cadence
Dennis Brophy	- Mentor
Vassilios Gerousis	- Infineon
Cliff Cummings	- Sunburst Design
Mark Hartoog	- Synopsys
Don Mills	- LCDM Engineering
Doug Warmke	- Mentor
Rishiyur Nikhil	- Bluespec
Stu Sutherland	- Sutherland HDL
Peter Flake	- Synopsis

101 Members of Email Reflector

Sunburst Design	0-in
Infineon	Cisco
Verplex	Synplicity
Synopsys	Parthosceva
NSC	Telllabs
Xilinx	Doulos
Cadence	Interra Systems
Applistar	Bluespec
Axis	Boyd Techonology
LSI	Handasarabia
Verisity	Expert EDA
Motorola	
Mentor	
Willamette HDL	
LCDM	
Intel	

SV-BC Status

- Mission
  - Address remaining issues from System Verilog 3.0
  - Address issues exposed in SystemVerilog 3.1 standard through implementation
  - Handle all design modeling issues, such as refinements of the language as well as design enhancements, to solidify System Verilog as RTL design language
- Goal
  - Be complete with 3.1A release by DVCON 2004

SV-BC: Accomplishments

- Issue status
  - 118 issues have been filed
  - 64 (54%) have been addressed
    - 35 closed
    - 2 passed
    - 18 updated
    - 9 committed (separate compilation)
  - 16 (13%) have proposals
  - 37 (31%) are currently open, deferred
- As a process, it was agreed that an issue must have an owner before it is discussed
- Active participation and progress
  - Decided to hold a F2F meeting to make progress complex issues

SV-BC: Accomplishments

- Accepted Proposals
  - SV-BC-48 - Flexibility in Function description and use
  - SV-BC-49 - Operator overloading
  - SV-BC-53 - Expand array querying functions
  - SV-BC-54 - Changing ref ports for variables in an interface
  - SV-BC-71 – BlueSpec donation
  - SV-BC-72 - $inside operator
  - SV-BC-67 - Memory pattern file formats
- These proposals will be discussed for approval on F2F meeting

Separate Compilation

- A separate compilation proposal was developed and approved by the Separate Compilation task force.
  - Adds a separate compilation unit to the language
  - Limits $root to a separate unit
  - Provides packages as a method to share data among units
- Proposal was sent to all committees for comments
- Completed proposals will be reviewed and voted on by SV-BC for acceptance into the standard

SV-BC: Milestones

- 7 July 2003 – Committee started operating
- 4 August 2003 – Close of submission commitments
- 15 September 2003 – Close of submissions
- 1 December 2003 – Complete technology errata, freeze technology of submissions, close implementation feedback
- 24 December 2003 – End of LRM development, start of LRM review
- 24 January 2004 – Send to board
- 24 February 2004 – Release 3.1a LRM