

### SV-EC Status 14 November 2003

David Smith – Chairman Neil Korpusik – Co-Chairman



# Agenda

- Mission
- Members
- Status
- Milestones
- Challenges
- SystemVerilog LRM Status





## **Mission**

 Maintain and extend the SystemVerilog language for testbench support





## Members

Voting Company Members	Non-Voting Company Members (due to attendance)	Participating Individual Members
Arturo Salz (Synopsys)	Chris Spear (Synopsys)	Don Mills (LCDM)
Brad Pierce (Synopsys)	Jeff Freedman (ModelTech)	James Young (HP)
Cliff Cummings (Sunburst Design)	Stu Sutherland (Sutherland HDL)	
Dave Rich (Synopsys)		
David Smith (Synopsys)		
Dennis Brophy (ModelTech)		
Jay Lawrence (Cadence)		
Michael Burns (Motorola)		
Mehdi Mohtashemi (Synopsys)		
Neil Korpusik (Sun)		
Ray Ryan (ModelTech)		





## Status - Errata

#### Errata

- 43 items have been identified
- 38 have been closed
- 1 has been proposed
  - built-in global package
  - waiting for the Package and Separate Compilation proposal
- 4 have been assigned and will be closed by the end of November (clarifications)
  - ERR-4: Lifetime of automatic variables in fork/join\_\*
  - ERR-8: Using Event Controls with Methods
  - ERR-20/21: Fix example based on ERR-4 resolution





## **Status - Extensions**

- Extensions logged: 15
  - Moved:
    - EXT-6 Size of types (1 page)
    - EXT-13 to SV-BC general namespace support
  - Closed with no action:
    - EXT-5 Optional order of sign, etc...
  - Closed with no submission:
    - EXT-1 Additional string routines
    - EXT-4 Additional tasks for new types
  - Approved:
    - EXT-2 Fine Process Control (2 pages)
    - EXT-8 RandCase support (close to approval) (1 page)
    - EXT-11 Dynamic Queue Support (6 pages)
    - EXT-15 General foreach construct (1 page)
    - EXT-9 Stream Generation (7 pages)
    - EXT-10 Functional Coverage Specification (10 pages)
    - EXT-14 Constraint completion (11 pages)
  - Accepted:
    - EXT-7 Reacting to assertions (3 pages)
    - EXT-3 Virtual interfaces/ports (5 pages)
    - EXT-12 Bit stream support (pack/unpack) (6 pages)





### **Milestones**

#### Completed:

- 7 July 2003 Committees start operating
- 4 August 2003 Close of submission commitments
- 15 September 2003 Close of submissions

#### Upcoming:

- 1 December 2003
  - Complete technology errata
  - freeze technology of submissions
  - close implementation feedback

#### To come:

- 24 December 2003 End of LRM development, start of LRM review
- 24 January 2004 Send to board
- 24 February 2004 Release 3.1a LRM





# Challenges

Keeping coordinated with other committees





## Status – LRM Changes

- Draft 1 Complete on 29 October 2003
  - 37 Change requests
    - SV-AC: 2 change requests (formal semantics clean-up)
    - SV-BC: 16 change requests (BNF changes, both corrections and updates from 1364, and clean-up)
    - SV-CC: 3 change requests (BNF and Open array consolidation with dynamic arrays)
    - SV\_EC: 16 change requests (Extensions plus clean-up)
- Draft 2 Planned for 1st week of December
  - http://www.eda.org/sv/LRMChanges\_draft2.html
  - 19 change requests (so far)
    - SV-AC: 0
    - SV-BC: 4 (BNF corrections plus 1364 BNF updates)
    - SV-CC: 1 (correction)
    - SV-EC: 14 (Extensions plus corrections/clarifications from committee and Infineon review)

SystemVerilog