SV-AC Update
18 September 2003

Faisal Haque – Chairman

Arif Samad – Co-Chairman

Agenda

- Mission

- Members

- Status

- Milestones

13 May 2003   www.accellera.org

Mission

- Incorporate feedback from EDA vendor implementations of 3.1 and customer usage

- Complete enhancements from v3.1 development required to make SystemVerilog a solid foundation for HDVL

Members

Voting Company Members	Non-Voting Company Members (due to attendance)	Participating Individual Members
Faisal Haque (Cisco)	Arif Samad (Synopsys – replacing Steve)	Connie O'Dell (consultant)
Steve Meier (Synopsys - outgoing)	Richard Ho (0-In)	
Roy Armoni (Intel)		
Surrendra Dudani (Synopsys)		
Cindy Eisner (IBM)		
John Havlicek (Motorola)		
Adam Krolnik (LSI)		
Joseph Lu (Sun)		
Eric Marschner (Cadence)		
Andrew Seabright (0-In)		
Bassam Tabbara (Novas)		
Tej Singh (Mentor)		
Hillel Miller (Motorola)		

Status - Errata

- Errata items logged: 7
    - Closed: 6
        - Associativity – change to right
        - Allow clocked sequences(including multi-clock) to be parenthesized
        - Parenthesis around expression with local variable assignments
        - Formal semantics needs to define meaning of multiple local variables attached to a single boolean
        - need to define neutral trace semantics, in alignment with PSL
    - Items in progress: 1
        - unary ## should have the higher precedence than binary ##

Status - Extensions

- Extensions logged: 26
  - Moved:
    - EXT-18 General clocked event object triggered on completion of assertion (SV-EC)
    - EXT-19 Extend expect to support wait on in-lined sequence event… (SV-EC)
    - EXT-20 Feature to embed assertions within a user defined type… (SV-BC)
  - Closed:
    - EXT-17, 21
  - For consideration beyond 3.1a
    - EXT 22 – template feature (should be passed to BC)
    - EXT 23 – extend time windows to allow negative delays
    - EXT 24 - assertions on variables, classes, dynamic objects
    - EXT 25 - allow additional temporal operators…
    - EXT 26 – More fomal features

Status – Extensions (continued)

- Submitted:
  - EXT-1 – Assume directive for concurrent assertion… (Surrendra)
  - EXT-2 - Assume directive that must hold for all times (Joseph)
  - EXT-3 - Alignment/ synchronization with testbench constraints language (Surrendra)
  - EXT-4 - Local variable reference outside of containing assertion (John)
  - EXT-5 - Non-blocking clocked assignment variables… (Surrendra)
  - EXT-6 - Message reporting using assertion values,… (Surrendra)
  - EXT-7 - Support parameters for assertions, extend to allow sequence… (Joseph)
  - EXT-9 - Allow passing of infinite range as argument… (Surrendra)
  - EXT-11 - Dynamic and recursive calls to a property… (John)
  - EXT-12 - Boolean connectives, nesting… (John)
  - EXT-13 - Assertions inside of functions (Adam)
  - EXT-14 – Enhance gated clock support (Surrendra)
  - EXT-15 - Report interface assertion messages in child scope… (Adam)
  - EXT-16 – Extend modport to enable assertions in modport statement (Adam)

Milestones

- 7 July 2003 – Committees started operating
- 12 August 2003 – Close of submission commitments
- 15 September 2003 – Close of submissions
- 1 December 2003 – Complete technology errata, freeze technology of submissions, close implementation feedback
- 24 December 2003 – End of LRM development, start of LRM review
- 24 January 2004 – Send to board
- 24 February 2004 – Release 3.1a LRM

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