Accellera SystemVerilog

SystemVerilog 3.1A Technical Committees

Accellera SystemVerilog 3.1A Agenda

- Introduction
- SystemVerilog 3.1A Committee Status:
  - Testbench Enhancement Plus SV3.1A LRM (David Smith-Synopsys)
  - Design Enhancement - (Johny Srouji- Intel)
  - DPI enhancement -- (Swapnajit Mittra - SGI)
  - Assertions Enhancement -- (Faisal Haque - CISCO)
- **LRM status, including BNF.**
- **JEITA Activities with SystemVerilog.**
- **Issues.**
- **Accellera efforts to move forward with other activities related toSystemVerilog:**
  - **a- SystemVerilog Acceleration Working Group.**
  - **b- Modeling Group.**
  - **c- SystemVerilog-AMS (engagement with Verilog-AM**
  - **committee).**
  - **d- Interoperaibility with VHDL, SystemC.**
  - **Assertions for VHDL**

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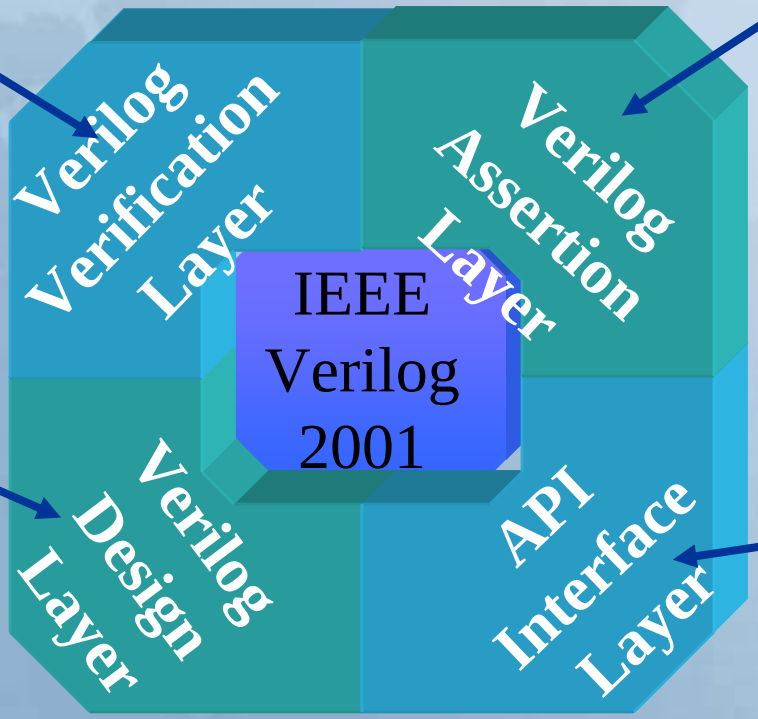
SystemVerilog Charter

- **Charter: Extend Verilog IEEE 2001 to higher abstraction levels for Architectural and Algorithmic *Design* , and *Advanced Verification*.**

Transaction-Level Full Testbench Language with Coverage



Advanced verification capability for semiformal and formal methods. The Assertion Language Standard For Verilog

Design Abstraction: Interface semantics, abstract data types, abstract operators and expressions

DPI interface, Assertion API, SV API and Coverage API

SystemVerilog 3.1A Milestones

- Language Development – Complete by end of January 2004
- Extensive LRM review and corrections - Complete by March 10 2004
- Submit LRM to the TCC and Accellera Board by March 15.
  - LRM review will continue until middle of March.
  - Clean LRM will be generated by end of March
- Approval by the Accellera Board is planned for April 15.
  - Errata will be collected and released as addedum to the 3.1A standard.
- Transfer to IEEE by June 2004.

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